Voltage Control of a Single Distributed Generation Unite in Autonomous Mode Operation Under Unbalance and Non-linear Load Conditions.

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Abstract—This paper propose a voltage control of a single distributed generation (DG) unit powered local load. The DG system utilizes three phase four wire voltage source inverter VSI with split DC link as the medium interface and LC filter to attenuate the switching frequency harmonics. A dual loop scheme is employed. Dead beat current controller in inner loop, which achieve fast dynamic response. In the outer loop, Multi-generalized resonant filter with feedback state is employed to track reference voltage and eliminate the low order harmonics, and to make the dynamic of the system greatly adjustable via pole-placement strategy.

The proposed controller provides a set balanced three phase voltage with low THD equal to 1.80% in worse case (non linear load) for a locale load, despite unbalanced and distorted current load, guarantee a robust stability, fast dynamic response to disturbance, zero steady state error. Effectiveness of the proposed control strategy is evaluated based on time domain simulation studies in Matlab/ Simulink™ environment.

Keywords—Distributed Generation DG; Dead beat Controller; resonant filter Controller; pole placement technique; Autonomous Mode Operation; Voltage Controller; VSI with split DC link.

I. INTRODUCTION

In the last years, the number of distributed generation DG unites has increased considerably to meet power electricity demand. The various reasons which make this kind of production very attractive: Economic and environment benefits, power quality improvement, ... [1]. Many of DG resources require a power electronic interface. The control of this converter depends on the operation mode. In the grid connected mode, the control of the converter is performed to export power to the grids. However, in autonomous mode, the DG unite supplies a local load.

In autonomous mode, the DG should provide a high quality sinusoidal voltage waveforms to the customer despite the nature of the load. The most connected load to DG are; non-linear which cause distortion of the output voltage a common example; computers communication equipments. ... [2], a single phase and so negative and zero sequence output voltage are expected, and randomly switched with different dynamic/static properties [3]. In this context, the control of DG unite in autonomous mode is a challenging task.

The control scheme of the DG system power electronic interface in autonomous mode should provide:

- Set balanced three phase voltage despite unbalanced current load.
- Fast transient in case of connection or disconnection of the load.
- Low distortion harmonic (THD) of the output voltage.
- Robust stable operation for large load parameters variations.
- Allows Limitation of the inverter current (dangerous to the semiconductors).

To achieve these goals, various techniques have been reported in the literature.

The Proportional Integrator PI controller has been employed in [4]. However, the use of PI controller in the stationary a,b,c frame results in an unstable system if the loop gain is increased further than a specific limit. There also exists an inherent steady state error impossible to eliminate for non DC signal [5], which degrades the performance of the system in presence of harmonic.

Alternatively, PI controller in d-q reference frame [6] achieves zero steady state error, by transforming the system from the natural reference frame a,b,c to the synchronous rotating frame, the measured voltage and current can be translated from AC to DC variables. Yet, these assumptions are true only if the connected load to the DG is linear and balanced, which in practice is not the case, and the performance of the system could be deteriorate, especially in nonlinear load conditions. The authors [7] have proposed multi rotating reference frames, to accommodate load unbalance and nonlinearity. The resulted regulator is more complex as it involves a multi synchronous reference frames.

Reference [8] has proposed poles placement control strategy via integral state feedback applied on voltage regulator designed in q-d reference frame for four leg inverter to make transient of the system adjustable. Therefore, the performances of the system are not evaluated for non linear and unbalance load conditions.

In [9],[10] have used sliding mode technique to design the voltage controller. But, sliding mode control suffer from phenomena known as "chattering" which can be caused by parasitic of sensor or feedback components [11]. In this last

reference, authors have developed a deadbeat with feed-forward controller for both voltage and current loops, presented result in static and dynamic term for linear and nonlinear load is sensibly good. But, deadbeat control signals largely depend on a precise model of the system, which might affect the stability of the system, especially in the case of double dead beat controller loop.

The authors of [12] have applied H_∞ design procedure onto single phase inverter to improve robust stability under load disturbance and model uncertainty. In this case, the control performance under non linear load is not satisfactory.

The internal model principle has been proposed by Francis and Wonham [13] states that the controlled output tracks a reference commands in the presence of disturbances (zero steady state tracking error), can be achieved if the models that generate these references and disturbances are included in the stable closed loop systems.

The repetitive controller (RC) works on the internal model principle, it has potential to eliminate periodical error or disturbance whose frequency is less than half sampling frequency. This control technique has widely [14],[15],[16] and [17]. However, the main drawback of the repetitive controller is the slow dynamic transient, requires a large memory space and the difficulty to stabilize the system.

An attractive approach to eliminate errors which also used the internal model principle, is to introduce the mathematical model of sinusoidal reference along the open loop path to ensure almost zero steady state error. This regulator is called resonant controller, also known as generalized integrator. The advantages of this controller over RC controller are, the selective harmonic compensation, which generally enough for DG interface medium since and the high harmonics can be eliminated by the LC output filter.

Resonant regulator used in [18] to track the reference output voltage without steady state error and eliminate disturbance. However, a controller base only on the internal model cannot guarantee a good transient performance when the system is affected by disturbance, especially in fluctuating load condition.

In [2] and [19] a proportional is associated with resonant regulator to improve transient performances of the system, but there is not systematical method of stabilizing the system.

The author of [20] proposed, resonant regulator combined with a plant state feedback controller. This technique allows fast dynamic transient and strong harmonic rejection. Non inner current control loop is used and the current under overload or fault conditions can not limited

This article suggest, a dual loop scheme to regulate the output voltage of DG unite powered local load, the current controller in inner loop and voltage regulator in the outer loop. Dead beat current controller is used to achieve fast dynamic response. Multi-generalized resonant filter with feedback state is employed to: track sinusoidal voltage reference, eliminate the low-order harmonics, and adjust the dynamic of the system via pole-placement strategy. The proposed control scheme presents a good performance in voltage reference tracking, low-order voltage harmonics elimination and load disturbance rejection under nonlinear and unbalanced load conditions.

The remainder of this article is organized as fellows. Section 2 describes the control plan modeling. Section 3 illustrates the

proposed control scheme. Simulation results are shown in section 4, and section 5 concludes the paper.

II. MODELING OF THE ISLANDED DG UNIT SYSTEM

Fig.1 illustrates three-phase DG unit system studied in this work. The DC voltage bus are assumed supplied by ideal DC voltage source, which can be released by DC voltage regulated front end with storage system energized by a distributed generator, which can be, wind turbine, photovoltaic device... The interface system of DG unit is composed from three phase inverter three phase second order L-C filter, The neutral is connected to the middle point of the two DC capacitors on the DC link of inverter and so this is called a "split capacitor inverter". The output voltage is fed three sets of local load ;1) three phase balanced load, 2) three phase unbalanced load, and 3) nonlinear load. The unbalance load represent unequal single phase loads which are connected between the phases and neutral conductor.

In the system proposed the neutral point of the output filter and the load are connected to the middle-point of the capacitor bank through an inductance to limit the neutral current.

Fig. 1. Three-phase four-wire inverter with a split DC bus.

Due to the presence of balanced DC link, we consider this system as three independent single phase, and hence there is no needs to study here the three phase behavior of the system. A simplified model of the system is shown in Fig.2.

Where C_F , L_F and R_F are the filter parameters, capacitance, inductance and resistance respectively.

And $i_{I,x}$: Generated phase inverter current.

$v_{I,x}$: Neutral-phase inverter output voltage.

$v_{L,x}$: Neutral-phase load voltage.

$i_{L,x}$: Load current.

And x represent the corresponding phase x=a, b, c.

A state space model of this system is:

$$\begin{cases} \frac{dX}{dt} = A.X + B.U + H.\zeta \\ Y = C.X \end{cases} \quad (1)$$

Where: the state variable $X^T = [v_{L,x} \ i_{I,x}]$, the control signal $U = u_{inv,x}$ and the disturbance $\zeta = i_{L,x}$

And the coefficients are $A = \begin{bmatrix} 0 & 1/C_F \\ -1/L_F & R_F/L_F \end{bmatrix}$; $B = \begin{bmatrix} 0 \\ 1/L_F \end{bmatrix}$; $H = \begin{bmatrix} -1/C_F \\ 0 \end{bmatrix}$; and $C = [1 \ 0]$

Fig. 2 .Single phase equivalent for three phase four wire inverter

Space model of this system in a,b,c frame is:

$$\begin{cases} \frac{dX}{dt} = A \cdot X + B \cdot U + H \cdot \zeta \\ Y = C \cdot X \end{cases} \quad (1)$$

Where: the state variable $X^T = [v_{L,x} \ i_{L,x}]$, the control signal $U = u_{inv,x}$ and the disturbance $\zeta = i_{L,x}$

And the coefficients are $A = \begin{bmatrix} 0 & 1/C_F \\ -1/L_F & R_F/L_F \end{bmatrix}$; $B = \begin{bmatrix} 0 \\ 1/L_F \end{bmatrix}$; $H = \begin{bmatrix} -1/C_F \\ 0 \end{bmatrix}$; and $C = [1 \ 0]$.

Using zero order hold method, the discrete time domain of the above equation system (1) can be described as follows:

$$\begin{cases} X^d(k+1) = A^d \cdot X^d(k) + B^d \cdot U^d(k) + H^d \cdot \zeta^d(k) \\ Y^d(k) = C^d \cdot X^d(k) \end{cases} \quad (2)$$

Where; $A^d = \int_0^T e^{A(t-\tau)} d\tau$, $B^d = \int_0^T B \cdot e^{A(t-\tau)} d\tau$,

$H^d = \int_0^T H \cdot e^{A(t-\tau)} d\tau$, and $C^d = C$

And T is the sampling period.

III. CONTROL SYSTEM STRUCTURE

A dual loop control structure (current loop and voltage loop) is proposed in this work, the basic idea is controlling the inverter current in order to regulate the output voltage. A dead beat current controller is used to achieve fast dynamic response. The outer loop is for output voltage control, the core of this controller is a multi-resonant filter to eliminate unwanted harmonic, the state feedback is associated with multi resonant filter to make the dynamic of the system adjustable.

A. Design of the Current Controller

The design of the current controller is based on the internal model of the system, which is used to predicate the behavior of the system. The main objective of the dead beat controller is to compute the inverter reference voltage to feed a PWM modulator for switching the inverter.

From the discrete state space model of the system equation (2), the inverter current can be write as:

$$i_L(k+1) = a_{22}^d \cdot i_L(k) + a_{21}^d \cdot v_L(k) + b_2^d \cdot u_{inv}(k) + e_2^d \cdot i_L(k) \quad (3)$$

And

$$u_{inv}(k) = \frac{1}{b_2^d} (i_L(k+1) - a_{22}^d \cdot i_L(k) - a_{21}^d \cdot v_L(k) - e_2^d \cdot i_L(k)) \quad (4)$$

Where the coefficients (a_{22}^d, a_{12}^d) , b_2^d and e_2^d are the elements of matrices A^d , B^d and E^d respectively.

Using the system parameters given in the table I we have found $e_2 \cong 0$ and $a_{22} \cong 1$.

Equation (4) becomes:

$$u_{inv}(k) = \frac{1}{b_2^d} (i_L(k+1) - i_L(k) - a_{21}^d \cdot v_L(k)) \quad (5)$$

The inverter voltage for the next step is given by:

$$u_{inv}(k+1) = \frac{1}{b_2^d} (i_L(k+2) - i_L(k+1) - a_{21}^d \cdot v_L(k+1)) \quad (6)$$

Adding (5) to (6), and by assumption the load voltage for instant k equal to the next step, we find:

$$u_{inv}(k+1) = \frac{1}{b_2^d} (i_L(k+2) - i_L(k) - 2 \cdot a_{21}^d \cdot v_L(k)) - u_{inv}(k) \quad (7)$$

To let the inverter current of the step $i_L(k+2)$ track the reference inverter current $i_L^*(k)$, the reference inverter voltage should be:

$$u_{inv}(k+1) = \frac{1}{b_2^d} (i_L^*(k) - i_L(k) - 2 \cdot \widetilde{a_{21}^d} \cdot v_L(k)) - u_{inv}(k) \quad (8)$$

Where $\widetilde{b_2^d}$ and $\widetilde{a_{21}^d}$ are the estimated coefficients of b_2^d and a_{21}^d respectively, depend only on the estimated inverter inductance.

We assume that there is no error model. The close loop system exhibits two poles located in the origin of the complex z plant and no zeroes.

The augmented state space model (discrete state space model of the system with current controller) can be described as:

$$\begin{cases} X^{d1}(k+1) = A^{d1} \cdot X^{d1}(k) + B^{d1} \cdot U^{d1}(k) + H^{d1} \cdot \zeta^{d1}(k) \\ Y^{d1}(k) = C^{d1} \cdot X^{d1}(k) \end{cases} \quad (9)$$

Where the state variable $X^{d1T} = [v_L(k) \ i_{inv}(k) \ v_{inv}(k)]$, the control signal $U^{d1} = i_{inv}^*(k)$ and the disturbance $\zeta^{d1} = i_L(k)$

$$A^{d1} = \begin{bmatrix} a_{11}^d & a_{12}^d & b_1^d \\ a_{21}^d & a_{22}^d & b_2^d \\ -\frac{2 \cdot a_{21}^d}{b_2^d} & -\frac{1}{b_2^d} & -1 \end{bmatrix}; B^{d1} = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{b_2^d} \end{bmatrix}; H^{d1} = \begin{bmatrix} h_1^d \\ h_2^d \\ 0 \end{bmatrix} \text{ and } C^{d1} = [1 \ 0 \ 0].$$

B. Design of the Voltage Controller

Fig.3 shows voltage control scheme block, the voltage controller is composed from multi-resonant filter with state feedback, to guarantee the output voltage quality and high dynamic disturbance rejection. Consequently, the reference output voltage can be tracked without steady state error and the dynamic of the resulted system could be adjusted.

The resonant filter used in [5] to track reference output voltage introduces an infinite gain for the specific frequency, which could cause stability problems.

Damped resonant filter introduced by [21]. Is used to avoid this problem. Other advantage of damped resonant filter, is the

providing an appropriate resolution for the resonant filter coefficients (in the fixed point processor applications) [19].

$X^{d2^T} = [X^{d1^T} \quad X_h^{d^T}]$, the control signal is $U^{d1} = i_{inv}^*(k)$

Fig 3. Synoptic of the output voltage control scheme of DG unit

In DG system, the high harmonics have already suppressed by the LC output filter.

And the major components that may affect the performance of the system are low harmonics, typically third, fifth, and seventh order harmonics [5].

The transfer function of damped multi-resonant filter is expressed as:

$$G(s) = \frac{s+1}{s^2+2\omega_c s+\omega_0^2} + \sum_{l=3,5,7} \frac{s+1}{s^2+2\omega_c s+(l\omega_0)^2} \quad (10)$$

Where; ω_0 is the resonant frequency of the selected resonance frequency and ω_c damped coefficient. Typically, the choice of ω_c is tradeoff between sensibility of the resonant filter to frequency deviation and the rejection of steady state error capability. In practice, the value of 5-15rad/s found to provide a good compromise [19]

The transfer function can be written in the state space as:

$$\frac{dX_h}{dt} = A_h \cdot X_h + B_h \cdot U_h \quad (11)$$

Where: $X_h^T = [X_1^T \quad X_3^T \quad X_5^T \quad X_7^T]$, $U_h = v_{ref}(t) - v_L(t)$.

$$A_h = \begin{bmatrix} A_{h1} & 0 & 0 & 0 \\ 0 & A_{h3} & 0 & 0 \\ 0 & 0 & A_{h5} & 0 \\ 0 & 0 & 0 & A_{h7} \end{bmatrix}; B_h = \begin{bmatrix} B_{h1} \\ B_{h3} \\ B_{h5} \\ B_{h7} \end{bmatrix}$$

$$A_{hl} = \begin{bmatrix} 0 & 1 \\ -(l\omega_0)^2 & -2\omega_c \end{bmatrix}; B_{hl} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}; X_l = \begin{bmatrix} X_l \\ X'_l \end{bmatrix}$$

$l = 1, 3, 5, 7$

Using zero order hold method, the discrete time domain can be described as follows:

$$X_h^d(k+1) = A_h^d \cdot X_h^d(k) + B_h^d \cdot U_h^d(k) \quad (12)$$

Where $A^d = \int_0^T e^{A(t-\tau)} d\tau$, $B^d = \int_0^T B \cdot e^{A(t-\tau)} d\tau$,

$$H^d = \int_0^T H \cdot e^{A(t-\tau)} d\tau$$

and T: is the same sampling period as above.

The new augmented system can be write as:

$$X^{d2}(k+1) = A^{d2} \cdot X^{d2}(k) + B_1^{d2} \cdot U_1^{d2}(k) + B_2^{d2} \cdot U_2^{d2}(k) + H^{d2} \cdot \zeta^{d2}(k) \quad (13)$$

Where the state variables are:

and $U^{d2} = v_{ref}^*(k)$, and the disturbance is $\zeta^{d2} = \zeta^{d1} = i_L(k)$

And the coefficients are $A^{d2} = \begin{bmatrix} A^{d1} & 0_{3 \times 8} \\ -B_h^d & 0_{8 \times 2} \end{bmatrix}$;

$$B_1^{d2} = \begin{bmatrix} B^{d1} \\ 0_{8 \times 1} \end{bmatrix}; B_2^{d2} = \begin{bmatrix} 0_{3 \times 1} \\ B_h^d \end{bmatrix} \text{ and } H^{d1} = \begin{bmatrix} H^{d1} \\ 0_{8 \times 1} \end{bmatrix}$$

The control input to the system is the reference current, which expressed as:

$$i_{inv}^*(k) = K \cdot X^{d2}(k) \quad (13)$$

The problem control to be solved is to compute the matrices gain $K = [K_1 \quad K_2]$.

In order to provide good response and rejection of disturbance, pole placement technique is used in this work.

IV. COMPUTER SIMULATIONS RESULTS

This section is devoted to verify the performances of the proposed control scheme by means of computer simulations using Matlab/SimulinkTM, where the inverter is fully modeled and the control system is implemented in discrete time. The filter parameters, DC bus voltage, and switching/sampling frequency are given in Table I.

TABLE I. SYSTEM PARAMETERS

Inverter	DC bus voltage (Vdc)	180 V
	Switching frequency	6KHz
	Sampling frequency	100 KHz
Filter	Inductor L_F	10mH
	Capacitor C_F	100μF

The reference voltage is set to 60V RMS/50Hz phase to neutral. The inverter output is connected to the local load through LC filter.

Several tests in simulation were conducted to verify the effectiveness and dynamic/static performances of the proposed voltage controller.

Fig. 4 shows the instantaneous output voltage with RMS value, the instantaneous THD value, load current and inverter current under transient condition when the load change.

Fig 4.a: connected load change from no load to inductive load (At $t=6s$, the load rises from 0 to $L=5mH$ and $R=10\Omega$) And Fig 4.b: the DC resistance Load connected to three phase rectifier drops from 30 to 0 Ω)

It is clear from this figure, the voltage output are slightly affected by load transient and after short transient the output voltage restored to steady state.

Fig. 5 shows the waveforms of the filter output voltage with load current for two different load conditions, it can be seen, the three-phase unbalanced and nonlinear load induces obviously an unbalanced and distorted load current respectively. Moreover, even in unbalanced and nonlinear load conditions, the output voltage is kept balanced.

I. CONCLUSION

In this paper, dual loop control structure (current loop and voltage loop) to control output voltage for three phase four wire DG unite with split DC bus topology has been proposed. Dead beat current controller is used in the inner loop, The outer loop is a combination of multi-resonant filter and stat

feedback controllers, to achieve a fast dynamic response to disturbance due to load transient and ensure the rejection of periodic disturbance injected in the output voltage.

The overall controller enables high dynamic, accurate regulation and high quality of the output voltage.

Analysis and studies have been performed on the proposed control technique including the design of the Dead beat current controller and voltage controller and time domain simulation studies in the Matlab/SimulinkTM software environment under various load scenarios. The simulation results conclude that the proposed control technique :

- Provides excellent tracking of three phase output voltage i.e. fast and smooth transient under the load switching.
- Accommodate the nonlinearity, the THD of the output voltage is lower than 1.8 % in the worse case.

All these analyses, simulation have certified the effectiveness of the proposed control solution.

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Fig 4 : From top to the bottom; Three phase output voltages; Three phase Inverter currents; Three phase load currents; RMS output voltages values ; Output voltages THD . (a) : linear load (rises from 0 to $L=5mH$ and $R=10\Omega$) ; (b): three phase rectifier (DC resistance Load of the rectifier drops from 30 to 0 Ω)

Fig 5 : From top to the bottom; Three phase output voltages; Three phase Inverter currents; Three phase load currents (a) :unbalanced load; (b): nonlinear load(three phase rectifier)

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