Reconfigurable Electro-Optical Logic in Silicon Photonic Integrated Circuits

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Abstract: The paper presents a new optical directed logic architecture that is based on a regular array of integrated optical switches. The same circuit can be reconfigured to perform different combinational logic functions. Its application in network routing is discussed.

1. Introduction

Directed logic (DL) is an innovative logic paradigm that minimizes the latency in calculating a complicated logic function by taking advantage of fast and low-loss propagation of light [1]. A DL circuit is formed by an on-chip network of optical switches [2]. The state of each switch is controlled by a digital electrical input logic signal. While it takes a finite amount of time for each switch to respond to a change in its control signal, all of the switches operate simultaneously and their switching delays do not accumulate—in contrast to electronic transistor logic circuits wherein gate delays are cascaded, resulting in large latency. Latencies from optical propagation in the waveguides and the group delay of the optical switches, which do accumulate along the circuit, are much shorter than the gate delay in transistor logic circuits (currently at a level of 5-10 ps).

We will present here a reconfigurable cellular optical DL architecture [3] that is well suited for CMOS-compatible silicon photonics, especially for logic based upon resonant, electro-optical optical switches that employ micro-rings or micro-disks whose resonance mode is shifted by the depletion or injection of carriers [4-6]. The idea is to create large-scale integrated (LSI) reconfigurable optical logic fabrics (an optical equivalent of FPGA) using the small size, fast switching speed and ultra-low power consumption of the micro resonators.

2. Reconfigurable Switch: the Unit Cell

The basic building block of the DL circuit is a reconfigurable switch that can be built based on silicon microring or microdisk resonators. This type of switch has small size, fast switching speed, low power consumption and the capability of large-scale integration.

Fig. 1(a) shows an SEM picture of a typical microring resonator having a radius as small as 1.5 μm side-coupled to a straight waveguide [7]. When the light traveling in the straight waveguide resonates with the microring resonator, light couples from the waveguide to the ring, and the optical transmission in the waveguide reaches a minimum. Thus the transmission spectrum of a microring resonator shows a sharp dip around the resonant wavelength. By tuning the resonant wavelength of the resonator, the transmission of light at a given wavelength λ_L can be changed from high to low, or vice versa, resulting in the *pass* and *block* states we need for a 1×1 switch.

To build a reconfigurable switch, two types of resonance tuning will be used. One is for the switching controlled by the logic signal. The resonance can be tuned with fast speed over 10 Gbit/s by changing the free-carrier density in silicon with an embedded p-i-n junction shown in Fig. 1(b). The refractive index of silicon changes with the carrier density due to the plasma dispersion effect, resulting in the desired resonance tuning. The logic signal applied on the p-i-n junction can tune the resonant wavelength between λ_0 (when the logic signal is '0') and λ_1 (when the logic signal is '1') as shown in Fig. 1(c).

The switch is reconfigured with another control signal that determines the position of λ_0 with respect to the laser wavelength λ_L . When λ_L aligns with λ_1 (see Fig. 1(c)), the switch is in the block/pass mode, i.e. it blocks light when the control logic signal is '1' and passes light when the control logic signal is '0'. When λ_L aligns with λ_0 (see Fig. 1(d)), the switch is in the pass/block mode. When λ_L aligns with neither λ_0 nor λ_1 (see Fig. 1(e)), the switch is in the pass/pass mode. For most applications, the reconfiguration speed can be relatively slow (e.g. from μs to ms), and a slower tuning mechanism based on the thermal-optical effect or micro-mechanical structures can be used.

The insertion loss and group delay of the optical switch at the *pass* state depends on the bandwidth of the ring resonance and the amount of tuning. As an example, if we assume the FWHM width of the ring resonance is 0.33 nm around the telecom wavelength of 1.55 μm and the resonance at the *pass* state is tuned 1 nm away from the laser wavelength, the insertion loss of each switch is only 0.1 dB and the group delay is only 0.17 ps. That means over a hundred switches can be cascaded along the waveguide without incurring impractical loss or latency.

Fig. 1. (a) An SEM picture of a silicon microring resonator. (b) A diagram of an optical switch with a p-i-n junction built across the ring. (c) The transmission spectra of a switch in block/pass mode for light at λ_L . Red line is the spectrum when the logic signal is '1'. Blue line is the spectrum when the logic signal is '0'. (d) The transmission spectra of a switch in pass/block mode. (e) The transmission spectra of a switch in pass/pass mode.

Fig. 2. The truth table and the circuit diagrams of an 8-bit priority encoder. (a) The truth table. 'x' means "any". (b) The directed logic implementation of the encoder. Black lines: optical waveguides; Red lines: electric logic signal controlling the optical switches;

3. Logic Architecture

Any combinational logic function can be written in a sum-of-products format. The sum-of-products expression of a logic function can be mapped onto a two-stage directed-logic circuit shown in Fig. 2(b) where the first stage calculates all the products, and the second stage calculates the sum of the products. Each stage is formed by an array of parallel optical waveguides.

In the first stage, each waveguide passes through an array of identical and reconfigurable optical switches shown in the previous section. Light can pass through the waveguide and give an output signal as TRUE ('1') only when all the switches are in the *pass* state. The optical output of this waveguide thus represents a product (AND) of the logic inputs. When a switch is configured to be in the pass/block mode or the block/pass mode, the product that the waveguide calculates includes respectively the non-inverted or the inverted logic signal that controls the switch.

The second stage is to calculate the sum (OR) function. While the OR function is hard to implement directly, we can take advantage of the relationship between OR and NAND functions: $A + B = \overline{\overline{A} \cdot \overline{B}}$, which converts the sum to a product that can be calculated in the same way as discussed above. In between the two stages, an optic-to-electric (O/E) conversion module converts the optical output of a waveguide in the first stage to an electrical logic signal that is used to control the optical switches in the second stage. The optical outputs of the second stage give the calculated results of the target logic functions. If desired, they can be converted back to electric logic signals by an optional O/E conversion module.

Here we use an 8-bit priority encoder as an example to illustrate how a logic function is mapped onto the proposed directed-logic circuit. Fig. 2(a) shows the truth table of the encoder whose output, a three-bit binary number, is the index of the first (with the highest index) nonzero logic input. Fig. 2(b) shows the directed-logic circuit constructed to perform this function. The black lines represent optical waveguides, while the red lines represent the electrical lines carrying the input (x_i) and output (y_j) logic signals. At each cross point of a red line and a black line, there is a reconfigurable optical switch that either passes or blocks the optical signal.

By comparing Fig. 2(a) and Fig. 2(b), one can see that the circuit is a direct mapping of the truth table to the three operation modes of the switches as follows. (1) The first stage of the logic circuit is mapped from the left side of the truth table. The '1's in the truth table are mapped to switches in the pass/block mode; the '0's are mapped to switches in the block/pass mode; while the 'x's are mapped to switches in the pass/pass mode. (2) The second stage

of the logic circuit is mapped from the right side of the truth table. The ‘1’s are mapped to switches in the pass/pass mode while ‘0’s are mapped to switches in the block/pass mode.

4. Application Example

The strength of the proposed DL circuit lies in its low latency and its reconfigurability. One application that can take full advantage of these characteristics is packet routing in optical interconnection networks. Low latency is extremely important for interconnection networks, especially for an intra-chip interconnection network on a many-core processor. Most of the proposed architectures use static routing algorithms (such as the dimension-order routing in a mesh network) or point-to-point links to avoid the latency caused by the routing function.

In a network with multiple paths between two points, adaptive routing, where paths are chosen based on the anticipated network traffic, can be much more efficient. When a many-core processor is running multiple tasks, we can expect much heavier traffic between cores that are assigned to the same task than that between cores that are running different tasks. The controller that assigns tasks to the cores can use this information to balance the traffic through the network and reduce the possibility of network congestion. To achieve that, each node of the network needs to maintain a routing table that is dynamically updated based on the task distribution. When a packet arrives at the node, the routing decision needs to be made as soon as possible based on the dynamic routing table, and that is where the reconfigurable DL circuit is needed.

To check the routing table, the DL circuit compares the destination address of the packet with each entry of the routing table and the matching entry determines the output port to which the packet will be forwarded. Fig. 3 shows an arbitrary routing table as an example. One can see that a routing table has the same structure as a truth table, and can be directly mapped onto the DL circuit in the way the truth table is mapped in Fig. 2. Given the low latency of the DL circuit, it is possible to make a routing decision within one clock cycle even for a much larger routing table.

Fig. 3. (a) An example of a routing table at a node of an optical interconnection network. (b) The DL circuit that translates the network address to the number of the output port based on the routing table.

5. Conclusion and Discussion

We propose here a cellular optical DL logic architecture that is reconfigurable and scalable. This architecture is built with ultra-compact silicon photonic devices that offer the capability of large-scale integration. This architecture can also be used to build an all-optical logic by replacing the electro-optic switches with all-optic switches. Beside the two-stage architecture shown here, we have also proposed a multi-spectral circuit [3] that does not need the O/E conversion module between the two stages. In the multi-spectral design, the waveguides in the 1st-stage switch fabric carry light with different wavelengths. The optical outputs of 1st-stage waveguides are then coupled to the output waveguide and collected by a broadband detector. The logic output will be ‘1’ if the total received power is above the level expected from a single non-blocked waveguide.

References

- [1] J. Hardy, and J. Shamir, Opt. Express **15**, 150-165 (2007).
- [2] L. Zhang, R. Q. Ji, L. X. Jia, L. Yang, P. Zhou, Y. H. Tian, P. Chen, Y. Y. Lu, Z. Y. Jiang, Y. L. Liu, Q. Fang, and M. B. Yu, Opt. Lett. **35**, 1620-1622 (2010).
- [3] Q. Xu, and R. Soref, Opt. Express **19**, 5244-5259 (2011).
- [4] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, Nature **435**, 325-327 (2005).
- [5] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, Opt. Express **15**, 430-436 (2007).
- [6] P. Dong, R. Shafiiha, S. Liao, H. Liang, N.-N. Feng, D. Feng, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, Opt. Express **18**, 10941-10946 (2010).
- [7] Q. Xu, D. Fattal, and R. G. Beausoleil, Opt. Express **16**, 4309-4315 (2008).