

# Fault Isolation and Reconfiguration in a Three-Zone System

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**Abstract**— This paper provides experimental verification of a fault isolation sequence in a DC Zonal Electrical System. Three electrical zones consisting of phase controlled rectifier interfaces to medium voltage AC distribution, two DC distribution buses and downstream converters, inverters feeding loads are energized and bolted faults are applied to various locations. The Fault Isolation and Reconfiguration approach utilizes no load switches for fault isolation aided by de-energization of the affected buses. Three electromechanical no load switches in a single assembly are utilized at the interface between electrical zones. The instantaneous peak fault currents were captured at each switch and sent to adjacent modules over a Ethernet-based Local Area Network in order to locate and isolate the fault to the nearest bus segment. Experimental results show that in most cases full output capacity was restored autonomously. Loss of communications scenarios are tested showing limited power restoration.

**Keywords**—DC Distribution; Shipboard Power Systems; DC Fault Protection.

## I. INTRODUCTION

Future Navy shipboard electrical systems will be based on the Integrated Power System (IPS) approach in order to provide electric power to the total ship (propulsion and ship service) in an integrated fashion [1], [2]. IPS enables shipboard service loads, i.e. pumps and lighting, to be powered from the same electrical source as pulsed loads and electric propulsion—enabling the optimal use of energy resources. The first consideration for an IPS architecture is survivability during fault events. The main goal of Next Generation IPS (NG-IPS) should be to ensure that non-faulted portions of the system are either unaffected by the fault or can ride through a temporary power interruption while the system autonomously re-configures itself to remove the fault from the system.

Previous work [3] presented a DC Zonal Electrical System (DCZEDS) that responds to a bolted fault by executing an autonomous reconfiguration sequence that isolates the faulted bus segment with motorized no load switches. Three zones of this DCZEDS have subsequently been built and tested. Testing was performed in three different line-ups with faults at six different locations, with and without communications. Other variations were performed, such as partial communications, stuck switch, emergency source fed, and ramping into a fault present on a dead bus. A total of twenty fault events were recorded during the testing. The purpose of this paper is to present the results of this testing. It is hoped that these results will provide some context as the Navy looks forward to NG-IPS with the intention of continuing DCZEDS but at higher

voltages, improved architectures for fault tolerance [4] and injection of new technologies such as fast acting Solid State Protective Devices (SSPDs) [5].

## II. DC ZONAL ELECTRICAL SYSTEM OVERVIEW

A DCZEDS is shipboard IPS that divides the generated downstream DC power into physical zones that can be isolated from each other in order to mitigate damage to un-faulted portions of the system during a vulnerability event [6], [7]. DCZEDS is intended to be a highly survivable system. A notional DCZEDS with a representative low voltage alternating current (LVAC) and low voltage direct current (LVDC) distribution in one electrical zone is shown in Fig. 1. The conventional definition of DCZEDS implies switchgear that can autonomously galvanically isolate one electrical zone from another by opening one or more switches distributed along a port longitudinal bus and starboard longitudinal bus along the length of the ship that can access all physical locations in the ship. The conventional definition of DCZEDS also implies redundant delivery of power from both port and starboard distribution networks within a defined electrical zone. It is assumed that a portion of the loads within the zone will be undisturbed in the event of a loss of power to either port or starboard distribution buses. Each phase controlled rectifier (PCR) and electrical zone is isolatable by motorized no load switches capable of carrying but not interrupting thousands of amperes. These electromechanical switches provide a relatively low cost and low risk method for achieving galvanic isolation between PCRs and a Line to Line (LL) fault anywhere on the bus. However, the methodology depends on the PCRs to interrupt the flow of current, which causes an interruption of power to the LVAC and LVDC distribution downstream of the faulted DC bus while the fault is being isolated. Switch actuation is also quite slow, taking about ten seconds.

Implementation of a switch is described in [3]. It is a motorized switch that disconnects both positive and negative polarities of the DC bus. Each switch requires a bypass contactor to allow for some current to flow when the switch makes or breaks, due to stray load on the DC bus, such as power supplies for the motorized switch and associated controls or inrush current from small mismatches between voltages if energized sections of the electrical bus are connected.

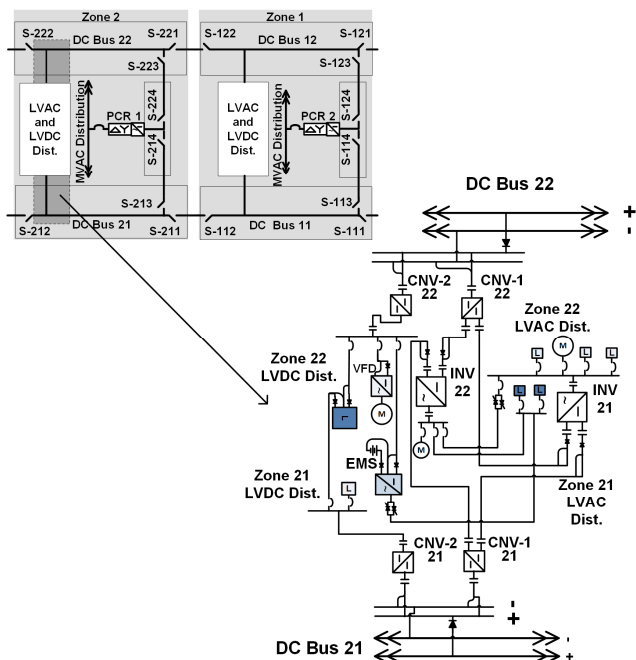


Fig. 1. Notional DCZEDS based IPS with representative zone

There is a two-switch assembly associated with each PCR and a three-switch assembly associated with the port and starboard longitudinal bus in each zone. The bus switch assemblies and PCRs contain local control processors responsible for controlling the opening and closing of the switches and communicating operational status over a Local Area Network (LAN) shared with the switch assemblies, as described in [3].

### III. FIR SEQUENCE OVERVIEW

The IPS executes a Fault Isolation and Reconfiguration (FIR) sequence whenever a LL fault is detected on one of the longitudinal buses. This is an autonomous process that is enabled by the LAN communications between bus switch assemblies and PCRs so that the system acts as a single unit to isolate a fault and recover un-faulted portions of the system to normal operation. When a LL fault occurs on one of the longitudinal buses the redundantly fed loads shown in Fig. 1 do not experience a power interruption during the entire FIR process due to their diode auctioneered inputs. However, due to the length of the FIR execution time, any single fed loads connected to the faulted bus will lose power during the sequence. If the fault occurs on the section of bus feeding an electrical zone then loads that are single fed from the faulted bus section cannot be recovered. Also, to avoid overloading the remaining bus, ship loads may need to be rebalanced so the demand load does not exceed ratings.

As described in [3], the FIR sequence begins with the detection of fault current above a predetermined threshold of 10kA. Each assembly that detects the fault notifies all other assemblies. All connected PCRs immediately inhibit output power. The peak current captured in each switch when the fault occurred is then broadcast to all other connected PCRs and switch assemblies over the LAN. These current measurements

are referred to as “snapshots”, and consist of magnitude and direction from each current sensor in the assembly. Each assembly then gathers the current snapshots of adjacent assemblies and uses an algorithm to determine a course of action. Assemblies determined to be closest to the fault open the appropriate switch(es). After a preset time duration, the PCRs ramp up output voltage, restoring power to unfaulted portions of the longitudinal bus. This timer value is the amount of delay time required to de-energize the buses, actuate the motorized switches to fully opened conditions, and re-energize. The bulk of the time is the switch commutation time. This time must be sufficiently long to ensure that no bus is re-energized while the switch is in transit in order to avoid the possibility of significant equipment damage. The length of time is driven by the fact that the bus segments that must be moved in order to fully isolate the fault are very large due to their high current carrying capability. Further details about the FIR sequence are provided in the following subsections.

### A. Fault Event Capture

The PCRs have large output filter capacitors across the 1kV bus for stability. When a low-impedance fault occurs these capacitors discharge into the fault, producing a current spike on the order of tens of thousands of Amps for a short duration. Each assembly in the current path detects the spike and records the magnitude at peak as well as direction. A measured plot of a typical fault current profile is shown in Fig. 2. A typical snapshot window is superimposed on the transient. The transient peak lasts for 5-10mseconds, depending on the loading of the bus when the fault occurs. For this particular scenario the peak current level is about 22kA, which is well over the peak threshold for detection (10kA). This current snapshot is sent over the LAN so assemblies that did not detect the current spike can participate in the isolation if necessary. An assembly is considered a “participant” in the fault event if it detected the fault itself or if it is connected to an assembly that did. An assembly determines which other assemblies it is connected to by tracing the open/closed states of switches throughout the system. PCRs that detect the fault immediately de-energize, causing a loss of input power on downstream dc-dc converters and inverters. Assemblies that are not participants in the fault event, typically those connected to the opposite Longitudinal Bus, ignore the event and continue producing output power. Auctioneered loads transfer seamlessly to the remaining longitudinal bus and the majority of loads continue without interruption.

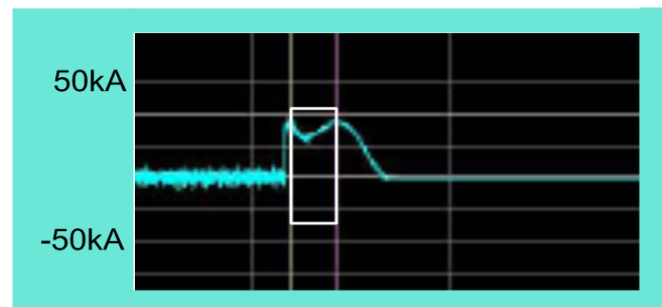


Fig. 2. Measured fault current from full load and snapshot window

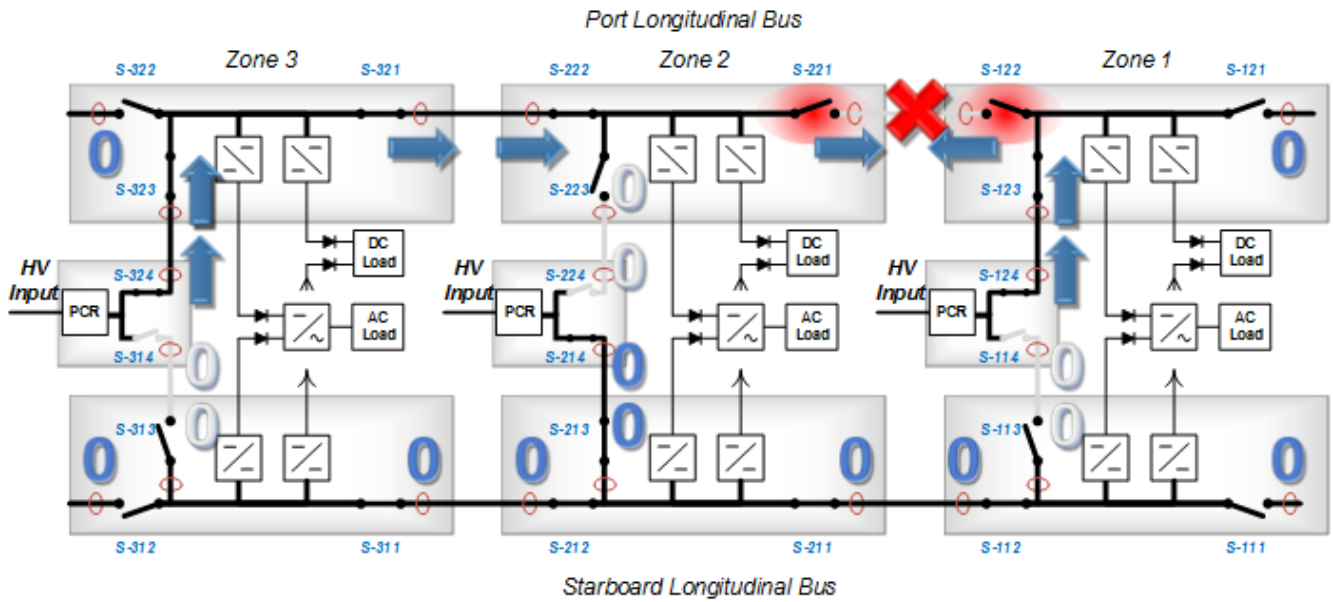


Fig. 3 Example of FIR with Communications

### B. Fault Location Algorithm Execution

Upon FIR detection, each participant assembly waits 0.5s to take snapshots, send them out over the LAN, and gather snapshots from adjacent modules.

Along each longitudinal bus, each three-switch assembly includes a switch that can disconnect aft of the zone, forward of the zone, and into the zone. Each assembly converts the currents from its switches into vectors – either the current is into the assembly, out of the assembly, or zero (did not exceed the threshold). If each assembly has snapshots from adjacent assemblies, the fault location can be reliably determined to the nearest bus segment by following three general rules: 1) If any current vector is into an assembly and no current vectors are out of the assembly, then the fault is internal to the assembly. The assembly isolates itself by opening all of its switches which isolates the bus feed to that zone completely 2) If two vectors out of adjacent assemblies point toward each other, the fault is between the two. Both assemblies open their outgoing switch. 3) If a current vector out of an assembly does not correspond to a vector into the adjacent assembly, the fault is between the two. Both assemblies open the switch closest to the fault.

An example application of the algorithm is shown in Fig. 3. PCRs in zones 1 and 3 supply the port bus and the PCR in zone 2 supplies the starboard bus. The fault is marked with a red X, located between zones 1 and 2 on the port side. The current snapshots are represented in blue, either as an arrow pointing in the direction of current (vector) or a zero. A current spike flows to the fault from zone 1 and zone 3. In zone 3, current into the port switch assembly corresponds to an outgoing current. This does not satisfy any of the three rules, so that switch assembly takes no action. However, both the zone 1 and 2 switch assemblies on the port side see the current vectors pointing at each other, so in accordance with rule #2 both open

their outgoing switch, isolating the fault to the nearest bus segment. The figure shows starboard currents as zero, though they would not be sent out since those assemblies are not participants in the FIR event.

### C. Fault Isolation and Reconfiguration

Using the three rules described above, assemblies that determine a need to open switches do so immediately without notifying other assemblies of the change. The PCRs are inhibited, so no current is flowing through the switches. All participant PCRs re-energize their output 11.5s after detecting the fault. The downstream dc-dc converters, upon receiving input power automatically restore output. The inverters, which are fed by dc-dc converters automatically restore output when their input voltage is restored. The restored dc-dc converters seamlessly pick up half the load through downstream auctioneering diodes according to pre-set voltage droop settings. Only the faulted portion of the port longitudinal bus is isolated. In some cases, such as that shown in Fig. 3, all output power is restored and the system remains at 100% capacity. If the fault is internal to an assembly, or if the fault is between a zone and its only power source(s), then power is restored only to the extent possible given the bus configuration.

Switches that are opened as part of an FIR sequence are placed in an inhibited state, which requires an operator action at the local HMI before re-closure is allowed. This prevents a remote operator or other autonomous sequence from closing the switch into the fault before it can be diagnosed and repaired. Due to the construction of the switches used, they can survive the current spike in the closed state, but the bypass contactors will be severely damaged if the switch is closed into an existing fault while energized on the other side.

If for some reason the fault is still present when a PCR restores output power (degradation in communications between switch assemblies and PCRs), the FIR sequence is repeated a

second time. If the fault is still present after the second attempt, the PCR transitions to a faulted state.

#### D. Loss of Communications

The FIR sequence described above does not rely on a centralized controller to locate and isolate the fault. As a result the same sequence can be used even if assemblies have no communications with each other. The only side effect is that switch assemblies cannot use the three rules to make an ideal location, since they are missing snapshots from adjacent assemblies. They can still use rule 1; if a current vector is ingoing and no vectors are outgoing, the fault is internal and is isolated by opening all switches on that assembly. However, instead of rules 2 and 3, all modules that see current in and current out must assume the fault is just beyond the outgoing switch and isolate the fault by opening the outgoing switch. This potentially results in a larger segment of the longitudinal bus being isolated than if the assemblies had communications.

Fig. 4 shows a fault in the same location and in the same line-up as Fig. 3, but with no communications. The result is that the fault is isolated in the same amount of time, but with a loss of output power from the zone 2 converters on the port side. Without information from zone 2, the zone 3 port switch assembly must assume the fault is between zone 2 and 3 and isolate it. All diode-auctioneering-fed LVAC and LVDC loads remain online throughout the sequence, powered by the starboard side, but in zone 2 only half the power capacity is restored after the FIR sequence is executed.

An additional consequence of having no communications is that PCRs that are connected to the fault but not in the fault path will not reconfigure. For example, in Fig. 4 if the zone 1 PCR had not been online, the fault current would pass through zone 2 and 3, but the zone 1 longitudinal bus connected dc-dc converters would not be aware of the fault, only that input power was lost. As a result, the fault is only partially isolated and system configuration knowledge is limited. However, this consequence is minimal. If the zone 1 PCR is subsequently

energized into the fault, a second FIR sequence would occur only in zone 1, and the resultant state would match Fig. 4.

Another consequence of loss of communications is that the PCR cannot fully isolate the fault on the first attempt; it will always re-energize. This gives the three-switch assemblies the first attempt at isolation. Only if the second FIR attempt results in a current spike does the PCR isolate the fault. This has the impact of doubling the time to isolate a fault between a PCR and downstream switch assemblies.

#### E. Special Case - Energization into a Fault

If a low impedance fault is present on a de-energized bus and a PCR is energized into it, there will not be a current spike (as in Fig. 2) since the capacitors are not charged. Therefore a second detection condition is necessary. The PCR ramps current into the fault until it reaches a predetermined current limit, on the order of a few thousand Amps. It limits to this current by collapsing output voltage. If the PCR or longitudinal bus switch assembly detects a current above this threshold while simultaneously detecting voltage well below nominal, it considers this an FIR event and engages the FIR sequence in the same way as if it had detected a current spike.

### IV. INTEGRATION TESTING

Integration testing was performed on a three-zone system. The first problem to be solved was the FIR sequence timing, which is dependent on the time it takes the switches to open. This in turn is dependent on the time it takes the bypass contactors to close, the motor to open the main contactors, the bypass contactors to open, and the time it takes to sense these position changes. It was found that if the mechanical alignment of the motor shaft was slightly off, it could add a few seconds to the open time, which caused the FIR sequence to abort. To solve this problem, diagnostic software logged all these transition times to determine the average and the amount of variance.

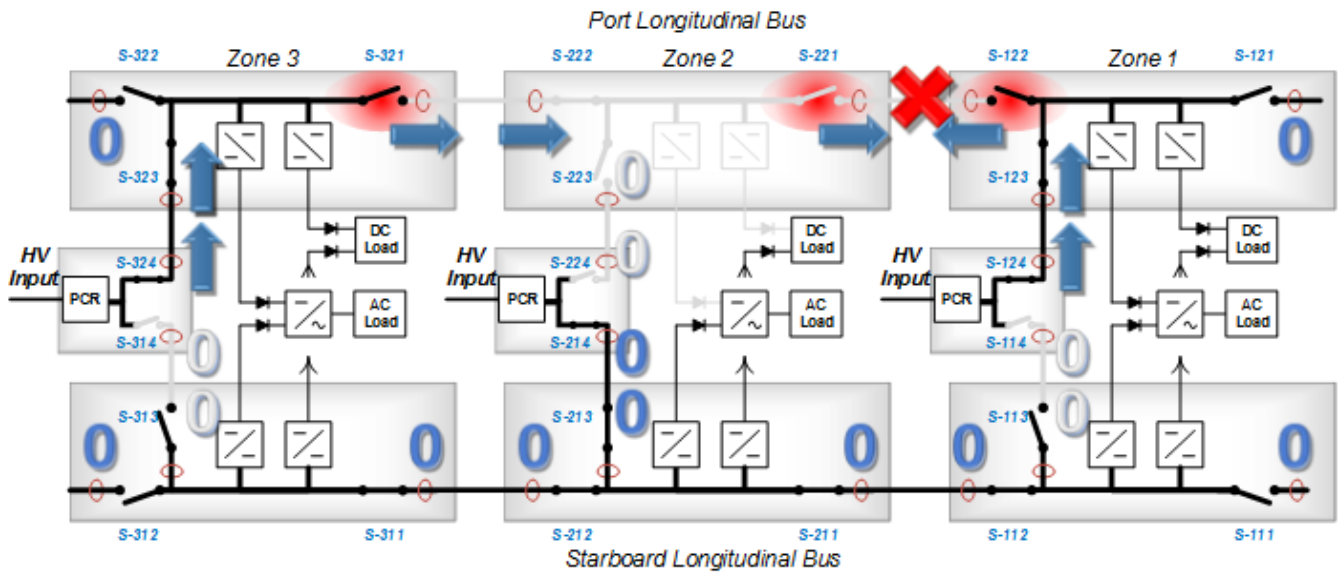


Fig. 4 Example of FIR without Communications

Additional margin was added for motors slowing over their lifetime and to account for small amounts of misalignment. The *FIR Restart Timer* provides adequate margin for all switches to reach their commanded state before being re-energized.

Bolted faults were applied with a test fixture that consists of a circuit breaker in a plexiglass housing with a remote pendant. The circuit breaker is rated for 1kVdc, 3200A and is capable of closing and latching into 100kA. The faults were applied at several different locations and in three different longitudinal configurations, shown in Fig. 5 as red X's.

All fault scenarios were tested twice; once with communications and once without. In the first test (labeled 1 in Fig. 5), a single PCR was feeding the bus and the fault was applied between the PCR and the first switch assembly. In this case, no portion of the longitudinal bus was able to be restored, but the sequence itself and the timing were demonstrated. The next test (2 in Fig. 5) verified that the portion of the Longitudinal Bus between the fault and the PCR could be restored, but portions of the bus downstream of the fault could not. Test lineup 2 demonstrated that with two PCR's in parallel, any fault between longitudinal bus switch assemblies (4,6) or between longitudinal bus switch assemblies and a PCR (3) can be isolated to the nearest bus segment, and all output power restored. In one case, the fault was applied internal to a dc-dc converter (4). The FIR sequence isolated the fault and both adjacent zones were restored.

Several test cases were performed with the fault applied before energizing the bus in order to demonstrate the special functionality described in Section III (E). The first fault was located between switch assemblies (2). The conditions that triggered the event were different, but the FIR sequence was identical to the case in which the bus was energized before applying the fault. The second fault was located on the crosstie bus between a PCR and a switch assembly (7). The system isolated the fault in zone 3 and restored all three zones from the PCR in zone 2.

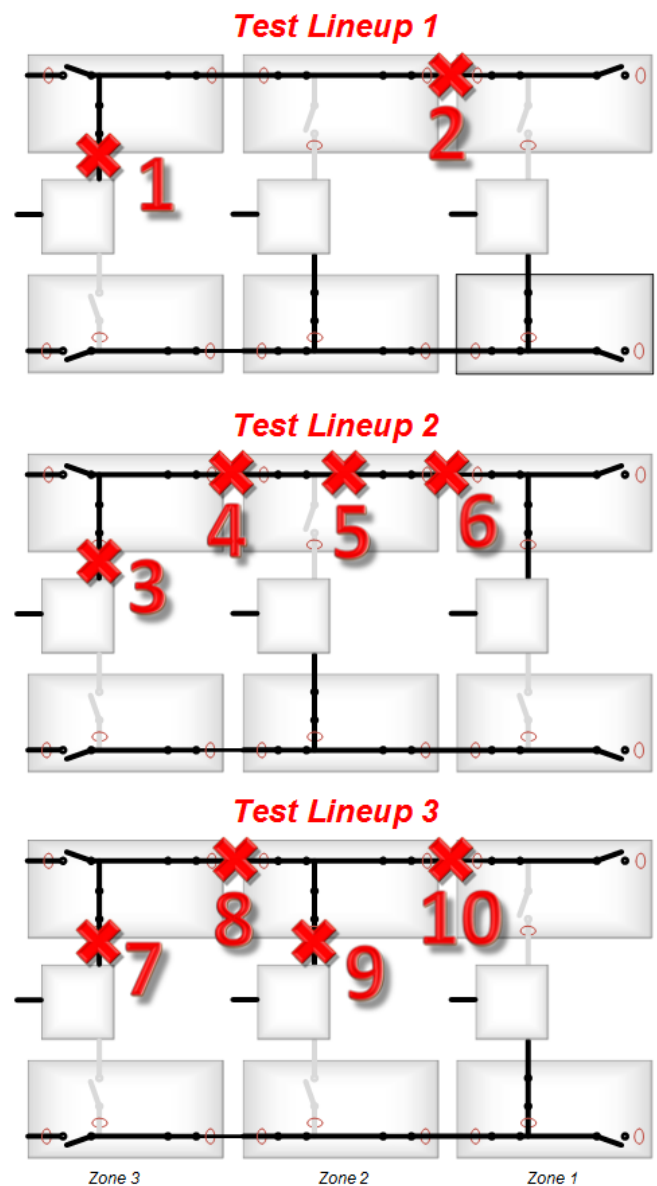


Fig. 5 Test Lineups and Fault Locations



In order to record the timing of the sequence as seen by a single fed AC load, a test was performed with the starboard side de-energized and a fault applied to the port side. The resultant voltages on the port side are shown in Fig. 6. The port bus (yellow trace) was de-energized for about 12s during the sequence. Single fed DC loads and inverters on the port side (green trace) lost input power for about 23s. Single fed inverters on the faulted side restored AC output power (blue trace) at about 30s.

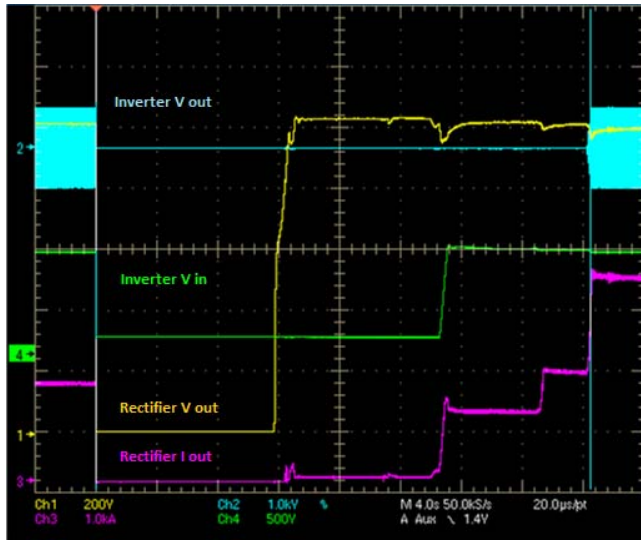


Fig. 6 Restoration Timing Measurements

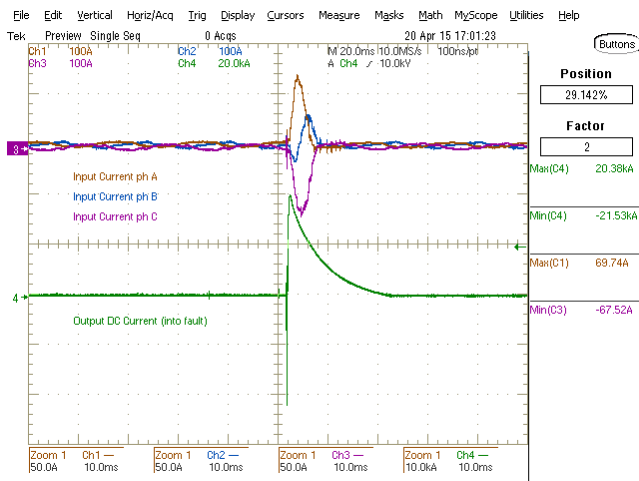


Fig. 7 Measured currents during application of the fault on the PCR input (top) and at the PCR 1kV bus output (bottom)

The fault currents were measured during sudden application of a bolted line to line fault on the output of an unloaded PCR and the results are shown in Fig. 7. These results show that some of the impact of the fault is seen on the 4160Vac input currents, so fault behavior on the 1kVdc bus is not completely decoupled from the input 4160Vac bus. However, the 4160Vac bus current transient lasts less than a full cycle and the surge current peaks are well below the continuous rating. On the 1kV bus the fault current peaks at 20.4kA and the transient lasts less than 10mseconds. It is expected that the peak currents will be slightly higher and last a little longer if the fault is applied to a loaded bus (see Fig. 2).

## V. CONCLUSIONS

A DCZEDS has been built and tested that is capable of surviving a fault anywhere on a longitudinal bus, autonomously isolating the fault, and restoring power to all bus segments possible given the lineup and communications status. This allows no load switches to be used in an IPS, combining the cost and weight advantages of no load switches with the many performance advantages of the IPS. The test verified that FIR maximizes survivability during a longitudinal fault, with no impact to dual-fed loads, and with no operator intervention.

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