A Hardware-in-the-loop Testbed for Distributed Energy Generation Penetration Analysis

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Abstract— This paper presents a real-time hardware-in-the-loop testbed to analyze the impact of distributed generations distribution level system. The IEEE 15-bus node distribution feeder has been developed in MATLAB and is connected to two real time inverter based distributed generators through the dSPACE hardware interface. The power flow outputs of the inverters are controlled by local decentralized TI C2000 modular microprocessor boards. The proposed hardware setup is designed so that it can easily be modified to a new distribution system infrastructure without making any changes in the hardware setup. The results of power flow control for distribution level lines, power loss reduction and voltage profile improvements as well as reactive power compensation from the actual distributed generators are compared for the different level of penetrations. The experimental results are compared with the simulation results to verify the accuracy and effectiveness of the decentralized controller on the proposed test bed.

Index Terms-- *Distributed Generation, Inverter, Real-time control, Communication, Coordinated Control*

I. INTRODUCTION

Future power system control and stability need to be revisited due to the high penetration level of non-traditional green electricity generation such as solar and wind. The inherent variability and uncertainty of such renewable electricity production is one key contemporary challenges for electric power grids, especially to power system stability. Microgrids [1] specifically in distribution levels are future electric power system infrastructures. Microgrids are using advanced monitoring and control technologies in order to overcome issues and challenges resulting in a safe, green, reliable and secure power grid.

Microgrids operate in either islanded or grid-connected mode. The balance between generation and demand must be maintained in order to ensure the voltage and frequency stability. To achieve this goal, each distributed generator DG inverter must be controlled in coordination

with other generating units in low voltage power networks [1]. Also, in distribution lines R/X ratio is not negligible and the effect of R must be included in power flow control equations [2], [3].

Reduction on transmission lines and improving voltage stability can be achieved through supplying power from end users at the end of the line side. Therefore, Inverter based DGs are going to play a significant role in future of electric power system because of their rapid output response to any change in comparison to rotating machine based DGs.

There has been significant number of research on control and operation of microgrids in literature. The decentralized as well as centralized control schemes have been proposed and simulated for inverters connected to distribution lines [4]-[7]. Moreover, it is expected that new generation of inverters called “smart inverters” to contribute not only in active power but also capable of providing reactive power control.

This paper presents a development of a real time hardware-in-the-loop (HIL) system to validate the simulation results using the obtained experimental ones. The proposed hardware is designed so that it can easily be modified to a new microgrid topology.

In this work, an 11 kV IEEE 15-bus node distribution feeder [8], [9] is used for different penetration levels. The proposed hardware is using dSPACE hardware interface [10] which makes is more cost effective in comparison to available real time simulators. A HIL approach is used to integrate two voltage source inverters, controlled by their local TI microprocessors, to the simulator.

This system has been tested for various case studies in which grid-connected inverters contribute to both active and reactive power output generation.

II. IEEE 15 BUS NODE FEEDER

The authors proposed a power flow control method in [6] for a grid-connected inverter which operates in distribution

level system where R/X ratio of line is much greater comparison to the one in a transmission line. The proposed method was implemented on a real time portable T1 digital signal controller and was tested for one voltage source inverter connected to infinite bus on a small scale test bed [7]. The active and reactive power flow controller operation was implemented successfully on single inverter connected to grid.

Figure 1 shows the IEEE 15 Bus node feeder [8] developed in MATLAB Simpowersystem toolbox [11], [12].

Figure 1. IEEE 15 bus distribution feeder developed in MATLAB Simpowersystem Toolbox

The load flow results for this distribution system is shown in Fig. 2.

Figure 2. Voltage profile for IEEE 15-bus distribution network

Where the total active and reactive substation output power are $P = 1.18$ MW and $Q = 1.20$ MVar, respectively.

The model has been simulated for three case studies as follows:

A. Case 1: DG1 is connected to Bus #8

DG1 which is an inverter based distributed generator provides 440 kW and 40 kVar at 11 kV.

B. Case 2: DG2 is connected Bus #5

DG1 which is an inverter based distributed generator provides 330 kW and 60 kVar at 11 kV.

C. Case 3: DG1 and DG2 are connected to bus #8 and #5, respectively

Both DG1 and DG2 are feeding power to buses 8 and 5. The load voltage profile for different case studies are plotted in Fig. 4.

Figure 3. IEEE bus distribution feeder with DGs on buses 5 and 8

The voltage profile for three case studies is depicted in Fig. 4.

Figure 4. Voltage distribution profile for case studies

III. HARDWARE IMPLEMENTATION

The system hardware consists of three major blocks: 1) The inverters 2) The inverters' controller, and 3) The Grid Model and Measurement devices, as depicted in Fig. 5. The following three subsections explain the details of each block.

A. Inverters

The inverters used in this experiment are part of the Lab-Volt™ workbench at the Renewable Energy Lab at the WVU Tech. These are inverters with 4 kW rating that are used in single phase mode; their IGBT firing signals are provided by the controller block. Each inverter has its own dedicated controller block, as depicted in Fig. 5.

Fig. 5. System Hardware Block Diagram

B. Inverter Controller

Each inverter is being controlled by a TMS320F28335-based Texas Instrument (TI) development board [15] that implements the P-Q control algorithm proposed and presented by the authors in [7]. The algorithm uses the inverter's output voltage and grid voltage difference to control the active power (P) and the angle between these two to control the reactive power (Q). The desired values for the P and Q are set by the user in the Grid Model and Measurement block (See subsection III.D.2) through a user interface. These values, along with the grid and inverter voltages as well as the inverter and load currents are sent from the Grid Model and Measurement block to the Inverter Controller block via a dedicated SPI communication channel. The received voltage and current values are processed by the controller to calculate the actual inverter active and reactive power, which are then used in the algorithm to adjust E (the inverter's output voltage) and δ (the angle between the inverter voltage and the grid voltage phasors).

C. Grid Model and Measurements

The IEEE 15-bus node distribution network is used in this experiment. The network and the measurement devices are all implemented in software using Matlab and Simulink which they are implemented on a dSPACE DS1104 system. The 15-node distribution network model is shown in Fig. 7. As it is indicated on the figure, each node in the model is connected to its neighboring nodes by the equivalent line resistance and inductance. Also, each node has its own local load, as depicted in Fig. 6. The overall model used for running the experiment is shown in Fig. 7. As highlighted on this figure, the model can be divided into 7 major blocks their details will be explained in the following sub-sections.

Fig. 6. IEEE 15-Node distribution network model

Fig. 7. Simulink Model of the System

1) Inverters Power Interface

The blocks labeled A and B in Fig. 7, represent the inverters power interfacing sections of the model. Notice that each inverter has a local load which is connected to an isolating transformer. The primary of the transformer is fed by the actual analog signal received from the corresponding inverter. For more accurate modeling of the inverter and its behavior under various loads, the LCL filter implemented in hardware is re-inserted in the primary of the isolating transformer as shown in Fig. 8. Each inverter is isolated from the grid by an electronic switch that activated by the control mechanism after the synchronization step. If it is required by the settings in the control panel (the inverter can be synchronized but still perform in the islanding mode but while it is ready for coupling to the grid any moment that it is required).

Fig. 8. Inverters Power Interface Section (Shown for one inverter only; Block A on Fig. 7)

2) Distribution Model, Grid, and Measurement Devices

Fig. 9 shows the 15-bus node distribution network model augmented with the measurement devices used at each node for monitoring purposes (Block C in Fig. 7). As shown in the figure the voltage and current (to the local load) at each node is measured. As it will be explained later, these information will be used for monitoring of the node load voltage and current waveforms and/or amplitudes and phases. This is also to calculate the exact amount of active (P) and reactive (Q) power transferred to each node load. Notice that as shown in Fig 9, on this experiment, node 1 of the distrubution model is fed by the grid voltage and nodes 8 and 5 by Inverter 1 and Inverter 2, respectively. It is important to mention that the grid supply voltage is modeled in software and its waveform, frequency, and amplitude are accurately set by this approach, as shown in Fig. 10.

Fig 9. Distribution Model and the Measurement Devices (Block C on Fig. 7)

Fig. 10. Grid supply voltage model (Block D on Fig. 2)

C.3) Synchronization Blocks

Fig. 11 shows the synchronization blocks used for grid-inverter synchronization. The details of these blocks have been presented by [6] and [7].

Fig. 11. SynchronizationbBlocks (Block E on Fig. 7)

C.4) ADC, DAC, and SPI interfaces

The ADC block of the dSPACE system is used to read-in the analog voltages produced by the inverters (attenuated versions of the voltages in the range of 0-3V). The digitally converted values are used by the model for synchronization with the grid as well as active (P) and reactive (Q) power calculations. The DAC block of the dSPACE system is used to send the grid voltage and the load currents to the Microcontroller boards used for synchronization and P and Q control (The details of these boards and the algorithms are provided in [6] and [7]). One dedicated connection is used for the transfer of each quantity to the ADC block and from the DAC block to the microcontroller board. The SPI block is used to communicate the desired P and Q values from the controller window to the microcontroller boards. Since these values are transferred in digital format a single serial bus is used for both microcontrollers. A total of 4 lines are required by SPI bus to run form the dSPACE station to the both controller boards. Fig. 12 shows the details of the communication block.

Fig. 12. Communications Block (Block F on Fig. 7)

C.5) Power Measurement Blocks

There are two power measurement blocks in the model as depicted in Fig. 7 which is expanded in Fig. 13. One is used for the measuremnt of the power supplied by the Grid and Inverters along with the powers consumed in the local loads of each inverter and the other is used for the power measurement of the nodes for the 15-bus node model.

Fig. 13. Power Measurement Block (Block G on Fig. 2)

The model that calculates P and Q for each node is shown in Fig. 14. It uses a discrete active and reactive power block that uses the measured instantaneous voltage and current (to the load) of a node to calculate P and Q. The block uses discrete Fourier Transform to calculate the amplitude and phase of both V and I and from there the values of P and Q, which are then averaged over time and are reported at the outputs of the block.

Fig. 14. Model for P and Q measurement for each Node

All the parameters measured and/or calculated in this model will be available to the main control panel for display and control purposes as will be explained in the next section.

D. Control Panel

The control panel of the system is designed using dSPACE “Control Desk Developer” utility which consists of three major windows that will be briefly introduced in the following sub-sections.

1) Waveform Monitor Window

As depicted in Fig. 15, this window displays the waveforms of the voltages and currents for the Inverters and the Grid. The status of the grid and Inverters can be observed on this window and any anomaly in their operation that affects their waveforms can be detected by examining their waveforms.

Fig. 15. Waveform Monitor Window

2) Inverter Monitor and Control Window

This window implements the main control blocks for each inverter. In addition, it provides display sections for continuous monitoring of inverters’ voltage waveforms and their relationship with respect to the grid voltage waveform (amplitude, phase, ...). The top plotters of the window keep track of the synchronization process of each inverter with the grid and the lower panels monitor the power, voltage, current, and phase of each Inverter and the grid. Also, the setting of desired P and Q for each inverter is performed on this panel

which will eventually be transmitted to the microcontroller boards via the SPI bus when it is desired. This window is shown in Fig. 16.

Fig. 16. Inverter Monitor and control Window

On the top center portion of this window there is a waveform window that can be used to monitor any individual node voltage and compare it against the grid or any of the inverter’s voltage.

3) Node Power Monitor Window

The third window consists of a pair of digital display tools that provide the instantaneous P and Q for each of the fourteen nodes of the distribution network (Node 1 is connected to the grid and has no local load connected to it in the standard model and has no display panel on this window). Fig. 17 displays a shot of the Node Power Monitor Window.

P_N2 (KW)	Q_N2 (KVAR)	P_N9 (KW)	Q_N9 (KVAR)
43.7	40.1	68.9	63.2
P_N3 (KW)	Q_N3 (KVAR)	P_N10 (KW)	Q_N10 (KVAR)
67.5	61.9	43.3	39.8
P_N4 (KW)	Q_N4 (KVAR)	P_N11 (KW)	Q_N11 (KVAR)
133.5	122.5	133.2	122.3
P_N5 (KW)	Q_N5 (KVAR)	P_N12 (KW)	Q_N12 (KVAR)
42.0	38.5	66.1	60.7
P_N6 (KW)	Q_N6 (KVAR)	P_N13 (KW)	Q_N13 (KVAR)
135.3	124.2	41.5	38.1
P_N7 (KW)	Q_N7 (KVAR)	P_N14 (KW)	Q_N14 (KVAR)
134.7	123.6	66.4	61.0
P_N8 (KW)	Q_N8 (KVAR)	P_N15 (KW)	Q_N15 (KVAR)
67.5	61.9	132.9	121.9

Fig. 17. Node Power Monitor Window

IV. COMPARISON RESULTS

The simulation and experimental results are provided in Table 1.

The PGrid and Qgrid are active and reactive power outputs from Grid. As shown in Table 1. The simulation and experimental obtained data are very similar for all three case

studies. The voltage profile data as well as power flow of the lines showed similar behavior as illustrated in Fig. 18.

Table 1. Comparison between experimental and simulation results

Case #	Experimental	Experimental	Simulation	Simulation
P/Q	PGrid	QGrid	PGrid	QGrid
No DG	1.24	1.13	1.18	1.20
Case 1	.88	1.089	0.79	1.17
Case 2	.96	1.09	0.91	1.15
Case 3	.60	1.06	0.51	1.13

Fig. 18. Voltage profile of experimental results for all case studies

V. CONCLUSION

This paper proposed a real-time hardware-in-the-loop testbed to analyze the impact of distributed generations on distribution level system where R/X ratio is not small. The IEEE 15-bus node distribution feeder has been developed in MATLAB and is connected to two real time inverter based distributed generators through the dSPACE hardware interface. The power flow outputs of the inverters are controlled by local decentralized TI C2000 modular microprocessor boards. The proposed hardware setup is designed so that it can easily be modified to a new distribution system infrastructure without making any changes in the hardware setup. The results of power flow control for distribution level lines, power loss reduction and voltage profile improvements are compared for the different case studies. The experimental results are compared with the simulation results to verify the accuracy and effectiveness of the proposed method.

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