

A Compact 100-A, 850-V, Silicon Carbide Solid-State DC Circuit Breaker

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Abstract—A 100-A, 850-V, solid-state circuit breaker (SSCB) having silicon carbide transistors and diodes was developed. The SSCB conducts 100 A continuously with air cooling in a 32 square-centimeter footprint. It is normally off and unidirectionally blocking, and has a configurable trip response allowing a range of overcurrent transients to be conducted, while maintaining a fast trip response at its fault-current limit. The SSCB also provides remote trip, status output, and reset functions. The time-versus-current trip response of the SSCB was characterized at 25, 50, and 75 degrees Celsius baseplate temperatures using pulsed currents with ramp rates of over 70 amps per microsecond. Saw-tooth-shaped current pulse widths of less than 5 microseconds, with amplitudes of greater than 200 A, were demonstrated.

Keywords—silicon carbide; circuit breaker; solid-state; avalanche breakdown

I. INTRODUCTION

A compact 100-A, 850-V, solid-state circuit breaker (SSCB), having silicon carbide (SiC) transistors and diodes, was developed. The SSCB provides advantages over electromechanical switches in transition speed, reduced degradation, and longer operating life [1] [2]. It can also be more tolerant of shock and vibration. These benefits enable improved performance in a wide range of applications, especially those on mobile platforms. The SSCB is normally-off and unidirectionally blocking, specifically for DC applications. It has low conduction losses that enable it to be used in applications with air cooling. Additionally, the SSCB analog controller was designed with a configurable trip response to allow a range of overcurrent (between the SSCB continuous rating and the fault interrupt rating) transients to be conducted, while maintaining a fast response at its fault-current limit. The SSCB also has remote trip, status output, and reset capabilities. Switched test circuits were built to provide pulsed SSCB currents of over 200-A peak, with slew rates of over 70 A/ μ s. The trip response of the SSCB was characterized from current pulses ranging from less than 5- μ s wide to the SSCB continuous current rating.

II. DEVICES AND TOPOLOGY

The SSCB was designed for third-generation, 1200-V blocking, 4.04-mm by 6.44-mm, SiC MOSFET engineering samples fabricated by Cree, Inc. Fig. 1 shows typical output characteristics for a packaged MOSFET at 28 °C and 150 °C,

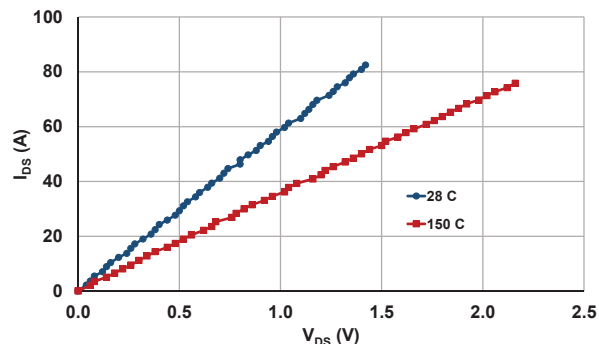


Fig. 1. Typical 4.04 × 6.44-mm third-generation SiC MOSFET forward conduction for $V_{GS} = 20$ V

at a 20-V gate bias. At 28 °C, and 59 A, the MOSFET on-state resistance is 17 m Ω . SiC avalanche breakdown diodes (ABDs) were integrated into the module, in parallel with the MOSFETs, for transient voltage suppression during MOSFET turn-off transitions [3]. The ABDs, having a nominal avalanche voltage of 950 V, provide sufficient margin for SSCB blocking-voltages up to 850 V, while also clamping well below the 1200-V rated MOSFET blocking-voltage. SiC 1200-V Schottky diodes (SDs) were connected anti-parallel to the MOSFETs, and additional SDs were connected in series with the MOSFET switch, with their anode at a separate terminal to provide an optional free-wheeling load-side current path. Fig. 2 shows a simplified schematic of the SSCB module in an application circuit with a load (R), and source-side (LS) and load-side (LL) line inductances.

The SSCB topology is very similar to that presented in [4] and requires an isolated power supply for MOSFET gate control. However, it can provide both high-speed fault-current protection and protection from overcurrent. Although self-powered SSCBs, as presented in [5], can interrupt short circuit

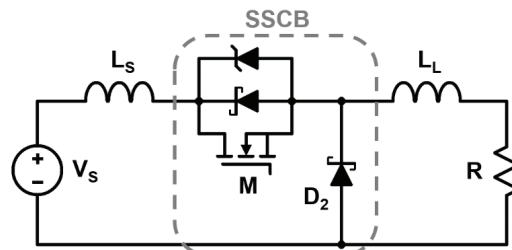


Fig. 2. Simplified schematic of the SSCB module in an application circuit

currents, they can require 4 to 5 volts across the SSCB for operation. This results in either no ability to interrupt overcurrent, or high SSCB conduction losses.

III. POWER MODULE DESIGN

The SSCB footprint area was chosen to approximate that of the GIGAVAC GX14 mechanical contactor. From the manufacturer datasheet, at 200 A, the GX14 is rated for about 25,000 switching cycles at 600 V, and about 800 switching cycles at 800 V. Its maximum release time is 12 ms and its typical operate time is 13 ms, including its maximum bounce time of 7 ms. The footprint of its body (excluding terminals) is 33.4 cm². A 32.0 cm² (6.4 cm x 5.0 cm) baseplate was designed for the SSCB module to have three MOSFET die, four 0.09-cm² SD die, and two 0.12-cm² ABD die. A 75% molybdenum, 25% copper, metal composite was selected for the baseplate for stress reduction. Fig. 3. shows the power-module layout. From left to right, the top row of die consists of an SD, MOSFET, ABD, MOSFET, ABD, MOSFET, and SD die. The second row consists of 2 SD die.

Results of a thermal simulation with the module mounted to a heatsink and a small blower are shown in Fig. 4. The simulation was run to thermal equilibrium with no convection at the top surfaces of the die, substrate, baseplate, and terminals, to approximate the effect of dielectric encapsulation. A flow rate of 2.8 CFM of 50 °C ambient air was modeled through the blower. The peak MOSFET temperature is 150 °C, with 23 W of dissipation per MOSFET. Based on the data shown in Fig. 1, 23 W of dissipation corresponds to approximately 29 A per die, and 87 A of module current.

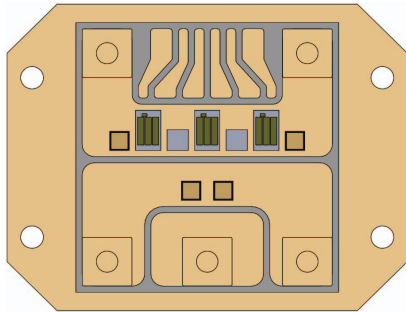


Fig. 3. SiC SSCB module layout with 6.4 × 5.0-cm baseplate

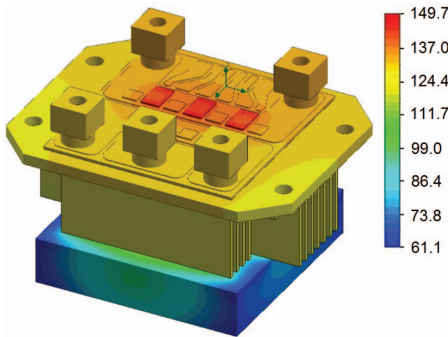


Fig. 4. Simulated thermal image of the SSCB power module, heatsink, and blower, conducting a steady state current of 87 A with 50 °C air at 2.8 CFM with no topside convection

The module was solder bonded in a vacuum furnace, wire bonded, and packaged. Fig. 5 shows the well-matched on-state curves for each of the 3 MOSFETs at room temperature at a 20-V gate bias. The off-state leakage current of the parallel combination of the 3 MOSFETs, 2 SDs, and 2 ABDs was low at 14 μA at 950 V, and ABD breakdown occurred at 956 V.

IV. CONTROLLER DESIGN

For small size, fast response, and noise immunity, the voltage across the MOSFETs was sensed, instead of the conducted current, to determine a trip condition. To sense voltage across the MOSFETs during conduction and to protect the sensing circuitry from high voltage during MOSFET blocking, a low-current-rated SiC 1200-V MOSFET was used as a sense MOSFET in series with a sense resistor. Fig. 6 shows a simplified schematic of the controller. The same gate drive signal (DRV) is used for the power MOSFETs and the sense MOSFET (M_1). However, the source of M_1 connects to the sense resistor (R_3). A sense-resistor value of 49.9 Ω was selected to limit noise at the controller input. The on-state resistance of the sense MOSFET is nominally 280 mΩ at 25 °C. Therefore, approximately 99.5% of the voltage across the power MOSFETs is dropped across the sense resistor when M_1 is conducting. The sensed voltage across R_3 is input to an inverting amplifier (OPA). The amplifier output charges capacitor C_1 through resistors R_{11} and R_3 (with $R_{11} \gg R_3$). Capacitor C_1 integrates the amplifier output voltage. The sum of the voltages across C_1 and R_3 is applied to the inverting input of a comparator (CMP). Therefore, the sensed voltage is provided to the comparator, with the voltage across C_1 adding to it during its charging time. This allows the SSCB to have a configurable high-speed trip point for high sensed voltages,

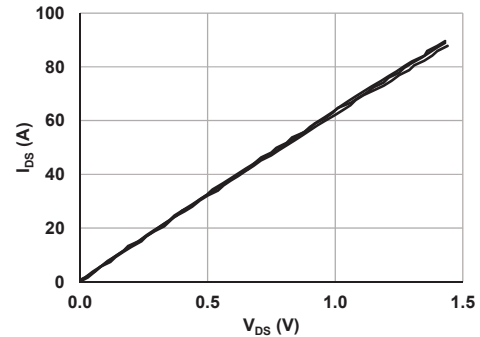


Fig. 5. Individual forward-conduction curves of the 3 SSCB MOSFETs at room temperature and $V_{GS} = 20$ V

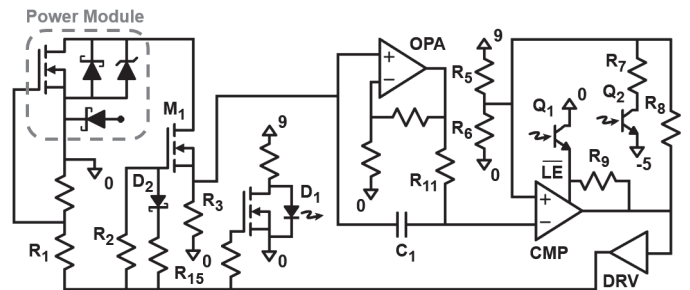


Fig. 6. Simplified schematic of the SSCB control circuit

and a configurable trend of trip levels over ranges of sensed voltage and time duration. The comparator has a latching output that drives the MOSFET gate driver to control the state of the SSCB and M_1 . The status output, reset, and external trigger signals are isolated by optocouplers represented by D_1 , Q_1 , and Q_2 , respectively.

During normal operation, with the SSCB conducting, the sensed voltage and amplifier output voltage are below the reference voltage set by resistors R_5 and R_6 at the non-inverting input of the comparator. Thus, the comparator provides a high output to the gate driver to maintain MOSFET conduction. The comparator's active-low latch enable (LE') pin is pulled up by R_9 to disable the latch and allow the comparator output state to change based on its inputs. When voltage at the inverting input of the comparator exceeds the reference voltage, the comparator output becomes low and pulls LE' low to latch the output. The gate driver turns off the MOSFETs to trip the circuit breaker. To reset the latch and turn the SSCB on, optocoupler transistor Q_1 is turned on to pull the LE' up to 0 V from the comparator negative supply voltage of -5 V. Resistor R_8 provides feedback for comparator hysteresis. The SSCB can be tripped using an external signal by turning on optocoupler transistor Q_2 to pull the comparator voltage reference low through R_7 . By pulling the reference toward -5 V, the SSCB can be externally tripped even at a sensed voltage of 0 V.

To prevent high-current pulses from flowing through the sense MOSFET and sense resistor during SSCB trip and reset transitions, an alternate gate turn-off path is provided by diode D_2 and gate resistor R_{15} . Resistors R_1 , R_2 , and R_{15} were selected so that sense MOSFET M_1 turns off a short time before the power MOSFETs during an SSCB trip, and M_1 turns on a short time after the power MOSFETs during a reset.

A trip current of 210 A was selected for the high-speed trip response, to allow 70 A peak per MOSFET at 28 °C, and to stay close to the repetitive-pulse capability of the two ABDs. From the MOSFET data of Fig. 1, 70 A at 28 °C, corresponds to 1.20 V. The comparator reference was set at 1.19 V. The steady-state trip point was selected to be 93 A based on the 150 °C curve in Fig. 1. This operating point corresponds to 31 A per MOSFET and a drain-to-source voltage of 0.87 V. With the amplifier gain set to 1.37, an output of 1.19 V results for a sensed voltage of 0.87 V. At voltages below 0.87 V, the controller will not trip the SSCB. At voltages between 0.87 V and 1.19 V, the SSCB response time is determined by the amplifier gain and the integrator at the amplifier output.

The plot in Fig. 7 shows simulated controller trip time versus sensed-voltage amplitude. The curve was plotted using voltage amplitudes between 0.88 V and 1.19 V. The curve has vertical asymptotes at about 0.87 V and about 1.19 V, corresponding to the steady-state and high-speed SSCB trip points, respectively. The middle part of the curve can be raised or lowered by changing the integrator and amplifier gain. The upper left and middle parts of the curve look similar to the trip-time versus current characteristics of many mechanical circuit breakers and fuses. However, as seen at the right side of the curve, the controller response does not follow a constant I^2t profile, and can provide very fast trip times near the 1.19-V limit. Yet, in implementation, as the SSCB controller and

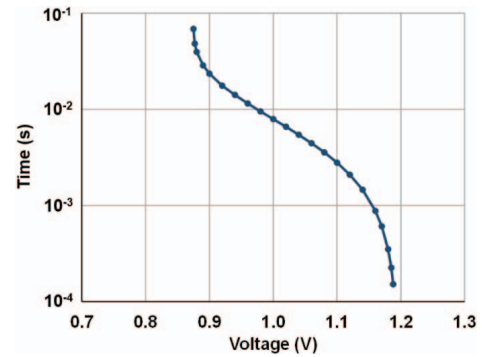


Fig. 7. Simulated controller trip-time versus sensed-voltage amplitude

power stage reaches its fastest trip response, the bottom of the curve will begin to turn toward the right and become horizontal with a constant minimum trip time for all sensed voltages.

The controller circuit board was mounted on the packaged power module. Two flat copper busbars provided SSCB drain and source terminals. The connection from the sense-MOSFET drain to the power module was made by a trace on the control board to one of the drain mounting holes. The module gate and source pins were soldered into the controller. Fig. 8 shows the assembled SSCB, heatsink, and forced-air cooler.

V. PULSED CURRENT TEST CIRCUITS

For SSCB response times on the order of 100 ms, the 5-ms rise time of a high-current power supply provided nearly-square current pulses without overshoot. With the SSCB in the on-state, and the supply connected directly to it, the supply output was enabled to produce each long current pulse. For shorter SSCB response times, the output of the power supply was initially enabled and the SSCB was reset from the off-state to initiate a current pulse. However, interactions between SSCB turn-on, sensing, and turn-off provided a different trip response than that from the SSCB on-state. Therefore, pulsed currents were switched-on externally to the SSCB to characterize its trip response from the on-state. The diodes providing an optional free-wheeling load-side current path were not connected during testing, as a load was not present and line inductance was only added to the supply-side of the SSCB to provide worst-case turn-off transients.

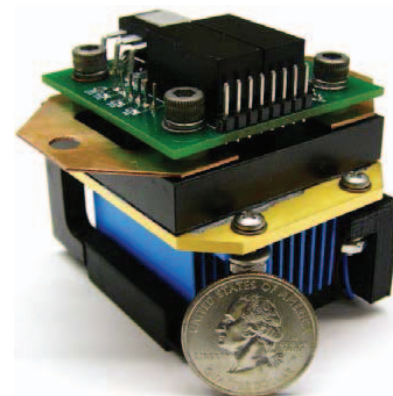


Fig. 8. SSCB module with compact forced-air cooler

Two pulsed-current test circuits were used to characterize the SSCB trip response. Sufficient delays between pulses allowed the SSCB to return to its initial temperature before the next pulse. Ideally, it was desired to obtain trip response times as the pulse duration at a constant current amplitude. However, providing nearly-square current pulses with amplitudes over 200 A for trip response times below 5 μ s, required ramp rates of over 100 A/ μ s. Sourcing such current pulses over a range of amplitudes without overshoot is difficult and can require several multistage pulse-forming networks. To provide pulsed-current ramp rates of approximately 10 A/ μ s, an insulated-gate bipolar transistor (IGBT) (Q) was added in series with the output of a high-current power supply, as shown in the left schematic of Fig. 9. With Q blocking, the supply (V_s) was in voltage-mode with its output capacitance charged. Turning Q on allowed the supply output capacitance to discharge through the SSCB and the loop inductance (L). When the supply reached its current limit, it switched to current-mode to maintain the current amplitude for the duration of the pulse.

To further increase pulsed-current ramp rates to over 70 A/ μ s, a compact switched RLC circuit was built. Current pulses were provided over a range of ramp rates determined by capacitor voltage and lead inductance. The circuit schematic is shown on the right in Fig. 9. Capacitor (C) was charged by a low-current power supply. IGBT (Q) was gated-on to provide each current pulse. Inductance was changed between tests by adding or removing wire loops to the circuit to function as an air-core inductor. The circuit was made compact enough to form a minimum loop area of approximately 70 cm^2 from the SSCB power terminals. Together, the two pulsed-current circuits facilitated SSCB characterization over 4 orders of magnitude of pulse width. However, current-pulse shapes varied from nearly square for long trip times, to nearly saw-tooth-shaped for short trip times.

The trend of the trip response is affected by the shapes of the current pulses used to characterize it. The average value of a square pulse is equal to its peak value. The average value of a saw-tooth pulse divided by its peak value is 0.5, and that same ratio for a sine wave from 0 to $\pi/2$ is 0.637. For current pulses tripping the SSCB and having average values less than their peak values, the pulse amplitude may be below the trip point for a large portion of the pulse. However, the current below the trip point contributes to the trip time. This issue also affects the trip responses of fuses and mechanical circuit breakers. However, because they respond more slowly, the rise times of

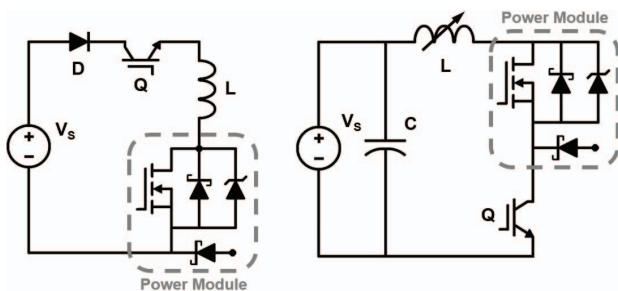


Fig. 9. Switched power-supply pulsed circuit (left) and switched RLC pulsed circuit (right)

their current pulses may be neglected. In this evaluation, the trip response was characterized using the total width and peak amplitude of each current pulse. However, because pulse shapes differed across the data set, the average pulsed current divided by the peak current was used as a figure of merit (FOM) to relate pulse shapes. For pulses having lower FOM values, the reported pulse width includes a significantly long sub-interval with current amplitude below the trip point.

VI. SSCB TRIP RESPONSE

Current pulse widths and amplitudes were recorded with the RLC-pulsed circuit connected to the SSCB with its minimum loop area of about 70 cm^2 , and with up to 7 additional loops of the same area. Fig. 10 shows the data for the minimum loop area (0 loops), 1, 2, 3, 5, and 7 loops at baseplate temperatures of 25 $^{\circ}\text{C}$, 50 $^{\circ}\text{C}$, and 75 $^{\circ}\text{C}$. Each series name has a hyphen between the baseplate temperature and the number of loops. Trip currents are lower at the higher baseplate temperatures for the same pulse widths. This result was expected due to higher sensed voltages caused by the positive temperature coefficient of resistance of the MOSFETs.

For each baseplate temperature set, the data shows an unexpected reverse S-shaped trend. Each 2- and 3-loop series has points with lower peak currents having narrower pulse widths, and points with higher peak currents having wider pulse widths. The trend is also contradicted by the change in current pulse shape within each loop data series. For each loop configuration, the capacitor voltage of the RLC circuit was increased to increase the pulsed-current ramp rate, resulting in narrower pulses with more linear trajectories. Therefore, for each loop configuration, the pulse-shape FOM (average pulsed current divided by peak pulsed current) decreases with decreasing pulse width. Pulses having decreasing FOMs are expected to have increasing peak currents. An explanation for the trend is that the capacitor that functions as an integrator at the output of the controller amplifier stage, functions as a differentiator at the input of the comparator stage. Points in the lower half of the plot bend toward higher trip currents and a lower trip-time limit. This is expected as the SSCB turn-off time becomes significant relative to the current pulse width. Points at the top of the plot show the expected integrator trend of increasing trip current with decreasing pulse width.

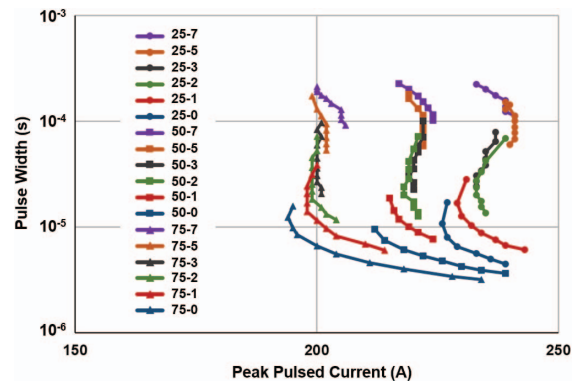


Fig. 10. SSCB trip response with switched RLC circuit for minimum loop area (0), 1, 2, 3, 5, and 7 loops at 25 $^{\circ}\text{C}$, 50 $^{\circ}\text{C}$, and 75 $^{\circ}\text{C}$ baseplate temperatures

The IGBT-switched pulsed circuit was used to extend the trip responses to longer pulse widths. Fig. 11 shows the longer pulse-width data with selected data from Fig. 10, to form the trip-response. The data are shown for maximum pulse widths of approximately 100 ms. For pulse widths longer than this, the trends are increasingly affected by baseplate temperature rise, causing trip currents to decrease for increasing pulse widths. The shapes of the responses for the longer pulse-width data look very similar to the simulated trend shown in Fig. 7.

The horizontal lines in Fig. 11 show the approximate pulse-shape FOM value. Except for the bottom 2 lines, FOM values generally decrease moving down the plot. It is observed that at each baseplate temperature, trip currents are nearly the same at both FOM values of 0.55. Also, these trip currents are higher than those at the FOM of 0.6. This is expected and suggests that for a constant FOM, the values between about 10^{-4} and 10^{-5} s may be more vertical than shown. However, some positive slope is still expected based on the trends of the 2- and 3-loop data series from the pulsed RLC circuit.

The SSCB module was attached to the forced-air cooler, as shown in Fig. 8. Current pulses ranging in width from less than 50 ms to over 50 min were supplied by enabling the output of the high-current power supply. Ambient air temperatures ranged from 22 to 25 °C, over the data set. The trip response with forced-air cooling is shown in Fig. 12, with the data from Fig. 11 included. For pulse widths near 50 ms, the SSCB trips at currents about 6 A lower (about 3.5% lower current) than those with the 25 °C liquid-cooled baseplate. This is a result of additional baseplate temperature rise during each current pulse with air cooling. Moving up the curve, pulse widths increase with decreasing trip current amplitudes. At a pulse width of 1000 s, the SSCB approaches a constant current amplitude of about 100 A. The trend will reach a constant current at the MOSFET thermal-equilibrium point. Following the test having the longest pulse width, at the top of Fig. 12, the SSCB was tested at 102 A for over 3000 s (over 50 min) without tripping. Although the response with 50 °C air-cooling was not tested, a maximum steady-state current can be approximated for 50 °C air-cooling, based on the data in Fig. 12. The offset current between the 50 °C and 25 °C data using liquid cooling is approximately 17 A. Subtracting this current from the tested 102-A steady-state current with 22–25 °C air cooling gives 85

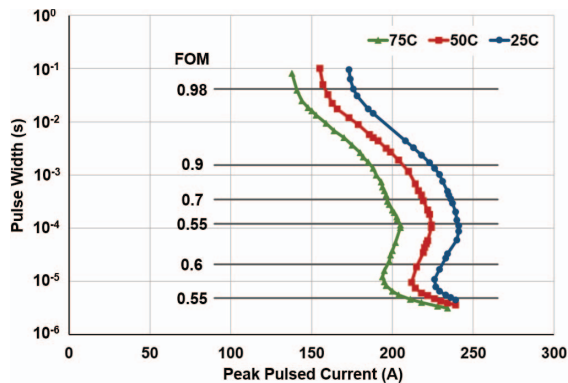


Fig. 11. SSCB trip response including FOM values at 25 °C, 50 °C, and 75 °C baseplate temperatures

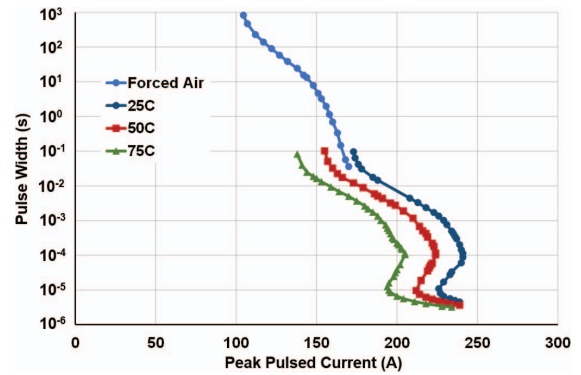


Fig. 12. SSCB trip response including data with 22 to 25 °C forced-air cooling

A. This value compares well with the simulated maximum steady-state current of 87 A using 50 °C air-cooling. This also indicates that the maximum MOSFET temperature at the 102-A test point is near the 150 °C operating value.

VII. CONCLUSION

A 100-A, 850-V, SSCB, having SiC MOSFETs, SiC Schottky diodes, and SiC avalanche breakdown diodes was developed. The SSCB has a 32 cm² footprint and is able to continuously conduct up to 100-A with 25 °C air cooling. It was designed with an analog controller that provides a configurable trip-response characteristic to allow a range of overcurrent transients to be conducted, while maintaining a fast response at its fault-current limit. The controller also provides remote trip, status output, and reset functions. Test-circuits were built to provide current pulses with ramp rates up to over 70 A/μs. A pulse-shape FOM was used to relate pulse shapes provided by the test circuits. The SSCB trip response was characterized at baseplate temperatures of 25 °C, 50 °C, and 75 °C. The trip response showed expected trends associated with the controller integrator and the power-module thermal resistance, and an unexpected differentiator trend. A minimum pulse width of 3.2 μs was demonstrated for a nearly saw-tooth-shaped 234-A current pulse, at a baseplate temperature of 75 °C. With 22–25 °C air cooling, the SSCB conducted 102 A continuously for over 50 min (the test duration) without tripping. In total, the SSCB trip response was characterized over nearly 9 orders of magnitude in current pulse widths.

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