A Gate Assist Circuit for Cross Talk Suppression of SiC Devices in a Phase-leg Configuration

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Abstract— In a phase-leg configuration, the high switching-speed performance of silicon carbide (SiC) devices is limited by the interaction between the upper and lower devices during the switching transient (cross talk), leading to additional switching losses and overstress of the power devices. To utilize the full potential of fast SiC devices, this paper proposes a gate assist circuit using two auxiliary transistors and a diode to eliminate cross talk. Based on CMF20120D SiC MOSFETs, the experimental results show that this gate assist methodology is effective to suppress cross talk under different operating conditions, enabling turn-on switching losses reduction by up to 19.6%, and negative spurious gate voltage minimization within the maximum allowable negative gate voltage of the power devices without the penalty of reduced switching speed. Moreover, in comparison to the conventional gate driver with -2 V turn-off gate voltage, this gate assist circuit without a negative isolated power supply is more effective in enhancing the switching behavior of power devices in a phase-leg. Accordingly, the proposed gate assist circuit is a cost-effective solution for cross talk suppression.

I. INTRODUCTION

To achieve higher performance power conversion, wide band-gap semiconductor devices such as silicon carbide (SiC) have become a promising alternative to silicon, offering increased junction operating temperature, low specific on-resistance, and high switching-speed capability. Among these benefits, the fast switching performance plays a key role in reducing switching losses, shortening dead time for a phase-leg, and increasing switching frequency. All of these are beneficial to high power efficiency, quality, and density [1-6].

However, in an actual converter using the phase-leg configuration, high dv/dt during fast switching transient of one device will affect the operating behavior of its complementary device [7-14]. This interaction between the two switches is cross talk [14].

Specifically, during the turn-on transient of the lower switch, as can be observed in Fig. 1(a), the positive charge stored in the Miller capacitance of the upper switch is transferred via its gate loop, inducing a positive spurious gate voltage. Thus, the upper switch may be partially turned on; and a shoot-through current will be generated, leading to

additional switching losses in both switches and even shoot-through failure. In addition, based on the transfer characteristics of power devices, this extra shoot-through current increases the channel current, and then affects the gate voltage of the lower switch. The increased gate voltage reduces the gate current, resulting in the decrease of dv/dt . Thus, the turn-on switching speed of the lower switch will also be limited by this self-regulating mechanism [14].

Fig. 1 Mechanism causing cross talk interference with conventional gate driver: (a) Turn-on transient of lower switch; and (b) Turn-off transient of lower switch.

TABLE I. CHARACTERISTICS OF SEVERAL COMPARABLE Si/SiC POWER DEVICES [22-26]

Type	Manufacturer	Model	V_{DS} / I_D (100 °C)	V_{th} (25 °C)	$V_{gs_max(-)}$	$R_{g(in)}$
TFS Si IGBT	Fairchild	FGA20N120FTD	1200 V / 20 A	5.9 V	-25 V	N/A
NPT Si IGBT	IR	IRG4PH505	1200 V / 33 A	4.5 V	-20 V	1.6 Ω
Si MOSFET	Microsemi	APT34M120J	1200 V / 22 A	4.0 V	-30 V	N/A
SiC MOSFET	CREE	CMF20120D	1200V / 17 A	2.5 V	-5 V	5 Ω
SiC JFET	Semisouth	SJEP120R100	1200V / 17A	1.0 V	-15 V	6 Ω

On the other hand, during turn-off transient of the lower switch, as shown in Fig. 1(b), the negative spurious voltage induced at the gate-source terminals of the upper switch may overstress the power device if its magnitude exceeds the maximum allowable negative gate voltage acceptable to the semiconductor device.

Based on the aforementioned analysis, the core element of cross talk during both turn-on and turn-off transients of the lower switch is the spurious gate voltage of the upper switch. Ignoring the impact of parasitic inductance, the peak value of this spurious gate voltage is shown as [10]-[14],

$$v_{gs_H(max)} = a \times \frac{(R_{g_H} + R_{g(in)_H})C_{gd_H} \times V_{DC}}{(1 - e^{-a \times C_{iss_H}(R_{g_H} + R_{g(in)_H})})} \quad (1)$$

where a is the slew rate of drain-to-source voltage of the lower switch V_{ds_H} , partially representing the switching speed. R_{g_H} , $R_{g(in)_H}$, C_{gd_H} and C_{iss_H} refer to the external gate resistance, internal gate resistance, Miller capacitance and input capacitance of the upper switch, as shown in Fig. 1.

Therefore, in a phase-leg configuration, to fully utilize the potential advantages of fast SiC devices and guarantee the reliability of the power converter, cross talk should be suppressed. Prior reported work has proposed several methods for cross talk mitigation [5, 15-19]. They can be divided into three categories:

1) Add additional capacitance between gate-source terminals to shunt the Miller current [15-18]. This external gate-source capacitor is to take up additional charge originating from the Miller capacitance, resulting in spurious gate voltage reduction, and cross talk mitigation for the affected power device. While the device is under operation, this capacitor will worsen the switching performance with slower switching speed and higher switching losses.

2) Apply a negative biased turn-off gate voltage [15-18]. This method suppresses the impact of cross talk during the turn-on transient, but worsens the overstress of power devices due to the higher negative spurious gate voltage induced during the turn-off transient, especially for the SiC device when considering its lower maximum allowable negative gate voltage compared with the silicon-based power device (see Table I). Additionally, this method is less cost-effective due to the additional negative isolated power supply that is required.

3) Use active Miller clamping [18, 19]. The operation principle of this method is to activate an additional

transistor between the gate-source terminals to short the gate-source region after detecting the gate voltage of the affected power device above the clamp threshold [18]. Thus, it is the measured gate voltage that is used to identify the existence of cross talk. However, due to the relatively large internal gate resistance of SiC devices, as shown in Table I, the measured spurious gate voltage is less than that across the internal gate-source terminals. Moreover, during the fast switching transient, the measured gate voltage will be greatly interfered due to the coupling of the common source inductance (i.e., L_{cs_L} and L_{cs_H} as shown in Fig. 1) between the gate loop and power loop, which is inevitable in practical situations [20, 21]. Thus, active Miller clamping is not suitable for SiC power devices.

Additionally, previous studies of cross talk suppression merely focus on the Cdv/dt induced shoot-through, with little attention on the harm of the negative spurious gate voltage [5, 15-19]. Moreover, because of the relatively low maximum allowable negative gate voltage of SiC power devices, the negative spurious gate voltage would easily exceed its range, and overstress the power devices.

In summary, on account of the intrinsic characteristics of SiC power devices, such as low threshold gate voltage, low maximum allowable negative gate voltage, and large internal gate resistance, cross talk would become more serious, and the suitable solution for cross talk mitigation is critical. Thus, this paper proposes a gate assist circuit to eliminate cross talk for SiC power devices in a phase-leg. First, according to the mechanism causing cross, the basic ideas for cross talk elimination are introduced. Second, based on the ideas, a gate assist circuit is proposed, and its structure and operation principle are presented. Third, the design of primary parameters of this gate assist circuit is discussed. Finally, a double pulse tester with CMF20120D SiC MOSFETs is established to demonstrate the validity and effectiveness of this new gate assist methodology.

II. BASIC IDEA FOR CROSS TALK SUPPRESSION

According to the mechanism causing cross talk, the core element of cross talk is the spurious gate voltage. Its amplitude is determined by the portion of displacement current from the Miller capacitance that is used to charge/discharge the gate-source capacitance of the affected device. Therefore, once its gate impedance becomes small during the switching transient, most displacement current will be bypassed by the gate loop, resulting in less current that would induce spurious gate voltage. In other words, regulating gate loop impedance

of the effected device during the switching transient of the operating one is a solution for cross talk mitigation.

Also, another more direct solution to avoid cross talk is to actively control the gate voltage of the affected device during the switching transient of the opposite switch in a phase-leg. For instance, we can negatively pre-charge the gate-source capacitance of the upper switch before the turn-on transient of the lower switch so that Cdv/dt induced positive spurious gate charge will be cancelled by this pre-stored negative gate charge. Once the pre-stored gate-source charge of the upper switch is sufficient, cross talk during the turn-on transient of the lower switch can be eliminated.

In summary, gate impedance regulation and gate voltage control are the two basic ideas for cross talk suppression, among which, the gate voltage control methodology is a more direct and effective option. In this paper, gate voltage control is applied for cross talk elimination during turn-on transient. Besides, during turn-off transient, considering the potential hazard of shoot-through due to the pre-stored positive charge of the gate-source capacitance by using gate voltage control, the gate impedance regulation is selected for the negative spurious gate voltage minimization.

III. STRUCTURE AND OPERATION PRINCIPLE OF GATE ASSIST CIRCUIT

Based on the aforementioned concept, a gate assist circuit for cross talk suppression and its corresponding logic signals for control of the transistors are proposed, as shown in Fig. 2. Compared with the conventional gate drive circuit (S_{1_H} , S_{2_H} or S_{1_L} , S_{2_L}), two auxiliary transistors (S_{a1_H} and S_{a2_H} or S_{a1_L} and S_{a2_L}) together with one diode (D_{a_H} or D_{a_L}) are added between the gate-source terminals of each device, while the commonly used negative isolated power supply (V_{2_H} or V_{2_L}) is not needed (see Fig. 1). Fig. 3 displays the operating procedure of the proposed gate assist circuit, described as follows.

Fig. 2. Active gate driver for gate voltage control: (a) Active gate driver with gate assist circuit (S_{a1_H} , S_{a2_H} , D_{a_H} or S_{a1_L} , S_{a2_L} , D_{a_L}); and (b) corresponding logic signals of main device (S_{1_H} or S_{1_L}) and auxiliary transistors (S_{a1_H} , S_{a2_H} or S_{a1_L} , S_{a2_L}).

Subinterval 1 [$t_1 - t_2$]: Gate-source capacitance pre-charge of the upper switch. Before the lower switch starts to turn on, S_{1_H} and auxiliary transistor S_{a2_H} turn off; S_{2_H} and auxiliary transistor S_{a1_H} turn on. Via the loop formed by S_{2_H} , S_{a1_H} and R_{g_H} , the positive turn-on gate voltage V_{1_H} is used to pre-charge the gate-source capacitance of the upper switch C_{gs_H} to the required negative voltage for the cross talk elimination at the end of t_2 . The duration of this subinterval is determined by the required pre-charge negative voltage, which will be discussed in detail in the next section. At the end of t_2 , the lower switch starts to turn on.

Subinterval 2 [$t_2 - t_3$]: Turn-on transient of the lower switch. S_{1_L} turns on, S_{2_L} turns off, auxiliary transistor S_{a2_L} remains on, and S_{a1_L} remains off. Since the junction capacitance of the auxiliary diode D_{a_L} is usually an order of magnitude smaller than the input capacitance of the main power device, this auxiliary circuit has negligible impact on the turn-on switching behavior of the lower switch. Meanwhile, auxiliary transistor S_{a1_H} turns off and S_{a2_H} remains off. Due to the body diode of S_{a2_H} and auxiliary diode D_{a_H} , instead of bypassing through the external gate loop, the negative charge pre-stored in C_{gs_H} is fully utilized to cancel the positive charge transferred from the Miller capacitance of the upper switch C_{gd_H} . Once this pre-stored negative gate-source charge (i.e., negative gate voltage) is sufficient, cross talk during the turn-on transient of the lower switch can be eliminated. At the end of t_3 , the turn-on transient of the lower switch is completed.

Subinterval 3 [$t_3 - t_4$]: Fully turn-on the lower switch. Auxiliary transistor S_{a2_H} turns on. The residual negative voltage across C_{gs_H} at subinterval 2 returns to 0 for the preparation of cross talk mitigation during the upcoming turn-off transient of the lower switch. At the end of t_4 , the lower switch starts to turn off.

(a) Subinterval 1 $[t_1 - t_2]$

(b) Subinterval 2 $[t_2 - t_3]$

(c) Subinterval 3 $[t_3 - t_4]$

(d) Subinterval 4 $[t_4 - t_5]$

Fig. 3. Operation principle of the gate voltage control (GVC) circuit: (a) Subinterval 1 $[t_1 - t_2]$; (b) Subinterval 2 $[t_2 - t_3]$; (c) Subinterval 3 $[t_3 - t_4]$; (d) Subinterval 4 $[t_4 - t_5]$.

Subinterval 4 $[t_4 - t_5]$: Turn-off transient of the lower switch. $S_{1,L}$ turns off and $S_{2,L}$ turns on. Switching status of all auxiliary transistors are the same as that during subinterval 3. This auxiliary circuit does not affect the turn-off switching performance of the lower switch, just as in subinterval 2. Meanwhile, auxiliary transistor $S_{a2,H}$ and diode $D_{a,H}$ offer a low impedance loop to C_{dv}/dt induced current during the turn-off transient of the lower switch, that is, the gate loop impedance of the upper switch is largely decreased. Therefore, the negative spurious gate voltage is minimized. At the end of t_5 , the turn-off transient of the lower switch is finished.

Based on the circuit symmetry, the operation principle during switching transient of the upper switch, i.e., subintervals 5-8, as shown in Fig. 2(b), are similar to that during subintervals 1-4. Specifically, subintervals 5-8 correspond to gate-source capacitance pre-charge of the lower switch, turn-on transient of the upper switch, fully turn-on the upper switch, and turn-off transient of the upper switch, respectively.

According to the operation principle, the logic signals for the control of auxiliary transistors can be synthesized merely based on the logic signals of the main power devices using several logic gates. Thus, through feedforward control, this gate assist circuit is well suited for SiC power devices with fast switching capability.

IV. PRIMARY PARAMETERS DESIGN

For cross talk suppression, the pre-stored gate-source charge must be capable of cancelling the charge stored in the Miller capacitance. I.e., the gate voltage variation due to the gate-drain charge during the switching transient has to be lower than that pre-charged across the gate-source capacitance, as in (2)

$$Q_{gs(pre)} \geq Q_{Miller} \text{ or } V_{gs(pre)} \geq \Delta V_{gs} = \frac{C_{gd}V_{DC}}{C_{gs}} \quad (2)$$

where $Q_{gs(pre)}$ and Q_{Miller} refer to the pre-stored gate-source charge and gate-drain charge, respectively. $V_{gs(pre)}$ and ΔV_{gs} are the pre-charged gate voltage and the gate voltage variation during switching transient. C_{gd} and C_{gs} indicate the Miller capacitance and gate-source capacitance of the power device. Based on $V_{gs(pre)}$, the pre-charge duration at subinterval 1 and 5 should satisfy

$$t_{pre} \geq -(R_g + R_{g(in)}) \times C_{iss} \times \ln(1 - \frac{\Delta V_{gs}}{V_1}) \quad (3)$$

where t_{pre} represents the pre-charge duration. R_g , $R_{g(in)}$, and C_{iss} refer to the external gate resistance, internal gate resistance, and input capacitance of the power devices, respectively. V_1 is the positive output voltage of the gate driver. Note that t_{pre} is only related to the operating voltage, no matter how large the variation of load current and gate resistance. Once t_{pre} is selected under the maximum operating voltage, this gate assist circuit can eliminate Cdv/dt induced shoot-through under different operating conditions. Practically, t_{pre} is tens of nanoseconds.

V. EXPERIMENTAL VERIFICATION

Double pulse tester board with CMF20120D SiC MOSFETs is established, as shown in Fig. 4. Fig. 5 displays the gate driver board with the proposed gate assist circuit, which consists of Si5902BDC Dual N-Channel Si MOSFETs with MSS1P3 Schottky Barrier diode. To evaluate the effectiveness of the proposed gate assist circuit for cross talk elimination, the comparison experiments are conducted under three different groups according to with or without gate assist circuit as well as with or without negative biased turn-off gate voltage, listed in Table II. For each group, 12 cases with gate resistances of 10/4.7 Ω , operating voltages of 800/600 V, and operating currents of 5/10/20 A are tested.

TABLE II. THREE COMPARISON GROUPS

1 st Group	w/o gate assist circuit with V_{gs} of 20/0 V
2 nd Group	w/o gate assist circuit with V_{gs} of 20/-2 V
3 rd Group	w/ gate assist circuit with V_{gs} of 20/0 V

Fig. 4. Test board setup.

Fig. 5. Gate driver board.

Fig. 6 shows the comparison waveforms under three different groups with the operating condition of 800-V/10-A with 10 Ω gate resistance. During turn-on transient of the lower switch, the turn-on energy losses of the lower switch with gate assist circuit are less than that without gate assist circuit, even if -2 V turn off gate voltage is applied. Meanwhile, without further reducing the switching speed, this gate assist circuit improves the slew rate of the drain-to-source voltage. Also, the excessive switching losses of the upper switch generated by Cdv/dt induced shoot-through current are decreased once the gate assist circuit is adopted. Moreover, during the turn-off transient of the upper switch, the gate assist circuit enables the spurious negative gate voltages of the lower switch to be largely suppressed.

For example, under V_{gs} of 20/0 V, with gate assist circuit, the turn-on energy loss of the lower switch and shoot-through energy loss of the upper switch are reduced by 55.0 μ J and 45.5 μ J, respectively, enabling total turn-on energy loss savings of approximately 19.4%. In the meantime, dv/dt increases from 22.7 V/ns to 24.9 V/ns. Also, the negative peak value of the spurious gate voltage is minimized from -6.6 V which exceeds -5 V, the maximum rating of negative gate voltage of the CMF20120D, listed in Table I, to -0.9 V.

Fig. 7 displays the comparison test results dependence on the load current under the dc bus voltage of 800 V with 10 Ω gate resistance. In order to clearly demonstrate the effectiveness of the proposed gate assist circuit, the turn-on energy loss and dv/dt under second and third group are normalized based on that under first group, which are listed in Table III. It shows that under different load currents, the turn-on energy losses with gate assist circuit are always less than that without gate assist circuit and dv/dt is higher, even for the case of when -2 V turn-off gate voltage is applied in the conventional gate driver. Note also that the gate assist circuit has the capability of limiting the negative peak value of spurious gate voltages within its required range.

Fig. 8 presents the comparison test results dependence on dc bus voltage and gate resistance under the load current of 10 A. According to the conditions under the first group listed in Table IV, turn-on energy loss and dv/dt under the second and third group are managed the same as that in Fig. 7. The experimental results show that under different dc bus voltage with varying gate resistances, the proposed gate assist circuit is more effective to improve the switching behavior of power devices in a phase-leg configuration by the comparison to

the conventional gate circuit, even with -2 V turn-off gate voltage.

Fig. 6. Comparison test results: (a) Lower switch waveforms during the turn-on transient of the lower switch; (b) Upper switch waveforms during the turn-on transient of the lower switch; and (c) Lower switch waveforms during the turn-off transient of the upper switch.

TABLE III. E_{ON} & dv/dt vs. I_L UNDER 1ST GROUP WITH V_{DC} OF 800V & R_g OF 10 Ω

I_L (A)	5	10	20
E_{ON} (μ J)	381.3	519.0	852.6
dv/dt (V/ns)	23.5	22.7	21.1

TABLE IV. E_{ON} & dv/dt vs. V_{DC} & R_g UNDER 1ST GROUP WITH I_L OF 10A

V_{DC}/R_g (V/ Ω)	600/4.7	600/10	800/4.7	800/10
E_{ON} (μ J)	263.8	332.0	416.3	519.0
dv/dt (V/ns)	29.7	19.7	33.1	22.7

Fig. 7. Comparison test results dependence on load current: (a) Normalized turn-on energy losses during the turn-on transient of the lower switch; (b) Normalized dv/dt during the turn-on transient of the lower switch; and (c) Negative peak value of spurious gate voltage during the turn-off transient of the upper switch.

Fig. 8. Comparison test results dependence on dc bus voltage and gate resistance: (a) Normalized turn-on energy losses during the turn-on transient of the lower switch; (b) Normalized dv/dt during the turn-on transient of the lower switch; and (c) Negative peak value of spurious gate voltage during the turn-off transient of the upper switch.

In summary, the gate assist circuits have the capability for cross talk suppression. Considering the all transistor based auxiliary components, this gate assist circuit is a

suitable gate assist for gate driver chip-level integration, which will largely simplify the implementation of relatively complicated logic signal synthesis.

V. CONCLUSIONS

Based on the intrinsic characteristics of SiC power devices, a gate assist circuit using two auxiliary transistors together with a diode is proposed for cross talk suppression in a phase-leg configuration. The test results with CMF20120D SiC MOSFETs verify that without the negative turn-off gate voltage, this gate assist circuit has the capability to fully suppress cross talk under different operating conditions. It shows improved switching performance in comparison with the conventional gate drive, even with -2 V turn-off gate voltage: turn-on transient becomes faster; turn-on switching loss was reduced up to 19.4%; and spurious negative gate voltage is always suppressed within its required range. This all-transistor based gate assist circuit offers a simple, efficient, and cost-effective solution for cross talk elimination. Also, it is a promising option for gate driver chip-level integration.

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