

# Three Phase VSI with Reduced Output Voltage Distortion Using FPGA Based Multisampled Space Vector Modulation

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**Abstract** – This paper demonstrates reduced output voltage distortion in a three phase voltage source inverter (VSI) when digital multisampled space vector modulation is used. The modulator and the inverter controller are implemented entirely using a field programmable gate array (FPGA) platform, thus achieving increased bandwidth with respect to a typical digital signal processor (DSP) or microprocessor based controller. Increased controller bandwidth results in lower output voltage harmonic distortion in the frequency range above the fundamental and below the switching frequency. Experimental validation is presented together with the analysis carried out using a state space model of a VSI with an output LC filter.

**Index Terms**– Field programmable gate arrays, Pulse width modulated inverters, Sampling methods, Space vector modulation.

## I. INTRODUCTION

Digital pulse width modulation (PWM) techniques have been extensively studied over the last decade due to the availability of low cost, high performance digital controllers. While DSPs have been the most common platform to implement digital PWM, new devices allowing parallel computation have recently been used for power converter control. FPGAs have recently become very popular platforms for the implementation of digital PWM in three phase inverters, including space vector modulation [1-8]. FPGAs have the advantage over DSPs that instructions can be executed in parallel rather than in series, thus reducing processing time and increasing the controller bandwidth. In particular an FPGA based PWM modulator can take multiple samples of the reference voltage and recompute the power converter switching states and timers several times over one switching period [4],[9-11]. This is a clear advantage over typical DSP based controllers where the reference is typically sampled no more than twice in one switching period, with a technique often referred to as “double update” [12].

The multiple sampling method is addressed in [4] as “re-sample uniform” and is applied to sine triangle PWM, while in [9] and [10] is called “multisampled” PWM and is used to control dc-dc converters. In [11] the term “naturally sampled

space vector modulation” is used to indicate that “oversampling” approaches the bandwidth of the classic naturally sampled (analog) pulse width modulator [13-15].

This paper presents the analytical and experimental verification that an FPGA based controller reduces the output voltage distortion in a space vector modulated voltage source inverter. This is possible because of the increased controller bandwidth which is achieved via multiple sampling of the reference voltage over one switching period when space vector modulation is implemented.

The digest is organized as follows: section II presents the multiple sampling technique with a brief overview of space vector modulation. In section III the linearized model of the inverter including load and controller is presented through state space equations. The simulated and experimental Bode plots used to tune the PI controllers are also included. Section IV presents experimental measurements to support the claim of reduced VSI output voltage distortion. The conclusions are presented in section V.

## II. FPGA IMPLEMENTATION OF SPACE VECTOR MODULATION WITH MULTIPLE SAMPLING

The space vector modulation technique for the three phase VSI shown in Fig. 1 is well known and well documented,[11,13-15]. The space vector hexagon shown in Fig. 2 maps the eight possible switching states for the six transistors in the VSI. The six active switching states are identified by vectors and labels such as (pnn) where p and n indicate connection to the positive and negative DC bus respectively. The switching state (pnn) means that phase A is connected to the positive DC bus ( $V_{an}=V_{dc}/2$ ) because the top transistor is on and that phases B and C are connected to the negative DC bus ( $V_{bn}=V_{cn}=-V_{dc}/2$ ) because their bottom transistors are on. The two zero vectors, (nnn) and (ppp), are represented by a single point in the center of the hexagon. Fig. 2 shows that a reference voltage,  $V_{ref}$ , can be obtained by spending some time,  $T_1$  and  $T_2$  respectively, on each of the two adjacent states,  $V_1$  and  $V_2$ , and some time,  $T_0$ , on one of the zero states. The sum of the three timers must be equal to

the switching period,  $T_s$ , as shown in (1).

$$T_s = T_1 + T_2 + T_0$$

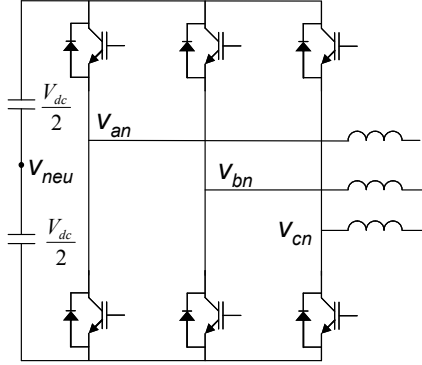


Fig. 1: Three phase VSI.

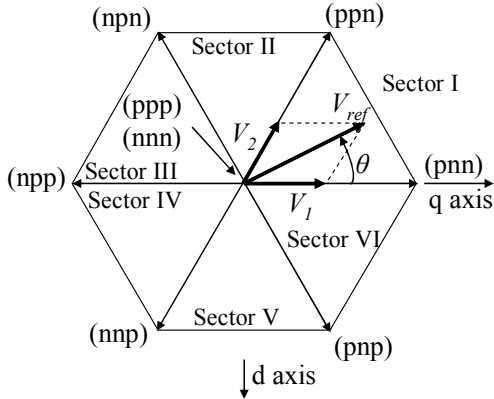


Fig. 2: Space vector hexagon.

The reference voltage,  $V_{ref}$ , is typically sampled once (single update) or twice (double update) during one switching period,  $T_s$ . The timers that define how long to stay at each switching state,  $T_0$ ,  $T_1$  and  $T_2$ , are updated every time the reference voltage is sampled. As the update rate of the sampled signals increases the discrete system converges on the behavior of a continuous system provided that the entire discrete algorithm is being updated at a very high rate [11]. With the use of an FPGA the reference voltage,  $V_{ref}$ , can be sampled multiple times over one switching period. Fig. 3 shows the cases when 1, 2 and 4 samples of  $V_{ref}$  are taken per switching period. In this paper typical double update PWM is compared to PWM with 20 updates per period to show how the increased update rate reduces the output voltage phase and gain error. Details of the FPGA implementation can be found in [11].

### III. STATE SPACE MODEL OF A VSI WITH OUTPUT LC FILTER

In order to tune the controller gains of the VSI, the linearized state space model of a VSI with a second order filter ( $L_f$ ,  $C_f$ ) and a load ( $L_o$ ,  $R_o$ ) was derived and is presented in this section. The output filter components are

shown in Fig. 4 and the control system is shown in

(1) Fig. 5. The passive components are presumed identical on all three phases in Fig. 4.

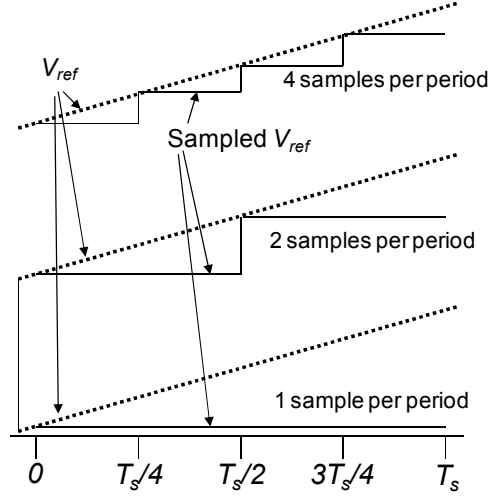


Fig. 3: Voltage reference sampling example.

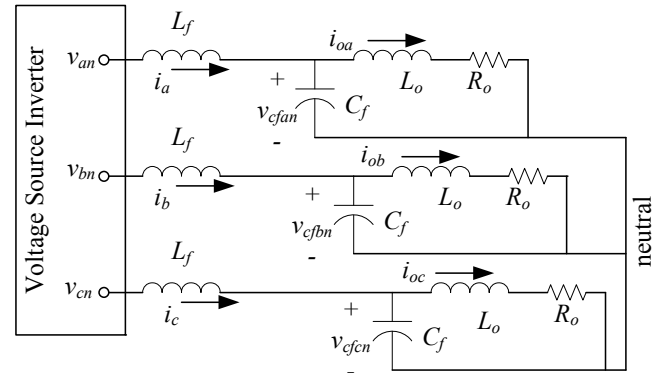


Fig. 4: VSI output filter and load.

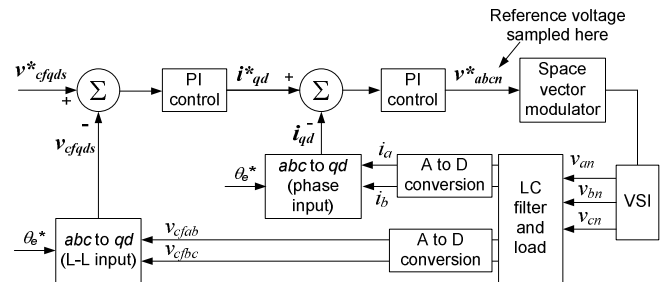


Fig. 5: Block diagram of the VSI controller as implemented in the experimental set-up.

The controller block diagram in Fig. 5 includes abc variables as well as synchronous reference frame variables used for the PI controllers. When the circuit variables are transformed to the qd reference frame, the zero sequence variables are ignored because the zero sequence load current is zero ( $i_{oa} + i_{ob} + i_{oc} = 0$ ), therefore we will only discuss the qd reference frame. In particular the filter capacitor voltages,  $v_{cfan}$ ,  $v_{cfbn}$ ,  $v_{cfcn}$ , transformed into the qd reference frame are

labeled as  $v_{cfqds} = (v_{cfqs}, v_{cfds})$ . Similarly the inverter currents ( $i_a, i_b, i_c$ ), transformed into the  $qd$  reference frame become  $i_{qd} = (i_q, i_d)$  in Fig. 5. The asterisks indicate reference variables.

The controller shown in Fig. 5 includes two control loops. First, the inverter voltages ( $v_{an}, v_{bn}, v_{cn}$ ) are used to control the inverter output currents ( $i_a, i_b, i_c$ ). The inverter output currents ( $i_a, i_b, i_c$ ) are then used to control the filter capacitor voltages ( $v_{cfan}, v_{cfbn}, v_{cfcn}$ ). The equations are derived for an arbitrary reference frame representation of the system [16], although the PI controllers are implemented in the synchronous reference frame.

In order to derive the state space model of the system, the differential equations in the  $s$  domain (2), (3) and (4) representing the physical subsystem in Fig. 4 are transformed from the  $abc$  to the  $qd$  reference frame using the well known transformation matrix (4) (5) [16]. This transformation can be shown to yield the set of differential equations in matrix format (6), where the matrices  $\mathbf{M}_{ph}$  and  $\mathbf{N}_{ph}$  are shown in (7) and (8) respectively. The subscript “ph” stands for “physical system”, referring to the VSI output filter and load passive components shown in Fig. 4. The currents  $i_{oqs}, i_{ods}$  are derived by transforming the output currents  $i_{oa}, i_{ob}, i_{oc}$ , into the  $qd$  reference frame and the voltages  $v_{qs}, v_{ds}$  are derived by transforming the inverter voltages  $v_{an}, v_{bn}, v_{cn}$ , into the  $qd$  reference frame.

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = sL_f \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} v_{cfan} \\ v_{cfbn} \\ v_{cfcn} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = sC_f \begin{bmatrix} v_{cfan} \\ v_{cfbn} \\ v_{cfcn} \end{bmatrix} + \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} v_{cfan} \\ v_{cfbn} \\ v_{cfcn} \end{bmatrix} = sL_o \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} + R_o \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \quad (4)$$

$$\mathbf{K}_s = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (5)$$

$$\mathbf{M}_{ph} \begin{bmatrix} i_{qs} \\ i_{ds} \\ v_{cfqs} \\ v_{cfds} \\ i_{oqs} \\ i_{ods} \end{bmatrix} + s\mathbf{N}_{ph} \begin{bmatrix} i_{qs} \\ i_{ds} \\ v_{cfqs} \\ v_{cfds} \\ i_{oqs} \\ i_{ods} \end{bmatrix} - \begin{bmatrix} v_{qs} \\ v_{ds} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = 0 \quad (6)$$

$$\mathbf{M}_{ph} = \begin{bmatrix} 0 & \omega L_f & 1 & 0 & 0 & 0 \\ -\omega L_f & 0 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & \omega C_f & 1 & 0 \\ 0 & -1 & -\omega C_f & 0 & 0 & 1 \\ 0 & 0 & -1 & 0 & R_o & \omega L_o \\ 0 & 0 & 0 & -1 & -\omega L_o & R_o \end{bmatrix} \quad (7)$$

$$\mathbf{N}_{ph} = \begin{bmatrix} L_f & 0 & 0 & 0 & 0 & 0 \\ 0 & L_f & 0 & 0 & 0 & 0 \\ 0 & 0 & C_f & 0 & 0 & 0 \\ 0 & 0 & 0 & C_f & 0 & 0 \\ 0 & 0 & 0 & 0 & L_o & 0 \\ 0 & 0 & 0 & 0 & 0 & L_o \end{bmatrix} \quad (8)$$

The next step is to include the control system. In order to accomplish this goal the assumption of unity gain for the switching inverter is made and equations (9) and (10) can be written for the two PI controllers, with  $v_{qs}$  &  $v_{ds}$  being the  $q$  and  $d$  axis inverter output voltages,  $i_{qs}^*$  &  $i_{ds}^*$  the  $q$  and  $d$  axis reference currents. The symbols  $K_{p_v}$  and  $K_{i_v}$  represent the proportional and integral gain in the voltage control loop respectively. The symbols  $K_{p_i}$  and  $K_{i_i}$  represent the proportional and integral gain in the current control loop respectively.

$$\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} = \left( K_{p_i} + \frac{K_{i_i}}{s} \right) \left( \begin{bmatrix} i_{qs}^* \\ i_{ds}^* \end{bmatrix} - \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} \right) \quad (9)$$

$$\begin{bmatrix} i_{qs}^* \\ i_{ds}^* \end{bmatrix} = \left( K_{p_v} + \frac{K_{i_v}}{s} \right) \left( \begin{bmatrix} v_{cfqs}^* \\ v_{cfds}^* \end{bmatrix} - \begin{bmatrix} v_{cfqs} \\ v_{cfds} \end{bmatrix} \right) \quad (10)$$

In order to include the two PI controllers in the state space model of the system some manipulation of the equations is required. First, the integrators of PI controllers are represented as state variables as shown in (11) and (12).

$$\begin{bmatrix} xv_{qs} \\ xv_{ds} \end{bmatrix} = \frac{K_{i-v}}{s} \left( \begin{bmatrix} v_{cfqs}^* \\ v_{cfds}^* \end{bmatrix} - \begin{bmatrix} v_{cfqs} \\ v_{cfds} \end{bmatrix} \right) \quad (11)$$

$$\begin{bmatrix} xi_{qs} \\ xi_{ds} \end{bmatrix} = \frac{K_{i-i}}{s} \left( \begin{bmatrix} i_{qs}^* \\ i_{ds}^* \end{bmatrix} - \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} \right) \quad (12)$$

Substituting (11) and (12) into (10) and (9) respectively and rearranging, yields (13) and (14).

$$\begin{bmatrix} i_{qs}^* \\ i_{ds}^* \end{bmatrix} = K_{p-v} \left( \begin{bmatrix} v_{cfqs}^* \\ v_{cfds}^* \end{bmatrix} - \begin{bmatrix} v_{cfqs} \\ v_{cfds} \end{bmatrix} \right) + \begin{bmatrix} xv_{qs} \\ xv_{ds} \end{bmatrix} \quad (13)$$

$$\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} = K_{p-i} \left( \begin{bmatrix} i_{qs}^* \\ i_{ds}^* \end{bmatrix} - \begin{bmatrix} i_{qs} \\ i_{ds} \end{bmatrix} \right) + \begin{bmatrix} xi_{qs} \\ xi_{ds} \end{bmatrix} \quad (14)$$

Finally, using (11) through (14) in (6) and rearranging so that the reference currents  $i_{qs}^*$  &  $i_{ds}^*$  are eliminated, the differential equations in matrix format (15) are obtained with the filter capacitor  $q$  and  $d$  axes reference voltages,  $v_{cfqs}^*$  &  $v_{cfds}^*$  as the only inputs. The matrices  $\mathbf{M}$ ,  $\mathbf{N}$  and  $\mathbf{P}$  are

shown in (16), (17) and (18) respectively. From (15) the state space equations in standard format,  $\dot{\mathbf{s}}\mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}$ , can be derived with  $\mathbf{A} = -\mathbf{N}^{-1}\mathbf{M}$  and  $\mathbf{B} = -\mathbf{N}^{-1}\mathbf{P}$ .

$$\mathbf{M} \begin{bmatrix} i_{qs} \\ i_{ds} \\ v_{cfq} \\ v_{cfd} \\ i_{oq} \\ i_{od} \\ xi_q \\ xi_d \\ xv_q \\ xv_d \end{bmatrix} + s\mathbf{N} \begin{bmatrix} i_q \\ i_d \\ v_{cfq} \\ v_{cfd} \\ i_{oq} \\ i_{od} \\ xi_q \\ xi_d \\ xv_q \\ xv_d \end{bmatrix} + \mathbf{P} \begin{bmatrix} v_{cfq}^* \\ v_{cfd}^* \end{bmatrix} = 0 \quad (15)$$

The state variables  $xi_q$ ,  $xi_d$ ,  $xv_q$ ,  $xv_d$ , represent the integrators of the PI controllers in the system as defined in (11) and (12). While (15) was derived for a generic  $qd$  reference frame, the synchronous reference frame was used for the control system as shown in Fig. 5.

$$\mathbf{M} = \begin{bmatrix} K_{p-i} & \omega L_f & 1+K_{p-i}K_{p-v} & 0 & 0 & 0 & -1 & 0 & -K_{p-i} & 0 \\ -\omega L_f & K_{p-i} & 0 & 1+K_{p-i}K_{p-v} & 0 & 0 & 0 & -1 & 0 & -K_{p-i} \\ -1 & 0 & 0 & \omega C_f & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & -\omega C_f & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & R_o & \omega L_o & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & -\omega L_o & R_o & 0 & 0 & 0 & 0 \\ K_{i-i} & 0 & K_{i-i}K_{p-v} & 0 & 0 & 0 & 0 & 0 & -K_{i-i} & 0 \\ 0 & K_{i-i} & 0 & K_{i-i}K_{p-v} & 0 & 0 & 0 & 0 & 0 & -K_{i-i} \\ 0 & 0 & K_{i-v} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & K_{i-v} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (16)$$

$$\mathbf{N} = \begin{bmatrix} L_f & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_f & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_f & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_f & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & L_o & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & L_o & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (17)$$

$$\mathbf{P} = \begin{bmatrix} -K_{p-i}K_{p-v} & 0 \\ 0 & -K_{p-i}K_{p-v} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -K_{i-i}K_{p-v} & 0 \\ 0 & -K_{i-i}K_{p-v} \\ -K_{i-v} & 0 \\ 0 & -K_{i-v} \end{bmatrix} \quad (18)$$

The gain and phase of the  $q$  synchronous axis output voltage with respect to the input are plotted in Fig. 6 and Fig. 7 respectively. The circuit parameters are the same ones used for the experimental set-up and are shown in Table I. The analytical model was used to tune the PI gains of the VSI controller. The same PI gains were used for all experimental measurements, regardless of the number of samples per switching period.

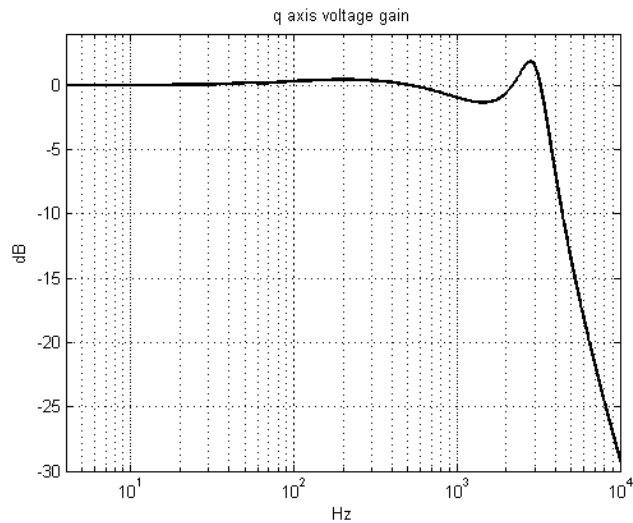


Fig. 6: Gain Bode plot of the transfer function  $\frac{v_{cfq}}{v_{cfq}^*}$  derived analytically.

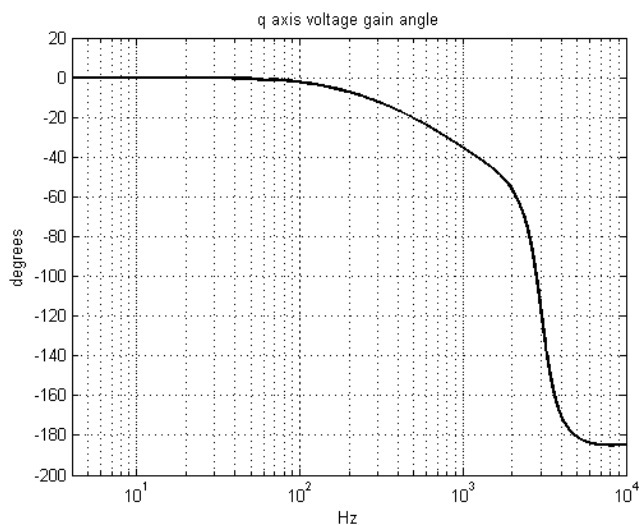


Fig. 7: Phase Bode plot of the transfer function  $\frac{v_{cfq}}{v_{cfq}^*}$  derived analytically.

Note that the model for the VSI assumes a unity gain transfer function for the “Space vector modulator” block shown in Fig. 5. This assumption is not exact when single or double update is used. In fact it has been shown that a

measurable phase delay exists, however this phase delay is dramatically reduced when multiple update rates, such as 16 or 20 are used [11]. Fig. 8 and Fig. 9 show the experimental measurements of voltage gain and phase delay for the block “Space vector modulator” in Fig. 5 [11]. In particular the phase delay shown in Fig. 9 is significant when single and double update rates are used, especially for higher frequencies. On the other hand higher update rates dramatically reduce the phase delay, thus making the unity gain model more accurate.

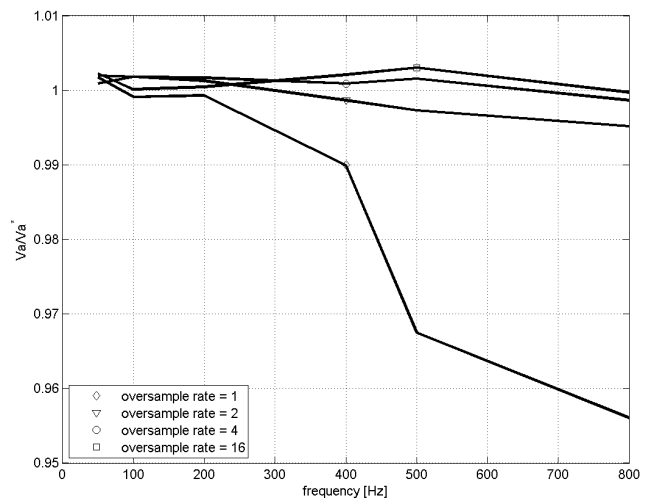


Fig. 8: Experimental measurements of voltage gain for the “Space vector modulator” block shown in Fig. 5 [11].

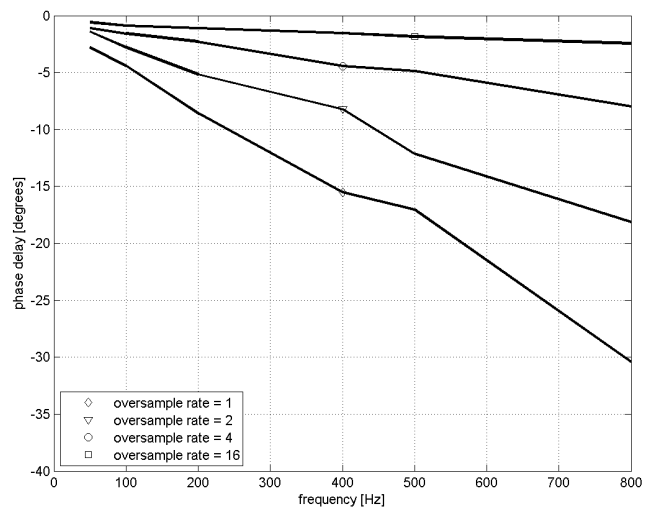


Fig. 9: Experimental measurements of phase difference for the “Space vector modulator” block shown in Fig. 5 [11].

#### IV. EXPERIMENTAL MEASUREMENTS

A VSI with an LC filter output and an inductive load was set up in the laboratory to show that the multiple sampling technique presented in this paper results in a significant

reduction of output voltage distortion. Fig. 10 shows the schematic of the laboratory set up. In the actual lab setup a  $1200\ \Omega$  resistor is in parallel with the load inductor. This is approximately equal to the inductive load case that was used to tune the pi controllers.

Double update space vector modulation was implemented as a benchmark and compared to space vector with 20 samples per switching period under the same conditions, including the controller gains. Table I shows the parameters and component values for the experimental measurements. Note that the load is inductive and very large to simulate no-load conditions. The operating conditions in the laboratory include expected distortion sources such as dead time, device voltage drop and DC bus voltage ripple.

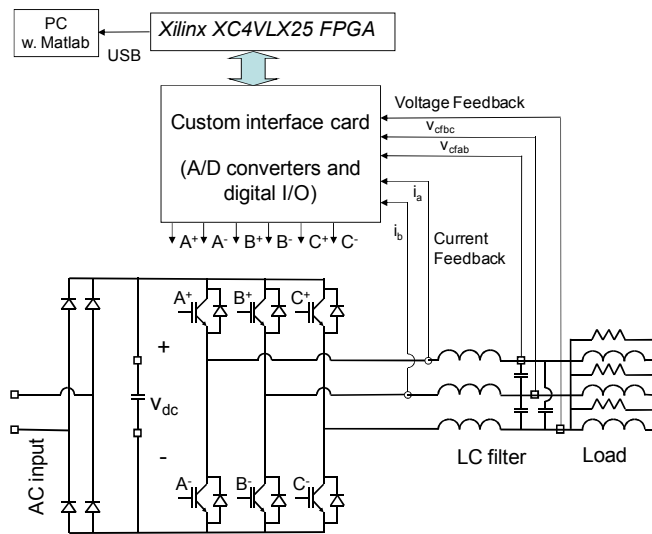


Fig. 10: Experimental set-up.

TABLE I  
PARAMETERS AND COMPONENTS IN THE EXPERIMENTAL SET-UP

Parameter name	value
Fundamental frequency	60 Hz
Switching frequency, $f_s$	10 kHz
Filter capacitance, $C_f$	6.6 $\mu$ F
Filter inductance, $L_f$	400 $\mu$ H
Load inductance, $L_o$	460 mH
DC bus voltage, $V_{dc}$	260 V

Fig. 11 contrasts the spectrum of the VSI output voltage (line-to-line, rms) when double update and when 20 samples per period are used respectively. Fig. 12 shows the zoom on the frequency axis. The average spectrum obtained with 20 samples lays clearly below the one obtained with double update all the way to the switching frequency where the two spectra are identical. This accounts for the increased controller bandwidth. The experimental data was acquired via USB interface and post-processed in Matlab. Three spectra were averaged to create each average spectrum. The case where the timers are re-computed 20 times per switching

period shows a clear advantage, with THD=1.71% compared to the THD=2.54% obtained with 2 computations (double update) per switching period. The THD was computed using the first 50 harmonics of the fundamental (60Hz), thus up to 3kHz, to capture the low frequency spectrum.

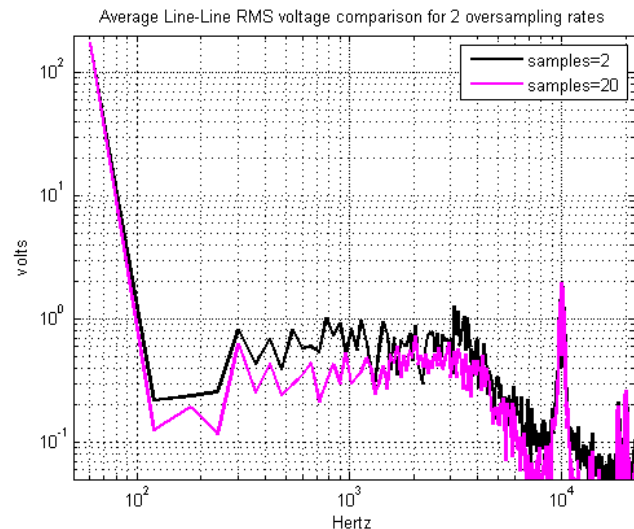


Fig. 11: Spectra of the line to line rms voltage: black is double update (THD=2.54%), magenta is 20 samples per period (THD=1.71%).

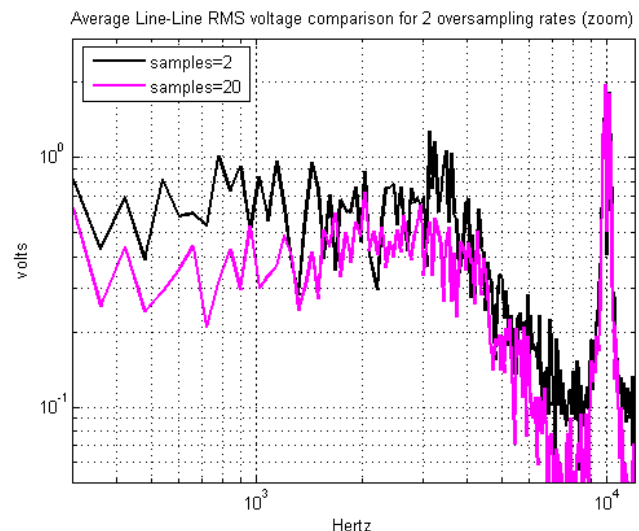


Fig. 12: Zoom on voltage amplitude and frequency axes of Fig. 11.

Fig. 13 contrasts the line to line output voltages of the VSI in the time domain for one sample of the two cases, double update and 20 samples per period. They are out of phase because the data acquisition trigger is random. The ripple on the voltage waveform is visibly reduced when 20 samples per period are used compared to the benchmark double update sampling technique.

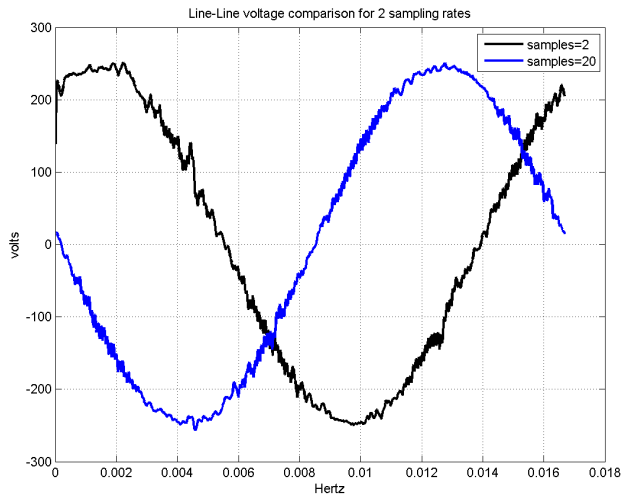


Fig. 13: Time domain waveforms of the VSI output line to line voltage.

## V. CONCLUSIONS

Embedding space vector modulation in an FPGA creates an opportunity to recompute the space vector timers multiple times during one switching period. This technique is often referred to as multiple sampling of the reference signal and can be implemented only if parallel computing is possible, as is the case with FPGA based controllers. This paper shows that the increased controller bandwidth, resulting from multiple sampling, is very beneficial for the output voltage quality. Bode plots created from simulations were used to understand the system gain and phase margins and tune the PI controller gains. Experimental time domain and frequency domain waveforms show the improved voltage quality of the VSI output voltage when 20 samples per period are used compared to typical double update space vector modulation.

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