

PROGRESSIVE AVIONICS PACKAGING TECHNOLOGIES

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ABSTRACT

Today's weapon systems are approaching a crisis with respect to avionics. More functions are being levied on aircraft systems. This increase in functional density increases the electronic component density. To meet the added functional requirements, electronic devices must shrink to allow more devices on a module and to allow processing/interconnection speeds to increase. This, however, produces a tremendous power density. This intensified heat load must be removed so that the components will remain reliable. The various device technologies are creating a coefficient-of-thermal-expansion mismatch, thus creating failures. The number of interconnections at the chip and system level must also decrease to increase system reliability. This paper describes technologies that address the packaging, cooling, and interconnect concerns for avionics that are applicable to current aircraft and future weapon platforms, as well as retrofit systems.

BACKGROUND

As avionics evolved from point design systems with line replaceable units (LRU) to modular designs with line replaceable modules (LRM), many benefits were obtained. Maintenance procedures were decreased, shrinking from a 3-level to a 2-level concept. The evolution of Very High Speed Integrated Circuitry (VHSIC) allowed more functions to be placed on a given module. Clock speeds were on the order of 250 MHz. Standardization was achieved by designing and developing common LRM's using VHSIC chip sets. Fiber optics permitted light weight, high speed (25-50 MHz) interconnects between integrated avionics racks (IAR) housing the LRM's. Reliability of avionics was increased by the use of liquid cooled IARs. This was obtained by lowering the junction temperature (T_j) of the chips and devices from 105° C to 85° C.

But as times marches on, weapon systems become more sophisticated, while their availability requirements become more stringent. More

avionics functions are required to be performed within the same volume and weight constraint. Thus power densities for LRMs increase dramatically. Today's typical LRM dissipates from 10-50 watts. However, future requirements will dictate that a given module generate between 100 and 400 watts. New techniques will have to be developed to cool these types of electronics. The LRM/IAR interconnect density is almost at its physical limit: 300-400 pins for a SEM-E module. Backplanes are also approaching a physical limit in terms of manufacturability and signal interconnect: 24-28 layers.

The R&M 2000 thrust dictates that weapons systems will have to operate at austere locations at sustained combat performance for 30 days at a time. The detrimental effects of the environment must be taken into account when designing avionics. Reliable systems must be developed, packaged, and cooled properly to meet these increasing stringent demands; all towards the end goal of reducing weapon system life cycle cost (LCC). Current and future technologies for all five packaging levels (chip, module, backplane, rack, system) must be pursued.

CURRENT TECHNOLOGIES

Packaging technologies can not be explored solely on a given level (chip, module, etc.). A total system look must be utilized. That way the effects of a new technology on one level can be examined to see its effects on other levels. Figure 1 shows one common problem across the chip/module/rack levels-thermal resistance.

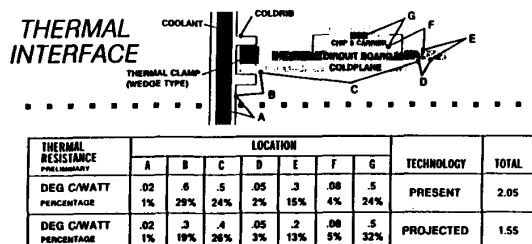


Figure 1. Thermal Resistance

Chip/Device Level

The days of transistors and integrated circuits (IC) have progressed to the current state of a device technology called multichip packaging (MCP). In this approach, individual naked chips are mounted on a separate interconnection substrate. Since both the chips and substrate can be individually burned-in and tested prior to assembly, testing is simplified and package yields are high. Packaging densities and electrical properties approach those of perfect monolithic wafer scale packaging and provide an additional advantage of supporting mixed technologies (GaAs, CMOS, Bipolar, etc). Devices can be obtained from different vendors, eliminating the need to design, purchase, and/or create all device masks. Costs are lower because one has only to design the MCP substrate and perform the chip attachment. Faulty chips can be removed and replaced, and errors in the interconnect wiring are more easily corrected.

MCP substrates are fabricated by depositing conductors and dielectrics on metals, ceramics, or silicon using a process very similar to conventional IC fabrication. A leading material for the interconnection substrate is silicon, as the processing is compatible with existing IC lines. Silicon has excellent thermal conductivity and naturally matches the coefficient of thermal expansion of most devices. In addition, it provides excellent surface flatness and is well suited for flip-chip attachment. Substrate designers have shown great inventiveness in fabricating and assembling silicon-on silicon multichip packages.

Flip-chip assembly allows chip to be mounted as close as 10 mils apart. This dense packaging results in very short chip-to-chip signal leads and low capacitive loading. Typical line widths and spacing are 10 microns, with 2 micron line thickness. Chip to substrate inductance is only 0.1H, with a 70 ohm transmission line characteristic impedance. Packages have been fabricated that achieve greater than 1 GHz clocking without line terminations, providing substantial power savings. Active devices such as by-pass capacitors, buffers and drivers can be fabricated as part of the interconnection substrate providing additional packaging and reliability gains. Different device types (GaAs, Bipolar, CMOS) can be interconnected on the same substrate. These MCP's can be functionally developed such that a family of MCP's can be the next level of standardization (one level down from the module level).

Military electronic components have been traditionally hermetically sealed to protect the delicate electronics against the elements (moisture, radiation, etc.). However, hermetic packages are expensive to develop, with large (> 1 in 2) packages costing up to a quarter of

a million dollars to develop and test. An alternate approach to hermetic sealing is protective encapsulation. Dielectric materials such as silicon dioxide and silicon nitride provide first level passivation/moisture protection, while conformal overcoating with organic encapsulants such as epoxies, silicones, polyimides, and paraxylene provide the primary environmental protection. Encapsulants have been developed that minimize thermal expansion mismatch problems, and damage to flip-chip solder joints during application. In addition, they provide good solvent resistance and repair capabilities.

Module Level

Electronic devices are mounted on printed wiring boards (PWB) which are usually mounted on an aluminum coldplate. This plate is 1/8" thick and weighs about 1 lb. Heat is removed conductively from this module to the IAR. But the denser-packed devices such as MCP's require more heat to be dissipated, and at the same time, weight poses a problem. The need for better heat removal, coupled with weight and CTE problems have spurred the development of alternate frame materials. Some of the frame materials that are actively being investigated are carbon/metal composites, copper/moly/copper, beryllium, and copper/invar/copper. (See Figure 2). In addition, frames are evolving to complex metal matrix and flow-through designs. Solid frame designs minimize stack thickness, but require excellent x-y thermal conductivities in order to move heat from the chip to the cooling medium. A number of researchers are working with metal matrixed graphite frames. These frames have excellent rigidity and vibrational damping. They are light in weight, and can be tailored to match thermal requirements. Graphite composites have had some problems with metal bunching and delamination, but recent results are encouraging. With solid frames and edge conduction, liquid-cooling should prove satisfactory for modules up to 50 watts, with the wedgelock/clamp being the limiting factor. However, high power dissipations may necessitate fluid flow-through techniques. Flow-through modules can significantly improve thermal resistivity by bringing the cooling medium closer to the heat source. The major problems associated with this approach are the design of a cooling medium connector, clogging and increased frame thickness. Preliminary analysis indicates that fluid flow-through modules could provide reliable cooling for modules with heat dissipations close to 200 watts.

To reduce the number of LRM/IAR interconnects, signal pins are being replaced with fiber optic termini. This allows signals to be transmitted at higher rates (100 HMz) without the problems associated with dense electrical pins (resistance, capacitance, etc.). To reduce pin counts even further, multiplexed lens

connectors have been developed and are being miniaturized (about 1/4" diameter) to fit LRM connectors. This could possibly reduce the 300 to 400 signal pins to about 10 lens connectors.

Material with the lowest Overall Rating is the most desirable.									
Material	Thermal Rating	Thermal K	Weight Rating	CTE ^{xx} x10 ⁻⁶	YF	Stiffness Mod. of Overall Rating	Mod. of Overall Rating		
Copper (pure)	1.0	401	4.9	.324	4.6	9.1	11.0	16	248
P140 Gr/Alum	1.4	288	1.6	.108	1.0	2.0	3.0	20	6.7
P120 Gr/Alum	1.7	226	1.3	.088	2.3	4.6	2.1	23	11
P100 Gr/Alum	1.9	208	1.4	.090	2.0	3.9	2.0	25	11
P75 Gr/Alum	2.7	150	1.4	.091	2.0	3.9	2.0	18	21
NX-5221 (silicone carbide)	2.5	160	1.6	.109	2.0	3.9	1.9	32	15
NX-5251 (silicone carbide)	2.7	150	1.5	.100	2.7	5.3	2.0	28	22
Aluminum (Pure)	1.7	237	1.5	.098	6.5	12.9	5.5	10	91
Aluminum (6061-T6)	2.3	171	1.5	.098	6.8	13.5	5.5	10	129
Copper Moly Copper (12.5/75/12.5)	2.0	200	5.4	.358	1.6	3.14	6.0	35	104
Copper Invar Copper (20/80/20)	2.4	167	4.7	.308	1.5	3.0	10.0	18	169
Copper Invar Copper (12.5/75/12.5)	4.0	100	4.6	.304	1.5	3.0	9.0	19	248
Tungsten	2.3	174	10.6	.697	1.2	2.4	9.0	50	234
Beryllium	2.0	200	1.0	.068	3.4	6.8	1.0	37	6.8
Molybdenum	2.9	138	8.6	.369	1.3	2.6	4.0	50	85
Titanium	18.3	21.9	2.5	.164	2.0	4.0	5.0	17	458

Figure 2. Module Coldplane Material

Backplane Level

Highly integrated avionics systems use backplanes that can interconnect between 30 and 90s SEM-E modules. These backplanes will provide all power and signal connections, including multiple 32-bit bussing and complex switching networks. These backplanes range in size from one to five square feet, incorporate several thousand nets and upwards of 25,000 connections, have between 24 and 28 layers, and contain over 20,000 vertical plated through holes (PTH). The z-axis coefficient of thermal expansion (CTE) becomes increasingly important as the backplane thickness and PTH aspect increases. A poor z-axis CTE match can lead to problems such as barrel cracking, foil cracking, pad lifting, and holewall pull away. Backplane transfer rates range between 12.5 and 25 megawords per second. The design and manufacture of highly reliable backplanes capable of meeting these challenging requirements require technological advances in the areas of resin and material fabrication, connector technology (including optical), inspection, and active circuitry. The two most common backplane material in use today are glass epoxies (Quatrex, BT) and polyimides. Glass epoxies are well established, mil-qualified materials that provide good availability and manufacturing properties. They are somewhat inferior to polyimides in terms of glass transition temperatures (affects dimensional stability), z-axis CTEs, and dielectric constant. Polyimides, on the other hand, are difficult to drill due their brittle nature. This is an important consideration when one has to accurately drill tens of thousands of holes. Cyanate esters are relatively new backplane materials with excellent all around properties and may well be the backplane material of the future. Unfortunately, it is still a relatively high cost material and has yet to be mil-qualified.

To further reduce weight and increase bandwidth, optical backplanes have been developed. It is currently a combination of a sandwiched electrical backplane and an optical backplane. (See Figure 3). The optical fibers are encapsulated as ribbon cables in polyurethane to back of the electrical backplane. A limiting factor to this design is the bend radius of the fiber out of the backplane connector. Depending on the connector vendor this varies from .47" to .85".

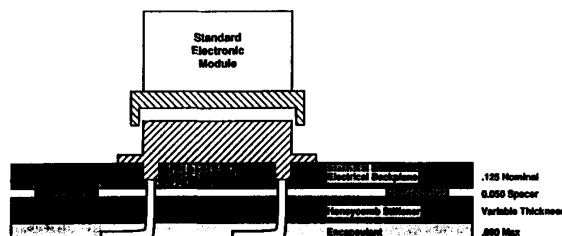


Figure 3. Optical Backplane

Most of the work to date has concentrated on the backplane/materials for digital avionics. However, improvements have been made in the RF domain. Embedding coax cable within the backplane is a recent development (See Figure 4). This has several R&M benefits. First the number of parts is reduced because many individual coax runs are replaced with a plate. Parts reduction increases reliability. Secondly this is front removable. Front removal aids maintainability. Isolation of 80-90db can be achieved between adjacent embedded coax lines (.086" diameter) up to 5GHz. Routing is flexible as radii can be bent as tight as .5" OD.

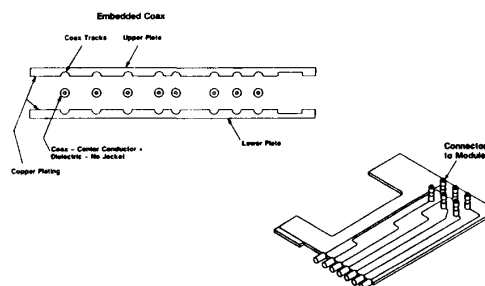


Figure 4. Embedded Coax Backplane

Rack Level

Previous avionics generations that were cooled by air (either by conduction or directly over the components) have given way to liquid cooling in the rack (conduction to the LRM). This unfortunately has a limitation by cooling

only low powered modules (10 - 50 watts). A new system has been designed, developed and tested that allows for liquid flow through modules. This has greater cooling capacity since the coolant is brought into the centerplate of the module, thus reducing thermal resistance paths between the coolant and the electronics (See Figure 5). LRMs that dissipate up to 200 watts can now be cooled. The weight penalty associated with this concept is minimal. The compressors for this system are the same as for a regular liquid cooled system. The fluid type is also the same polyalphaolefin (PAO). The only additional weight comes from the fluid in each module-about two tablespoons. The reliability benefits gained clearly offset their weight penalty.

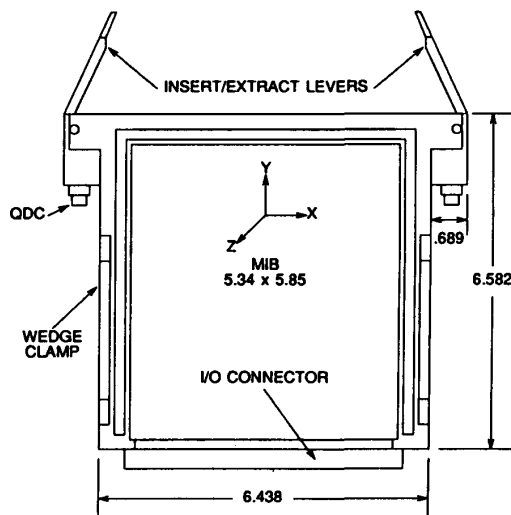


Figure 5. Liquid Flow-Through Module

Most IARs consist of 6061 aluminum. This is a strong, "light weight" metal rugged enough to meet military requirements. However, to reduce total aircraft weight, other materials are being used. The standard aluminum fin stock for the rack coldplates is being replaced by reticulated aluminum foam. The aluminum rack structure is being replaced by graphite/epoxy materials, or with a combination of a plastic foam material and an aluminum foil coating. Covers/doors are also being constructed with the same substance.

System Level

The technologies applicable to system level packaging have not progressed as much as the other levels, as they have not been pursued as aggressively. Areas under current research include fiber optics (backplanes and high speed/high bandwidth switches), smart cooling

(micro processor controlled), and distributed cooling (federated compressors vs one single environmental cooling system).

THE FUTURE

The future for avionics packaging must still yield to the continuing requirements of denser devices, lighter weight, higher processing/interconnect speeds etc.

SEM-E/IAR

For the last decade, process and packaging engineers have attempted to achieve denser packaging and faster chip-to-chip communication through wafer scale integration (WSI). Wafer scale integration is a monolithic approach to interconnection in which chips and their interconnection circuitry are fabricated as a single wafer structure. This approach promises excellent speed, packaging density, and thermal management. Reliability would improve dramatically since large numbers of solder joints and pad drivers would be eliminated. Unfortunately, this approach has several drawbacks. The size and complexity of a monolithic structure is ultimately limited by the presence of defects, making the economic production of large structures a difficult problem. Since repair was difficult (if at all possible), redundant devices and interconnection circuitry must be integrated into the structure, negating many of the packaging and performance gains. WSI also limits the types of chip technology that can be interconnected and requires the fabricator to design/purchase all chip asks and interconnection circuitry. However, WSI must be pursued and perfected to help meet future avionics packaging requirements.

With the advent of denser device packaging (MCP's, WSI, 3-D stacking, etc.) LRMs will need to dissipate as much as 400 watts. The likely cooling candidate for this problem is liquid immersion cooling, where the devices are actually bathed in a liquid. This substance must be inert so that it doesn't react with the electronics. Chlorofluorocarbons (CFC) will meet this requirement but are heavy, expensive, and harmful to the environment. Further research is required here.

One of the impedances to good thermal management is the thermal resistance between system levels. One of the largest is the interface between the LRM rib and the IAR rib. (See Figure 1). The standard thermal clamp is the 5-section wedgelock. This is cumbersome for module insertion and extraction (I/E), and its thermal efficiency decreases with the number of I/E's. A better thermal clamp would be a "thermal straw" - a thin walled copper tube filled with CFC liquid (See Figure 6). In the relaxed state, the oval shaped cross section would allow the module to slide in and

out of the rack. In the compressed state the force of the conductive fluid pressing the copper against the rib makes for an ideal thermal interface and reduces the thermal resistance by a factor of 2.

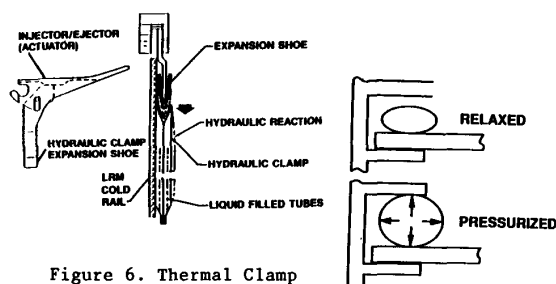


Figure 6. Thermal Clamp

To aid specifically with retrofit situations, a distributed cooling technique can be employed. In this concept a miniature compressor (100,000 rpm) would be embedded in each IAR. This way each rack would be individually cooled, and not depend on the system (in which most cases only air-cooling is available). Phase change materials (such as Freon) could be used for this. A system has been designed in which the Freon (or equivalent due to environmental concerns) flows through serpentine channels in the rack rib, thus bringing the coolant as close to the module as possible. Initial tests show that 106 watt modules can be cooled with T_j of 65° C.

Optical interconnects (I/C) are a must to decrease weight and increase signal speed. Optical I/C's at all levels, especially within chip and chip-to-chip need developed.

Other

Now if we can deviate slightly from the present packaging standards of SEME and IAR, there are other avenues worth exploring. If we move away from the "flat board module" using edge connections, to a solid shape like a "cube" or rectangular solid, we can increase the surface area available for thermal and I/O connections. These new concepts must be in concert with conformal packaging/smart skins and must include the new wafer stack and chip on board component configurations.

A more volumetrically efficient "Functional Module" configuration, a primary departure from the technology of today is replacement of the large flat board with signal and power I/Os on one edge and cooling on two edges, with a module in a more "cubic" shape. In this concept, the six faces are divided to use two surfaces for I/Os, two surfaces for cooling and the remaining two surfaces for structural positioning and support. In this concept the surfaces used for both I/Os and for cooling are

increased with respect to the surface area used for active components.

Figure 7 shows an expansion on this concept. The inside of this six-surface, rigid-flex-rigid assembly is used for attachment of the raw chips, hybrid substrates, or wafer stacks. When folded into the cubic shape the sealed internal cavity can be used as an isothermal bath for removal of the heat to the cold plane with a minimum delta temperature at high thermal fluxes. The outer surfaces of this cube are tailored to function in pairs as the I/O, thermal, and structural support planes. The area provided for I/O and thermal transfer are a higher percentage of the circuitry volume than the present flat board module.

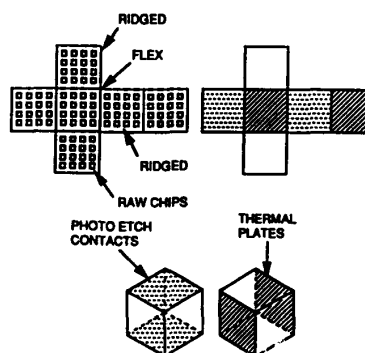


Figure 7. Cube Geometry

Figure 8 shows a packaging concept for application of avionics to a compound curved surface such as would be required for aircraft skin mounting. These avionics would be used in conjunction with surface mounted sensors and the system could be referred to as conformal avionics. In this concept the entire sensor/amplifier/processor could be mounted on a removable panel of the aircraft body skin or wing leading edge. This, by definition, becomes "remote electronics" as it is no longer a part of the "core avionics." By placing the processor at the site of the sensor, the interconnection to the core avionics and/or the cockpit display is reduced, but the cooling is complicated and will require added plumbing and coolant from the environmental control system (ECS). The thermal management is exacerbated by the added aerodynamic heating at the skin. To meet the ravages of this hostile environment, the structural supporting skin needs to be thermally insulated from the electronics assembly and its coolant. To meet the conformal shape the interconnection plane must be "faceted" with flat surfaces required by the individual chips, substrates or hybrids and the cooling should be provided by the isothermal coolant bath that is insensitive to the curved shape of the enclosure. Assuming there will be space limitations in these

applications, the coolant lines and I/O cables can be brought out at either the edge surfaces or on the inside surface.

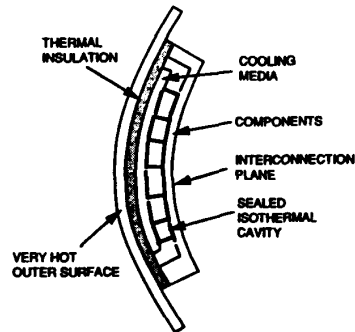


Figure 8. Conformal Avionics

If these advanced packaging technologies can be examined thoroughly (given enough time and money), then the ultimate packaging scheme to reduce power, weight and volume can be achieved. A given complete function (from sensor front end through video processing) can be placed on one highly reliable, easily removable aircraft panel. But beware—other extremely important issues such as manufacturability must also be studied in order to accomplish this goal in a practical manner.

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