FAULT COVERAGE MEASUREMENT FOR ANALOG CIRCUITS

E. Paul Ratazzi

Reliability and Diagnostics Branch
Rome Laboratory
United States Air Force
RL/ERDA

Griffiss Air Force Base, New York 13441-5700

Abstract

This paper describes an effort to develop a technique for measuring the amount of fault detection coverage that an analog test pattern has for a particular analog device. The technique is based on a software tool which statistically analyzes data from a circuit simulator. One example of a fault simulation experiment is presented, and some of the results are discussed. Finally, a look at the future of Rome Laboratory (RL) work in this area is given.

Introduction

Measurement of a test pattern's fault coverage plays an important role in the specification of complex digital microcircuits. Unfortunately, analog test engineers have not enjoyed the same benefit of being able to quantify how well a test pattern detects faults. This unfortunate fact can be attributed to the nondeterministic nature of analog signals and the inability to represent physical faults in a small number of fault classes (for example, stuck-at faults represent a large number of physical faults in digital logic circuits). Other factors which have prohibited meaningful measurement of fault coverage in analog circuits include the effect of nominal component variations on circuit response, the lack of mature analog simulators, and the wide variety of circuit functions that exist. In most cases, the development of a thorough test pattern for even simple analog circuits is based on an ad-hoc collection of sometimes redundant tests. Test specifications are developed based on the circuit's *function*, without regard to the circuit's *architecture*. Increases in the complexity of analog microcircuits and the advent of analog application-specific integrated circuits (ASIC), are pointing to the need for being able to quantify test quality and develop test patterns which account for circuit topology.

Background

Fault analysis of analog circuits has been an active research area for many years. Literature surveys¹ show that the Department of Defense (DoD) has held a small but steady interest in this area since the beginning of the 1960s. Early efforts were designed to ease the task of isolating component failures on circuit cards containing analog circuitry. Later efforts had goals ranging from fault-driven automatic test pattern generation (ATPG) to built-in self test (BIST). Recent RL involvement in this area has been with more general goals in mind. First, to develop an understanding of the basic problems associated with the simulation of faults in analog circuits, and second, to investigate various methods of fault analysis. In May 1989, RL awarded an eighteen-month contract to David Sarnoff Research Center (DSRC) to research the state-of-the-art and develop a specific technique of analyzing analog circuit faults. The result is the methodology embodied by the Statistical Fault Analyzer (SFA).^{2,3}

SFA Basics

The SFA is a software tool which provides data analysis and circuit faulting capabilities to a circuit simulator such as SPICE 3C1. It consists of a preprocessor which directs the simulation according to a set of control statements included in the simulator input file. These control statements describe how the circuit is to be faulted, the number of simulations to be run, and what information will form the output file. Gaussian component variations are specified by allowing any numerical value in the SPICE input (except node numbers) to be replaced by a mean and standard deviation value. The SFA also contains a post-processor to collect and format the output from the simulation. The SFA can post-process any numerical result of the simulation including nodal voltages, branch currents, frequency re-

sponse, and transient data. The resulting files may be analyzed using two different statistical methods: hypothesis testing for fault detection and discrimination analysis for fault classification. For the purposes of this discussion, only hypothesis testing (fault detection) will be discussed.

Hypothesis Testing

For hypothesis testing, the SFA generates a data file containing simulation results for an unfaulted circuit. It usually contains many entries, each one slightly different due to component variations introduced through Monte Carlo methods. The data file is a multivariate distribution representing the circuit's unfaulted behavior. This distribution forms the basis for the null hypothesis, H_0 , which states that the circuit is good or unfaulted. When simulation results from a faulted circuit are presented to the SFA, a hypothesis test is used to calculate the probability that the faulted response lies within the unfaulted distribution. If this probability is less than a predetermined threshold (confidence level), H_0 is rejected and the fault is detected. Otherwise, H_0 is incorrectly accepted, indicating that the fault may be undetectable. Incorrect acceptance of H_0 is known as a Type II error and may be due to a truly undetectable fault or an ill-defined unfaulted distribution. Consistent rejection of H_0 , allowing for the expected number of Type II errors, indicates that the faulted circuit's response is distinguishable from the unfaulted circuit's response. When this is the case, the fault is detectable and the test that achieved the detection is said to "cover" the fault.⁴

Fault Detection Coverage

Fault detection coverage is a measure of a test method's ability to detect faults in the device under test (DUT). For analog circuits, a test method defines the forcing functions applied to the DUT and specifies the external test circuitry used. Analog fault detection coverage is dependent on the test pattern, the faults selected, and the test circuit. Thus, any measure of fault detection coverage for analog circuits must specify the entire test method, as well as the fault set used. Fault detection coverage is reported as a ratio of the number of detected faults to the total number of faults possible in the DUT. In the most general sense, the total number of faults possible would include combinations of individual faults, resulting in an astronomical number of circuit states. For simplicity, this investigation considers only "one-at-a-time," or singly-inserted faults.

Experiment Description

For this study, the hypothesis test routine contained in

the SFA is used to determine if it is possible to measure the amount of fault detection coverage that specific analog test methods have for a given analog circuit. Before the actual experiment and results can be discussed, elements of the setup must be described. The elements used for this experiment include the DUT, the test circuit, and the fault set.

DUT Description

The DUT used in this experiment is a commercially available macrocell operational amplifier (MOPA). This macrocell is a part of the Raytheon Linear Array (RLA) series of analog ASICs. The selection of this device as a test case is based on two main factors. First, analog ASICs present an acute challenge with respect to developing quality tests. With standard single analog functions, it may be acceptable to have a function-driven, general-purpose test pattern that contains testing redundancies. However, when these functions are combined into large specialized circuits, as is the case with many analog ASICs, it is no longer acceptable to have an inefficient test pattern. Components of the test pattern must provide the most "bang for the buck" and be as independent as possible regarding the information provided about the state of the circuit. At the same time, they must together give a complete and accurate evaluation of the DUT. In choosing the MOPA as the test case, it was recognized that in order to assess test quality for combinations of these functions, one must first master assessment of individual functions. The second reason for selecting this particular family of circuits is that they have a strong relevance to analog military microelectronics. The RLA family of devices is the first analog semi-custom parts to achieve qualification under the Joint Army-Navy (JAN) MIL-M-38510 specification system for microcircuits.⁵ This

Figure 1. D.U.T. Transistor-level Circuit.⁶

Test	Test Pattern ($V_s, K1, K2, K3$)	Measure Point (fig. 2)
V_{OS}	0V, closed, closed, open	A
I_{OS}	0V, open, open, open	A
$+I_{IB}$	0V, closed, open, open	A
$-I_{IB}$	0V, open, closed, open	A
AV	0V, closed, closed, closed	A

Table 1. Test Pattern Description.

specification opens the door for widespread use of these devices in military systems. For this reason, it is in our best interest to seek better means of evaluating test quality for these devices. Figure 1 shows the MOPA internal architecture.

Figure 2. Test Circuit Containing D.U.T.

Test Circuit Description

In analog testing, the test circuit plays an extremely vital role in determining if faulty DUT behaviors are propagated to the measurement points. In fact, the test circuit is every bit as important to fault coverage as the test pattern is. For this reason, the test circuit must be grouped along with the DUT for any fault simulations. The test circuit selected for this investigation is a simplified operational amplifier test loop, such as those found on MIL-M-38510 analog detail specifications and in MIL-STD-883 analog test methods. The main point that distinguishes the DUT and the test circuit during simulation is that the DUT must be modeled structurally so that component faults can be inserted, whereas the test circuit may be modeled behaviorally or as a macro model since it is assumed that the test circuit contains no faults. Additionally, we assume that the test circuit is fixed and cannot be altered as a way of increasing fault coverage. However, note that alteration of the test circuit may very well be an excellent method of increasing fault coverage. A

schematic of the test circuit containing the DUT appears in figure 2.

The schematic of figure 2 shows the DUT in a standard operational amplifier test circuit. Input patterns to this test circuit consist of applying a forcing voltage at V_s and opening or closing relays K1, K2, or K3. The output is measured at test point A. The tests that were implemented and their associated test patterns are shown in Table 1. Due to computational limitations, a full operational amplifier test suite was not applied, but will be in future investigations.

Fault Set Selection

Selection of a realistic fault set for analog circuits (and perhaps for high-speed digital circuits) is a very difficult process. Very limited data is available on the types of faults which commonly occur in these circuits. For example, an Air Force study⁷ reports that 32% of IC failures are due to opens, 22% are due to shorts, and 18% are due to parametric or "soft" faults such as low gain. However, no breakdown is given for the type of structure or type of device (analog or digital) that the faults occurred in. Also, this data comes from field failures and may not be comparable to manufacturing defect data. In an attempt to remedy this situation, an RL effort⁸ is underway which is exploring the possibility of utilizing microcircuit defect simulators to generate a list of manufacturing faults prioritized by probability of occurrence. At the present time however, this approach is not well-defined and in this experiment the fault set selection was based solely on reasonable engineering judgement. For each transistor of the DUT, seven faults are considered. Each transistor lead (base, emitter, collector) can be shorted to each of the two remaining leads (3 faults), each lead can have a high resistance (3 faults), or the transistor's forward current gain (β_F) can be low (1 fault). This makes a total of 91 faults possible throughout the circuit. Note that this fault set is not intended to represent the actual faults that can occur in this device. It is used only for proof-of-concept purposes until a more realistic fault set can be developed.

Simulation

Once the DUT, test circuit, and fault set have been defined and coded into the SFA input format, fault simulations may be run. For fault detection coverage analysis, which uses the basic hypothesis test, the circuit's nominal behavior must be defined. In this case, the unfaulted circuit is simulated a total of 100 times while introducing a 10% normal variation into each transistor's forward current gain (β_F) and Early voltage (V_A). Previous sensitivity analyses¹ show that these two parameters have the most significant effect on transistor performance. The circuit is then simu-

lated 100 times for each single fault condition. A hypothesis test is performed after each simulation. This procedure is iterated for each test condition considered. Results of the fault simulation indicate how many times H_0 was accepted or rejected for each fault and test condition.

Initial Results

Results to date have shown many examples of faults that are detected by one test pattern, and not another. For example, simulations show that the offset voltage test (V_{os}) cannot distinguish between the nominal circuit and the circuit with a short inserted between the collector and base or collector and emitter of transistor Q5 (see figure 1). This is apparent from fault simulations where the V_{os} test correctly accepts H_0 94% of the time when the circuit is nominal, yet incorrectly accepts H_0 92-95% of the time when the faults are present. On the other hand, the offset current (I_{os}) test is able to detect these faults by causing the fault to propagate to the circuit output. I_{os} also correctly accepts H_0 during unfaulted runs, but rejects H_0 100% of the time when the faults are inserted. One can conclude from this that the I_{os} test has fault detection coverage for these faults, while the V_{os} test does not. Expanding this methodology to an entire test sequence for an entire fault set yields a measure of fault detection coverage or test quality.

Future Investigations

Continuing work sponsored by RL will focus on two main areas. First, contractual efforts will focus on refining the SFA methodology and researching practical methods of defining a fault set for a given circuit. Second, in-house work will continue to concentrate on using the SFA tool to define techniques for measuring fault coverage. Eventually, it is hoped that these measurement techniques will be standardized in the same way that digital techniques have been in MIL-STD-883, Procedure 5012: "Fault Coverage Measurement for Digital Microcircuits."

Conclusions

Initial results from an analog fault simulation experiment show that it is possible to measure the amount of fault detection coverage that a specific test method has for a given analog circuit. The method requires a transistor-level model of the DUT, a model of the test circuit, and a fault set in terms of component value or model parameter value modifications. Fault detection coverage is measured by taking the ratio of the number of faults detected by the hypothesis test to the total number of faults in the fault set. Additional work is needed in defining a realistic fault set

and in extending the method to a complex analog ASIC containing many function modules.

References

1. B. R. Epstein, "Linear Microcircuit Fault Modeling and Simulation (Interim Report)," *RADC-TR-90-30*, Rome Air Development Center, Griffiss AFB NY, April 1990.
2. B. R. Epstein, M. H. Czigler, and S. R. Miller, "Linear Microcircuit Fault Modeling and Simulation (Final Report)," *RL-TR-91-106*, Rome Laboratory, Griffiss AFB NY, June 1991.
3. B. R. Epstein, S. R. Miller, M. H. Czigler, and D. R. Gray, "Linear Microcircuit Fault Modeling and Detection," in *Digest of Papers, 1991 IEEE VLSI Test Symposium*, April 1991.
4. B. W. Johnson, *Design and Analysis of Fault-Tolerant Digital Systems*, Reading, MA, Addison-Wesley, 1989.
5. E. P. Ratazzi, "A Military Specification for Linear ASICs," in *Digest of Papers, 1988 Government Microcircuit Applications Conference*, November 1988.
6. *RLA Series Linear Array Design Manual*, Raytheon Company Semiconductor Division, Third Edition, 1989.
7. U. S. Air Force, Rome Air Development Center, "Microcircuit Device Reliability, Hybrid Circuit Data," *GIDEP Report No. 518.00.00.00-F9-03 (E073-2214)*, 1976-1977.
8. E. P. Ratazzi, "Statement of Work for Analog Microcircuit Fault Prediction," in *Purchase Request N-2-5723*, Rome Laboratory, Griffiss AFB NY, September 1991.
9. W. H. Debany, K. A. Kwiat, H. B. Dussault, M. J. Gorniak, A. R. Macera, and D. E. Daskiewicz, "Fault Coverage Measurement for Digital Microcircuits," *Test Procedure 5012 of MIL-STD-883 (Notice 12)*, Rome Laboratory, Griffiss AFB NY, 27 July 1990.