A NAVY PLAN FOR THE DEVELOPMENT OF A PRACTICAL COMPUTER-AIDED PROGRAMMING (CAP) SYSTEM FOR ANALOG CIRCUIT TEST DESIGN

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Abstract

This paper addresses some of the problems inherent in the development of Test Program Sets (TPS) required to apply automatic test equipment in support of Navy avionics. It then outlines a 3- to 5-year R&D Program to develop a Computer-Aided Programming (CAP) System which would improve quality and reduce costs over the current manual processes for producing TPS for avionics containing analog circuitry. Since the R&D effort is just beginning, only the initial tasks are described.

INTRODUCTION

Originally introduced for cost savings, Automatic Test Equipment (ATE) has proven to be more effective as a mission extender than a cost reducer. Thanks to ATE, avionics systems far more complex than originally predicted for the 1970's are being successfully maintained on naval vessels rather than being discarded or returned to a depot for repair as originally planned. During a time when avionics complexity has increased tremendously, driven by both aircraft mission sophistication and substantial advances in electronics technology, the use of ATE as a maintenance tool has enabled the fleet to continue its tradition of repair-on-board. In fact, ATE has given the fleet maintenance procedures a degree of precision and objectivity previously not available even in the depot.

But, from the total Navy support viewpoint, ATE has added a new dimension of complexity due to its dependence on Test Program Sets (TPS). A TPS consists of (1) a test program, containing the testing sequence and logic required to evaluate and fault isolate the Unit Under Test (UUT), (2) an Interface Device (ID), enabling the UUT to be connected to the ATE, and (3) a Test Program Instruction (TPI) booklet directing the ATE operator in his role. TPS are required for all ATEs, whether special purpose Peculiar Ground Support Equipment (PGSE), or multipurpose Common Ground Support Equipment (CGSE), such as the Versatile Avionic Shop Test (VAST).

The need for procuring expensive TPS concurrently with aircraft along with the usual Ground Support Equipment (GSE) has put a tremendous strain on the Navy's buying power, even though in the life cycle

of application, ATE is truly cost effective. Fortunately, the computer, which has made ATE practical, also has the potential to make it affordable. Computers are successfully assisting Navy contractors today in the development of digital test programs for the F-14, E-2, and S-3 aircraft. The process of computer-aided test program generation for digital circuits is being refined continually and offers even better prospects for cost reduction in applications such as the future support requirements of the F-18 aircraft.

Unfortunately, the immediate prospects for computer-aided test design for analog circuits is not nearly so promising. A detailed study of avionics on board modern Navy aircraft revealed that a typical avionics suit such as for the F-14, E-2, or S-3, contains in excess of 60 unique weapon replaceable assemblies (WRA) and 1,000 shop replaceable assemblies (SRA). Sixty percent of the avionics aboard such aircraft consists of analog circuitry. Much of the remaining 40% is hybrid and thus involves some analog testing. Even the purely digital circuitry sometimes requires parametric measurements which are of an analog nature. Hence, while analog testing is still a major requirement, almost all recent advances in the state-of-the-art have been in the digital field with very little progress in improving analog testing or test generating techniques.

TPS ARE THE ATE COST DRIVERS

Experience shows that the TPS costs for a typical ATE application greatly exceed the system hardware costs. But, separating out the cost of TPS from the myriad of GSE acquired to support an aircraft is at best a difficult task. Data is simply not available to determine the nonrecurring acquisition cost of any given TPS. However, the Navy has gained substantial experience in TPS. It has been buying large quantities of TPS since the early 1970's. Since that time, the Naval Air Engineering Center has participated in a very intensive technical monitoring effort at several aircraft manufacturing sites. Although not assigned to monitor costs, some financial data does come to the engineer's attention. Also, total costs for batches of TPS are traceable in procurement documents. From such information, it is clear that the Navy has been paying an average price of about \$500,000 for the nonrecurring development of a WRA

TPS and about \$50,000 for an SRA TPS. These prices seem independent of the chosen tester but primarily dependent on the complexity of the UUT and the degree of confidence and fault isolation demanded by the Navy.

While it may be hard to justify these high costs, they seem to be the going prices for TPS of the quality required by the Navy, based on contracts with several aircraft manufacturers. It is clear that TPS development is a labor-intensive process. Most of the nonrecurring costs are consumed in acquiring data on UUT performance and for engineering labor used in developing and validating test programs.

The TPS design process as currently practiced is totally dependent on data from the UUT manufacturer, who is generally not the prime contractor. The integrity of that data is always suspect and generally changes substantially during TPS design. Hence, the product is the subjective design of one engineer, even though he might be supported by many other people. Evaluating such subjective designs is nearly as time consuming as the design effort and often more difficult. So sampling is the only approach possible. The biggest problem is that, despite intensive evaluation during development, no true assessment can be made of the capability of the TPS to perform effectively in the fleet prior to actual deployment. Finally, making changes to TPS is extremely difficult for anyone other than the original design engineer. In extreme cases, where the original test designer is no longer available, some test programs have to be redesigned completely in order to implement a change resulting from an avionics engineering change.

DIGITAL TEST EXPERIENCE

The early designs of TPS for digital UUT's involved the same human analysis of the circuits and their testing requirements as has been applied in analog testing. The complexity of the problem,

however, exceeded the analog test requirements by more than 10 to 1. The sheer quantity of signals involved in a digital test makes human analysis excessively long, costly, and error prone.

It was soon learned that a much more practical approach involved modeling the circuits using a computer program to derive the testing patterns and evaluate failure modes. It took a substantial investment to develop and apply the Navy Logic Automated Stimulus and Response (LASAR) modeling system, but now it is fully operational. An evaluation of several UUT programs of medium complexity that had been prepared manually were modeled on LASAR and evaluated. Those prepared manually were found to be between 30 and 40% effective in determining whether a UUT was good or bad. With LASAR, this capability was increased to over 85%. The effort involved when using LASAR is also substantially reduced. Unfortunately there is no cost breakdown information with which to determine actual costs in either case, but knowledgeable opinion indicates a TPS cost saving of between 25 and 50% using computer-aided test design tools such as LASAR. At least 50% of the test design portion of TPS development is saved using computer-aided programming (CAP) for digital circuits.

OVERVIEW OF THE CAP PROCESS

Generically speaking, CAP is the process of using a computer as an aid or tool in the preparation of programs. Any programming tool that uses a computer could, in the general sense, be considered to be a CAP tool. In automatic testing technology, however, a more restricted connotation has evolved for CAP. It relates specifically to the use of a computer (together with a software system) to simulate (that is, model) a circuit network for purposes of determining testing parameters. In its simplified form, such a CAP system is illustrated in the block diagram shown. The concept shown is sufficiently general to be applicable to either digital or analog CAP.

In the process illustrated on the prior page, the test engineer uses the engineering drawing (schematic and/or logic diagram) as the basic definition of the UUT characteristics. An ideal CAP system can derive all of the necessary input data from such engineering drawings; however, they first must be coded in terms suitable for ingestion into a computer. Hence, the diagram is converted by human interpretation to a set of alpha and numeric characters in accordance with the programming rules given in a CAP user's guide. This information is generally keypunched into what is called a source deck and used to define the UUT to the CAP system computer. Resident in the computer memory is an algorithm (program of a permanent nature) which contains the logic for setting up a mathematical model of the UUT based on the input source deck and a resident circuit model library defining common circuits that can be called out by the test designer. When the UUT has been set up in the computer memory, the CAP algorithm determines the appropriate stimulus signals required to fully exercise the UUT and the appropriate responses to be expected from a properly performing UUT. It then inserts all of the programmed fault modes for each component in the modeled network, referring to the model library for failure modes. From this, the CAP system derives a fault dictionary of failed components for each combination of input and output signals. The input (stimulus) and output (response) data and the fault data are outputted by the computer to complete the modeling process. These data are generic to the UUT and not peculiar to the particular CAP or ATE system. Hence, further conversion is required to put the results of the CAP run into the appropriate ATE language, which becomes the test program.

Ideally, the CAP process is automatic and routine. Actually, a substantial amount of interaction takes place between the CAP system and the test designer before he achieves a good model that provides an end-to-end test of the UUT and desired resolution (acceptable ambiguity) of faults. For digital models a confidence of 90% or better can generally be realized with respect to being able to discriminate between operational and failed units and properly identify the failure. This should also be the design goal of an analog CAP (or hybrid CAP) system.

ANALOG CAP DEVELOPMENT IS A BIG JOB

Preliminary research and development efforts investigating analog CAP techniques and the feasibility of such a system indicate that it is indeed a large undertaking. Experts disagree on the best approach but all agree that the task is extensive. The Navy has projected a development time of between three and five years. In order to minimize both lead time and risk, several areas of preliminary development will be carried out concurrently by several independent commercial activities on one-year contracts. The more successful and promising techniques will be further developed in follow-on development contracts. When sufficient early development has been completed, a detailed specification for a practical CAP system will be developed. This will form the basis for a competi-

tive procurement. The project team that develops the CAP system will include full-time Navy engineers who will not only monitor the project but also will contribute actively to its design. This approach offers the following advantages:

- a. It will produce a finished design reflecting the exact needs of the Navy even though the full requirement might not be definable at the outset.

- b. Intimate knowledge of the design will be vested in Navy personnel making organic support (Navy maintenance) easier to achieve.

PROGRESS TO DATE

So far, the only accomplishment has been to award four of five contracts based on an open competition held early in 1978. In addition to Navy resources, the Air Force has also made some funds available to support the development. It is recognized that the ultimate CAP system will be of value to many DOD activities and even commercial activities. Consistent with Navy policy, it is intended that the final product be nonproprietary and generally available to qualified DOD contractors.

BRIEF DESCRIPTION OF 1979 TASKS

An analysis of preliminary study results, together with an intensive evaluation of proposals, has led the Navy to select five areas for parallel development. These are:

- a. Algorithm definition and development.
- b. Interactive program generation.
- c. Test implementation (processing techniques).
- d. Frequency domain analysis technique development.
- e. Deductive circuit model development.

The work statement for item c was in the final stages of definition at the time of this writing and, hence, contract award for this element will be delayed somewhat but is still targeted as a FY79 task.

ALGORITHM DEVELOPMENT

This task will pursue development of an algorithm for simulating small, nonlinear analog circuits. The circuits will be modeled in software by comparing predicted performance to actual readings taken from the hardware versions of the circuits. A developed, parameter value estimating algorithm will be applied to the model, and its ability to detect faults will be evaluated. Among the approaches planned are:

- a. Inserting faults in the hardware circuits and recording failure mode data for comparison with the software simulation predictions.

b. Developing a small "building block" library, principally for low-frequency circuitry.

c. Synthesizing a composite circuit model by cascading "building block" models of simpler circuits.

d. Proving the validity of the premise that circuits may be adequately simulated by estimating parameter values for small sections of a circuit between access points.

INTERACTIVE PROGRAM GENERATION

This task involves development of a software system module which will allow the user to communicate effectively with the analog CAP system in a natural, problem-oriented language. It will be implemented in FORTRAN and designed in modular form for easy interfacing with the other system modules.

TEST IMPLEMENTATION

This task deals with the development of a very fast arithmetic processor for computing the huge quantities of complex equations anticipated in the solution of analog circuit failure predictions. This task is the least well defined at this time. The work statement is still being developed, so it will be the last of five contracts to be awarded.

FREQUENCY DOMAIN ANALYSIS TECHNIQUE DEVELOPMENT

This task is intended to develop practical techniques for applying classical circuit analysis techniques, such as the Volterra-Laplace Method, to real circuit test design problems. Although to date the reduction of basic theory to practical implementation has not been adequately demonstrated, this task intends to pursue such a demonstration. This task includes three technical subtasks as follows:

a. The basic methodology development subtask will pursue further refinement of the fundamental concepts of the Volterra-Laplace Method so that it is applicable to realistic nonlinear circuit problems.

b. The application development subtask will apply the basic methodology of subtask "a" to multiple mesh or node, nonlinear analog networks.

c. The fault identification methodology subtask will follow up the nonlinear network analysis with a demonstration that extends the basic methodology to provide fault identification. The process will evaluate the coefficients that describe the component's nonlinearity through the use of a modified P algorithm.

DEDUCTIVE CIRCUIT MODEL DEVELOPMENT

The approach in this task is to build a system that "understands" circuit concepts. By partitioning the UUT circuitry into a set of subcircuits, a more rapid evaluation can be made of each subcircuit and the problem reduced to the faulty subcir-

cuit. This approach minimizes testing and maximizes deductive analysis. The stress will be on a global analysis as opposed to discrete element evaluation. The deductive circuit models used will contain input-output relationships and loading data in addition to the internal circuit models. A major concern will be the method of representing the "intelligence" gained through model analysis. One approach to be tried involves a system of procedural models such as used by Chien and Snyder at the Coordinated Science Laboratory. This technique proved useful for describing hybrid circuits in a system that performs "visual" inspection of automotive ignition systems. It is anticipated that this task will be able to capitalize on this earlier study. The objective of the task is to find a more original approach to fault diagnosis other than the traditional fault dictionary approach which, to date, has been most commonly used.

CONCLUSION

It is uncertain which of the five initial tasks will prove useful for the "ultimate" analog CAP system. Perhaps, alternate approaches will be required and the total project will exceed the ideal schedule of three years for a working system. But, it is the Navy's intent to continue piecemeal tasks until evidence shows that a workable system can be formulated. At that point, alternate methods will be forsaken for the most promising approach and a large-scale effort to develop the end product will be initiated. The Navy has no illusions as to guaranteed success of the early tries, but enough is at stake to continue a concerted effort until a practical CAP system is developed. Earlier experience in developing a practical digital CAP system has taught those involved that there is no simple solution to a complex problem. Nor is the Navy ready to accept the forewarnings of doom that some would predict; that analog circuits will disappear from military applications before the modeling problem is adequately solved. The Navy is not pursuing a "perfect" solution. Rather, one that works at least 10 to 25% better and at half the cost of hit-or-miss manual test design techniques will do very well.

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