Optimal Interleaved Pulsewidth Modulation Considering Sampling Effects

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Abstract—Previous works on interleaved operation of switching power converters are based on the assumption that natural-sampling pulsewidth modulation (PWM) is used. Various interleaving strategies have been reported to minimize EMI filtering requirements, eliminate system resonance at certain frequencies, or minimize total harmonic current distortion through optimization of the interleaving phase shift angles. In a digitally controlled converter, the PWM reference is updated only at discrete sampling points, which is equivalent to using regularly sampled PWM. Harmonic cancellation effects among interleaved converters are affected by such regular sampling such that interleaving strategies optimized based on natural-sampling become non-optimal or suboptimal. This work first presents mathematically models that can be used to quantify the sampling effects on interleaved voltage-source converter harmonic behavior. The effects of different sampling methods are analyzed and compared using the models. Possible modifications to the interleaved carrier phase shift angles to compensate for the sampling effects are developed and demonstrated for different system optimization objectives including minimization of total harmonic distortion in dc-link or phase output currents.

I. INTRODUCTION

The benefits of interleaving have been widely recognized for various applications. Voltage regulator modules [1] and critical mode boost power factor correction (PFC) converter [2] use interleaving to minimize harmonic current ripple thereby reducing ripple filtering requirements. Three-phase voltage source converters (VSC) can be designed to use smaller EMI filters or dc-link bus capacitors through proper interleaved operation of parallel modules [3,9]. The effects of interleaving can be described using spectral models of pulsewidth modulators [9-11], which have served as the basis for the development of optimal interleaving strategies targeting at reducing EMI filtering requirements, eliminating system harmonic resonance, or minimization total harmonic current distortion of either input or output currents [9,12-14]. Existing works on this topic have assumed natural-sampling PWM in which a continuous reference signal is compared with the carrier signal using an analog circuit, and the carrier signals in different modules are phase shifted from each other according to specific interleaving strategies to achieve certain system objectives as mentioned before [9].

Digital control is increasingly used in power electronics [4,18]. In particularly, high-power converters for motor drive, renewable

energy, and power system applications are almost always controlled digitally [4-7]. Unlike in analog control systems where the PWM reference is a continuous signal of time, a digital controller only updates the PWM reference at the sampling points of the system. This is equivalent to using regular-sampling PWM [15] where the reference is sampled at regular points. One implication of such digital control is that the spectral models that were used in the development of various interleaving strategies assuming continuous reference and natural sampling are no longer valid. As the result, interleaving methods that are optimized to achieve certain system objectives [9] become non-optimal or suboptimal. To maximize the benefit of interleaving in such digital control system, it is important to understand the effects of sampling on system harmonic cancellation, and to develop control techniques that avoid or compensate for the sampling effects.

Two different interleaving techniques have been reported in the literature. Among them, symmetric interleaving [10] uses the carrier signals that are equally spaced over a carrier period. A more general PWM method, asymmetric interleaving, removes this restriction on the carrier phase shift and allows it to assume any value between 0 and 360° [9-14]. This adds many more degrees of freedom in system control and allows different system optimization objective to be achieved. Asymmetric interleaving, on the other hand, is more sensitive to sampling effects. To date, the impacts of sampling on harmonic cancellation under either symmetric or asymmetric interleaving have not been investigated. Additionally, previous works have suggested that the regular sampling process introduces a reduction in the harmonic cancellation effects of the output voltage and current waveforms, thereby negatively impacting the benefits of interleaving. While this is true for the most general case, it will be shown that the effects can be minimized with proper coordination of the digital sampling instants and the individual carrier waveform interleaving angles.

This paper presents several digital sampling methods as solutions to minimizing the effects of sampling on the harmonic cancellation benefits of interleaving. Of these solutions, asymmetric interleaving in combination with the common single carrier sampling method provides improved system level performance with nearly zero impact on the digital control system. Analytical models based on an N parallel converter system operated under a distributed digital control architecture, assuming an arbitrary interleaving angle, ϕ_{ck} , and arbitrary PWM reference update rate, T_r , are developed to determine the optimum PWM reference update rate and applicable sampling method. The

proposed solutions avoid the increased input and output THD, dc-link ripple current, and output ripple current inherent to low switching frequency applications when the digital sampling effects are neglected.

The rest of the paper is organized as follows: Section II investigated the effects of sampling by developing the analytical models of the assumed system using double Fourier analysis. Section III proposes several sampling methods and PWM reference update rates, in addition to asymmetric interleaving, as solutions to minimize digital sampling effects in high power converters. Section IV discusses optimal PWM under both symmetric and asymmetric interleaving considering PWM sampling effects. Section V concludes the paper.

II. EFFECTS OF SAMPLING

Fig. 1 depicts three parallel three phase voltage source converters controlled by a distributed digital control system architecture. In this architecture, a digital device performs all system-level control functions and produces a common reference for all converter modules operating in parallel. Each module has its own modulator that accepts the system-level reference and produces gate control signals using either a digital (timer) or an analog circuit. It is assumed that all modules operate at the same switching frequency and use the same modulation method. The carrier signals, whether explicitly used (such as in the case of an analog modulator) or implicitly embedded in a digital modulator design, are phase-shifted from each other according certain inter-

leaving strategies [9-14].

As a comparison, consider if the system level controller were implement with only with analog circuitry (resulting in no digital sampling). In this type of system, the control inputs (voltage, current, etc.) would simply be connected to the inputs of the control loop circuitry (with proper scaling and isolation), with the output of this circuitry directly providing the analog (naturally sampled) PWM references to the local modulators. The local modulators (either implemented digitally or analog) would then use this continuous reference to generate the PWM gate control signals. The primary difference between the digital and analog system level controller implementations is the fact that the digital control system provides a discrete (sampled) PWM reference while the analog control system provides a continuous PWM reference. This variable is represented by v_{ref} in Fig. 1 and will be the primary focus of this paper.

The distributed digital control system depicted in Fig. 1 will serve as the basis for the harmonic analysis presented, with primary focus placed on the update rate of v_{ref} . It should be noted that although a distributed control architecture is assumed, the analysis and conclusions are equally applicable to single FPGA/DSP control systems, so long as the PWM reference is discrete (sampled).

Due to the benefits of asymmetric regular sampling (updating twice per carrier interval) over symmetric regular sampling (updating once per carrier interval), the remainder of the paper assumes double-edge sine-triangle PWM under asymmetric regular sampling [15]. This implies that each modulator in Fig. 1

Fig. 1. Three parallel voltage sourced converters operated under distribution digital control architecture.

requires an updated reference twice per carrier interval, independent of the update rate of v_{ref} .

To quantitatively describe the effects of sampling on interleaved PWM converter performance, we apply the modified double-Fourier integral presented in [9] to develop a spectral model for each PWM output. In general, the double-Fourier coefficient can be written as

$$C_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) e^{j(mx + ny)} dx dy \quad (1)$$

where $g(y) = \pi/2 + v_r(y)$, $v_r(y)$ represents the PWM reference, and φ_c is the initial phase angle of the carrier. To account for the sampling effect, the continuous variable y in (1) needs to be separated into two discrete stair-case variable corresponding to the updating instants of the discrete PWM reference. The resulting combined double-Fourier coefficient C_{mn} of N interleaved converter modules at harmonic frequency $mf_s + nf_1$ is

$$C_{mn} = \kappa_m \frac{V_{dc}}{q\pi} J_n\left(q\frac{\pi}{2}M\right) \sin\left[(m+n)\frac{\pi}{2}\right] \quad (2)$$

where V_{dc} is the dc-link voltage, M is the modulation index of the converter, J_n is a Bessel function of the first kind, m represents the carrier frequency counter, n represents the fundamental frequency counter, and

$$q = \frac{(m+n)f_1}{f_s}.$$

The scaling factor κ_m is defined as

$$\kappa_m = \frac{1}{N} \sum_{k=1}^N e^{jm\varphi_{ck}} e^{-jn(f_1/f_s)(\phi_{rk} - \varphi_{ck})} \quad (3)$$

where φ_{ck} is the carrier phase angle of the k^{th} module, ϕ_{rk} is the angular position of the PWM sample within the k^{th} modules carrier period and is related to the device switching period T_s , and digital sampling rate T_r , by $\phi_{rk} = (2\pi/T_s)T_r$. Note that the modification to the scaling factor over the naturally sampled case, as a result of including T_r , is captured in a single term given by $\exp(-jn(f_1/f_s)(\phi_{rk} - \varphi_{ck}))$. Next we will determine the effects the sampling process has on the harmonic spectrum in general.

Fig. 2 plots the output phase voltage spectrum for a parallel converter system operated under symmetric interleaving with the following operating parameters: $N = 3$, $V_{dc} = 2\text{kV}$, $M = 0.9$, $f_o = 60\text{ Hz}$, and $f_s = 540\text{ Hz}$. The primary differences between the two spectrums can be summarized as follows: First, the sampling process introduces asymmetry into each carrier and sideband harmonic group. This effect is well documented in the literature [15] and is independent of interleaved operation. Second, the fully cancelled carrier and sideband harmonics under natural sampling ($m \neq N$), are only partially reduced under digital sampling.

Fig. 2. Comparison of output phase voltage spectrum for parallel converter system operated under symmetric interleaving and a) natural and b) digital sampling at a rate of $T_r = 2/f_s$.

Lastly, the carrier and sideband harmonics that are not cancelled in the naturally sampled case, ($m = N$) have differing magnitudes and phases. The severity of each of these individual effects largely depends on the sampling method used and corresponding rate at which the PWM reference is updated. As such, the next section will discuss possible solutions for minimizing these effects through proper sampling and/or modifications of system interleaving angles.

Although the analysis above was focused on parallel VSCs, the developed spectral models can be extended to multilevel converters based on the relationship between parallel converter and multilevel converter switching functions established in [10]. For example, the following scaling factors can be obtained for different multilevel converter topologies where ϕ_{s1} and ϕ_{s2} correspond to the two sine-wave reference phase angles when unipolar PWM is assumed.

1) Cascaded H-bridge Topology:

$$\kappa_m = N(e^{jn\phi_{s1}} - e^{jn\phi_{s2}}) \sum_{k=1}^N e^{jq\varphi_{ck}} e^{-jn(f_1/f_s)(\phi_{rk} - \varphi_{ck})} \quad (4)$$

2) Cascaded Phase Leg Topology:

$$\kappa_m = N \sum_{k=1}^N e^{jq\varphi_{ck}} e^{-jn(f_1/f_s)(\phi_{rk} - \varphi_{ck})} \quad (5)$$

3) Capacitor Clamped Topology:

$$\kappa_m = \sum_{k=1}^N e^{jq\varphi_{ck}} e^{-jn(f_1/f_s)(\phi_{rk} - \varphi_{ck})} \quad (6)$$

III. POSSIBLE SOLUTIONS

The effects of limited sampling frequency on system control

performance has been discussed extensively in the control literature, see e.g. [16-18]. Instead of zero-order hold, for example, a first-order hold can be used to provide more continuous reference between system sampling instants. Interpolation and extrapolation techniques can also be used to generate additional reference points between system sampling instants. These methods, however, introduce additional dynamics into the system control loop that need to be considered in system control design. In the following, we will focus on system sampling and PWM algorithms that don't affect system dynamics.

A. Sampling at $2Nf_s$

This sampling method, depicted in Fig. 3c, is a general sampling method in which the PWM reference is updated according to the number of parallel modules N . Referring to Fig. 1, this method can be implemented by simply setting $T_r = 2N/f_s$ in the system level controller, with no additional modifications required to the pulsewidth modulators.

The drawback of this method is that it requires high speed control loops capable of updating the PWM reference $2N$ times the switching frequency, which may not always be possible. The advantage of this method is that it can result in increased harmonic reduction when standard symmetric interleaving is used. However, this advantage is limited to only those specific case in which the PWM reference update instants and carrier waveform peak and valleys coincide. In these special cases, the harmonic cancellation achieved under natural sampling can be achieved under digital sampling.

Figure 4 plots the difference in the magnitude of the scaling factor ($|\Delta\kappa_m|$) between the scaling factor under natural sampling (given by (3) when $\phi_{ck} = \phi_{rk}$) and the scaling factor under various

Fig. 3. Asymmetric Interleaving PWM reference updates under a) $T_r = 2/f_s$, b) multirate sampling synchronized to carrier signals, and c) $T_r = 6/f_s$.

digital sampling methods, defined in (3) for an irregular asymmetric interleaved system, representing the most generalized interleaving case. The $2Nf_s$ sampling method discussed here is represented in Fig. 4b. The major conclusions that can be drawn from Fig. 4b is that for low values of n ($n < 5$) the difference in the scaling factor over the naturally sampled case only varies by as much as 10%. This implies that the harmonic cancellation effects of naturally sampled interleaved systems are largely preserved under this sampling method, making it a good choice when the digital control systems allows for the increase in sampling frequency.

B. Multirate Sampling Synchronized to Carrier Signals

This sampling method, depicted in Fig. 3b, is a customized sampling method in which the PWM reference is updated according to the specific interleaving angles of the system. Referring to Fig. 1, this method can be implemented by adding N sampling intervals in the system level controller, each corresponding to a pulsewidth modulators specific interleaving angle. The pulsewidth modulators would then select the corresponding PWM reference update that coincides with its specific carrier interleaving angle.

The advantage of this method is that it can result in harmonic cancellation that is equivalent to natural sampling, independent of the specific interleaving angles within the system. This is highlighted in Fig. 4e where the variation between the naturally sampled scaling factor and the scaling factor associated with this sampling method is always equal to zero, independent of the specific value of n . This is in contrast to sampling at $2Nf_s$ which can only achieve the harmonic cancellation of natural sampling for specific cases of symmetric interleaving where the sampling instants and carrier waveform peak and valleys coincide. The major drawback of this method is that it requires complex high speed control algorithms resulting from the varying sampling intervals. This fact makes this sampling method undesirable practically.

C. High Frequency Sampling

Fig. 4. Variation in scaling factor between natural sampling and sampling at a) $2f_s$, b) $2Nf_s$, c) high frequency sampling at $8f_s$, d) high frequency sampling at $30f_s$, and e) multi-rate sampling synchronized f_s for $N = 3$, $m = 3$, and irregular asymmetric interleaving angles of 0° , 77° , and 193° .

This sampling method attempts to approximate natural sampling PWM by updating the reference at a much higher rate than f_s and has been applied to FPGA based, space vector modulated converters [20]. This sampling method updates the PWM reference at a fixed rate of $2kf_s$, where $k > N$. Referring to Fig. 1, this method can be implemented by setting $T_r = 2k/f_s$ in the system level controller, with no modifications to the pulse-width modulators. In general we can consider two different cases of high frequency sampling. Case I considers k that is only several times larger than N while the case II considers k orders of magnitude larger than N .

Case I is depicted in Fig. 4c where sampling frequency is set to $8f_s$. It is easy to see that this case results in higher scaling factor magnitude variations when compared to Fig. 4c, representing the $T_r=2/f_s$ case. This is mainly due to the angular position of the sampling instants within each carrier period to each carriers peak and valley. Therefore, in general, slightly increasing the sampling frequency above $2Nf_s$ does not guarantee achieving increased harmonic reduction over lower sampling frequencies.

Case II is depicted in Fig. 4d where the sampling frequency is set to $30f_s$. It is immediately apparent that this method results in the closest approximation to natural sampling when compared to all the other sampling methods. However, the primary drawback of this method is that it requires the fastest high speed control loop which can be orders to magnitude higher than the system switching frequency. Due to this limitation, this method is also not considered a good choice practically as it puts large constraints on the digital control system.

D. Compensating through Change in Interleaving Angles

In most practical systems, increasing the sampling frequency beyond twice the switching frequency is impractical and irregular sampling synchronized to the asymmetrically interleaved carrier signals is highly undesirable. When only regular sampling at $2f_s$ is permitted, the interleaving method can be revisited and possibly modified to compensate for the sampling effect. The mathematical models presented in the previous section provided a basis for developing such compensation methods. One must only consider the objective function for optimization (such as output current ripple or dc-link current expressions), and the analytical models of the previous section with the optimization variables being the N interleaving angles of the system. The next section will present specific compensation methods for different system optimization objectives using the above described method.

IV. OPTIMAL INTERLEAVING TO COMPENSATE FOR SAMPLING

As discussed in the previous section, multirate sampling and sampling above twice the switching frequency are in general not practical. A more practical method to compensate for the sampling effects is to modify the system interleaving strategy. The necessary modification depends on the specific optimization objective and is discussed in the following for three different system-level objectives.

A. Line-Line Voltage THD Minimization

For this optimization example, consider a parallel converter systems operated under the distributed control architecture depicted in Fig. 1 with the operating parameters as identified in Table I below where I_{pk} is peak output phase current and L_i represents system interleaving inductors.

TABLE I EXAMPLE SYSTEM OPERATING PARAMETERS

N	V_{dc}	M	f_1	f_s	RL load	I_{pk}	L_i
2	2 kV	0.9	60 Hz	540 Hz	2.5 Ω 2 mH	315 A	5 mH

The line-line voltage THD for this converter systems is plotted in Fig. 5 for both natural sampling and digital sampling where $T_r=2/f_s$. Note that for this example, symmetric interleaving does not result in the optimum interleaving angle in either the naturally sampled or digital sampled cases. For natural sampling, depicted in Fig. 5a, the optimum interleaving angle is 80° . For the digital sampling case, depicted in Fig. 5b, the optimum interleaving angle is 110° . Therefore, when operating under the common digital sampling method of $T_r=2/f_s$, the system interleaving angle should be changed from 80° to 110° degrees for output voltage THD minimization.

Fig. 5. Line-line voltage THD for two parallel modules operating under a) natural sampling and b) digital sampling of $T_r=2/f_s$.

B. DC-Link Ripple Current Minimization

In parallel converter systems, interleaving can also reduce the dc-link ripple current due to the harmonic cancellation benefits at the input [10,12]. The dc-link current for a single VSC is given by (7) and (8) below where C_{00} represents the dc component [19]:

$$C_{00} = \frac{3M}{4} I_{pk} \cos(\theta_{pf}) \quad (7)$$

$$C_{mn} = \frac{I_{pk}}{m\pi} \cos\left[\frac{\pi}{2}(m+n)\right] \left[1 + \cos\left(2n\frac{\pi}{2}\right)\right] \cdot \left\{ J_{n+1}\left(m\frac{\pi}{2}M\right) e^{j\theta_{pf}} - J_{n-1}\left(m\frac{\pi}{2}M\right) e^{-j\theta_{pf}} \right\} \quad (8)$$

Following the same procedure outlined in Section II above and modifying the expressions for the addition of the scaling factor κ_m , we can modify the above expressions to account an arbitrary digital sampling method. It should be noted that the dc component

of the dc-link current is unaffected by the specific sampling method and is the same as (7). The final expressions for the carrier and sideband harmonics is given by (9).

$$C_{mn} = \kappa_m \frac{I_{pk}}{q\pi} \cos\left[\frac{\pi}{2}(m+n)\right] \left[1 + \cos\left(2n\frac{\pi}{2}\right)\right] \cdot \left\{ J_{n+1}\left(q\frac{\pi}{2}M\right)e^{j\theta_{pf}} - J_{n-1}\left(q\frac{\pi}{2}M\right)e^{-j\theta_{pf}} \right\} \quad (9)$$

Using equations (7) and (9), we can examine the impact of the specific digital sampling method on the RMS dc-link ripple current, defined by (10).

$$I_{dc} = \sqrt{\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} C_{m,n}^2} \quad (10)$$

Fig. 6 plots the variation in the RMS dc-link current for a parallel converter system with the same operating parameters identified above except for we now assume three parallel modules ($N = 3$). Two cases with varying modulation index and varying power factor angles are depicted. Consider the case where the power factor angle is 70 degrees. In this case, Fig. 6d identifies an optimum regular asymmetric interleaving angle of 312° for natural sampling PWM. The resulting RMS dc-link ripple current is 46.6 amps and is shown in Fig. 7a along with the spectrum of the dc-link current.

If we were to assume this optimum natural sampling interleaving angle for the digital sampling case of $T_r=2/f_s$, the resulting RMS dc-link current would be sub-optimal. This is shown in Fig. 6e, along with the corresponding spectrum shown in Fig. 7b, and results in an RMS dc-link ripple current of 63.8 amps. Referring back to Fig. 6e, the optimum regular asymmetric interleaving angle for the digital sampling case of $T_r=2/f_s$ is shown to be 175° . This interleaving angle corresponds to a total RMS dc-link ripple current of 55.8 amps and is depicted in Fig. 7c. In general, asymmetric interleaving can be used to reduce RMS dc-link

Fig. 6. RMS dc-link ripple current for $N = 3$, $M = 0.9$, operated under a power factor angle of 16.7° (dotted) under a) natural sampling, b) $T_r=2/f_s$, and c) $T_r=6/f_s$ and 70° (solid) under d) natural sampling, e) $T_r=2/f_s$, and f) $T_r=6/f_s$. Plot discontinuities correspond to instances when interleaving angle equals PWM reference update instant.

Fig. 7. Spectrum of dc-link current under a) optimized natural sampling, b) unoptimized digital sampling of $T_r=2/f_s$ and c) optimized digital sampling of $T_r=2/f_s$. The RMS dc-link ripple current is also given.

ripple current when digital sampling is used. The exact optimum interleaving angle will vary over several system parameters including M , N , and power factor.

C. Output Current Ripple Minimization

Asymmetric interleaving has also been shown to reduce the output current ripple on parallel converter systems [9,14]. The most common metric to evaluate output current ripple is the weighted THD (WTHD) metric and this will be assumed here [15].

Fig. 8 plots the variation in WTHD for a parallel converter system with the same operating parameters as for the RMS dc-link current minimization example. Similar to dc-link ripple current minimization, the specific sampling method used effects the achievable harmonic cancellation. Figures 8a and 8c plot the variation in WTHD over all possible regular asymmetric inter-

Fig. 8. WTHD comparison for $N = 3$, $M = 0.9$ under a) natural sampling and b) $T_r=2/f_s$ and $M = 0.3$ under c) natural sampling and b) $T_r=2/f_s$.

leaving angles for natural sampling while Figs. 8b and 8d plot the variation for the digital sampling case of $T_r=2/f_s$. It is obvious to see that the optimum interleaving angle for natural sampling (240°) is sub-optimal when digital sampling is used. For the case of $T_r=2/f_s$, the optimum interleaving angle is 130° . Therefore, the interleaving angles for the pulsewidth modulators should be changed from the standard symmetric interleaving angle of 240° to the optimum regular asymmetric interleaving angle of 130° .

V. CONCLUSIONS

Digital control systems and the associated PWM sampling method can have significant impacts on the performance of interleaved converter systems. The developed analytical models provide a convenient and straight forward method to analyze such systems, and provides additional insight into the harmonic cancellation process of sampled systems. It was shown that when the PWM reference updates coincide with the specific interleaving angles of the system the harmonic cancellation benefits of naturally sampled systems is achievable under regular sampled systems. In situations where the PWM sampling frequency cannot be increased, modifying the system interleaving angles according to a given system optimization objective was shown to compensate for some digital sampling effects and provide additional reductions in output voltage THD, output current ripple, and RMS dc-link current ripple. The general modeling approach was applied to both parallel and multilevel converter systems, and the effect of the digital sampling process was shown to be topology independent. The practical benefits the proposed sampling methods include increased harmonic cancellation and minimization of input and output THD. Lastly, the scaling factors for several multilevel topologies were derived and presented as a means to analyze asymmetric interleaving and PWM sampling effects in MLCs.

REFERENCES

- [1] Y. Zhihong, D. Boroyevich, and F. C. Lee, "Paralleling non-isolated multi-phase PWM converters," in *Proceedings of IEEE Industry Applications Society Annual Meeting*, vol. 4, pp. 2433-2439, Oct. 2000.
- [2] J. R. Tsai, T. Wu, C. Wu, Y. Chen, M. Lee, "Interleaving phase shifters for critical-mode boost PFC," *IEEE Transaction on Power Electronics*, vol. 23, no.3, pp. 1348-1357, May 2008.
- [3] L. Asiminoaei, E. Aeloiza, P. Enjeti, F. Blaabjerg, "Shunt active-power - filter topology based on parallel interleaved inverters," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1175-1189, March 2008.
- [4] W. Yongqing, Z. Xiaofeng, Q. Mingzhong, K. Jun, "Control of parallel inverters based on CAN bus in large-capacity motor drives," in *Proceedings of Electric Utility Deregulation and Restructuring and Power Technologies Conference*, pp. 1375-1379, 2008.
- [5] S. Schoder, et al, "Modular high-power shunt-interleaved drive system: A realization up to 35 MW for oil and gas applications," *IEEE Transactions on Industry Applications*, vol 46, no. 2, pp. 821-830, March/April 2010.
- [6] M. N. Marwali, A. Keyhani, "Control of distributed generation systems - Part I: Voltages and currents control," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1541-1550, Nov. 2004.
- [7] E.J. Bueno, A. Hernandez, F.J. Rodriguez, C. Giron, R. Mateos, S. Cobrecas, "A DSP- and FPGA-based industrial control with high-speed communication interfaces for grid converters applied to distributed generation systems," *IEEE Transactions on Industrial Electronics*, vol.56, no. 3, pp. 654-669, October 2008.
- [8] J. Wen, K.M. Smedley, "Synthesis of multilevel converters based on single and/or three-phase converter building blocks," *IEEE Transactions on Power Electronics*, vol. 23, no.3, pp. 1247-1256, May 2008.
- [9] T. Beechner, and J. Sun, "Asymmetric interleaving - A new approach to operating parallel converters," in *Proceedings of IEEE Energy Conversion Congress and Exposition*, pp. 99-105, September 2009.
- [10] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase VSCs," in *Proceedings of IEEE Power Electronics Specialists Conference*, pp. 29-35, 2007.
- [11] J. Sun, *Modeling and Analysis of Pulse-Width Modulation*, Professional Education Seminar, *IEEE 2008 Applied Power Electronics Conference*, Austin, TX, February 2008.
- [12] D. Zhang, F. Wang, R. Burgos, R. Lai, D. Boroyevich, "Interleaving impact on harmonic current in DC and AC passive components of paralleled three-phase voltage-source converters," in *Proceedings of Applied Power Electronics Conference and Exposition*, pp. 219-225, 2008.
- [13] L. Xing, J. Sun, "Motor drive system EMI reduction by asymmetric interleaving," in *Proceedings of Workshop on Control and Modeling for Power Electronics*, pp. 1-7, 2009.
- [14] D. Zhang et al, "Impact of interleaving impact on AC passive components of paralleled three-phase voltage-source converters," *IEEE Transactions on Industry Applications*, vol. 46, no. 3, pp. 1042-1054, May/June 2010.
- [15] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters - Principles and Practice*, Wiley & IEEE Press, 2003.
- [16] H.A. Kojori, J.D. Lavers, S.B. Dewan, "A critical assessment of the continuous-system approximate methods for the stability analysis of a sampled data system," *IEEE Transactions on Power Electronics*, vol. 8, no. 1, pp. 76-84, January 1993.
- [17] E.A. Mayer, R.J. King, "An improved sampled-data current-mode-control model which explains the effects of control delay," *IEEE Transactions on Power Electronics*, vol. 16, no. 3, pp. 369-374, May 2001.
- [18] D.G. Holmes, T.A. Lipo, B.P. McGrath, W.Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2417-2426, January 2008.
- [19] B.P. McGrath, D.G. Holmes, "A General Analytical Method for Calculating Inverter DC-Link Current Harmonics," in *IEEE Transactions on Industry Applications*, pp. 1851-1859, September/October 2009.
- [20] A. L. Julian, G. Oriti, "FPGA based digital implementation of naturally sampled space vector modulation," in *Proceedings of IEEE Energy Conversion Congress and Exposition*, pp. 625-630, September 2009.