Demonstration of a 600-V, 60-A, Bidirectional Silicon Carbide Solid-state Circuit Breaker

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***Abstract*—Bidirectional solid-state circuit breakers (BDSSCBs) can replace mechanical fault protection devices in systems having bidirectional current flow through a single bus, for increased transition speed, functionality, and reliability. Silicon carbide, 1200-V, 0.1-cm^2 JFETs were designed and fabricated for the BDSSCB application. A novel BDSSCB gate driver was developed for both self-triggered temperature-compensated over-current protection, and external triggering. Bidirectional 600-V, 60-A fault isolation was demonstrated in a transition time of approximately 10 µs with two packaged JFET modules, a bidirectional RCD snubber, and a series distribution bus inductance of 20 µH.**

I. INTRODUCTION

In addition to AC systems, many DC power electronic systems have bidirectional current flow through a single power distribution bus. Commonly, these systems supply energy to and from electrical storage elements. Other AC and DC systems operate between active power sources and/or potential power sources. In these cases, a fault can result in an over-current condition in either direction in the system. Some examples of these systems include hybrid electric vehicle drives, grid-tie photovoltaic inverter systems, and bidirectional DC-DC converters. Such systems cover a wide range of power levels, generally require fault protection, and benefit further from bidirectional fault protection.

In many applications, bidirectional fault isolation is provided by mechanical contactors or relays. However, mechanical fault protection devices often do not have adequate actuation speeds for protection of solid-state system components. Furthermore, these mechanical devices can suffer severe degradation, dramatically reducing operating life, or resulting in catastrophic system failure. In contrast, bidirectional solid-state circuit breakers (BDSSCBs), even coupled with transient voltage suppression components, can be actuated orders of magnitude faster. Although practical BDSSCBs have higher conduction voltage drops than their mechanical counterparts, current scalable designs can dramatically reduce ON-state losses, and semiconductor packaging techniques can enable adequate cooling. Ultimately, BDSSCBs can provide dramatic improvements in reliability and operating life, resulting in superior system protection and reduced system maintenance and repair.

II. BDSSCB DEVICES

In many power switching applications, normally-OFF devices are preferred over normally-ON devices for their ability to block voltage in the absence of control power. However, in many applications, a normally-ON fault protection device may be preferred. This can be based on the percentage of system operating time that the protection device spends in the ON-state, and on the system reliability impact of damage to the fault protection sub-system, or its malfunction. With the normal BDSSCB state being the ON-state, system reliability is increased by not needing to provide an active bias to maintain rated conduction. A voltage-controlled, majority-carrier device, having a positive temperature coefficient of ON-state resistance, is preferred. These features simplify device control, and promote balanced currents among parallel devices, facilitating current-scalable BDSSCBs. Junction field effect transistors (JFETs) meet these criteria and can provide additional advantages over metal oxide semiconductor field effect transistors (MOSFETs). Without gate oxides, JFETs can operate at higher temperatures than MOSFETs, and can be more tolerant of high transient voltages [1],[2]. Also, the low JFET gate-charge results in fast transition speed and can aid in device current sharing during switching transitions.

Silicon carbide (SiC) 1200-V, 10-A, normally-ON, vertical JFETs were developed for a BDSSCB evaluation. Unlike other normally-ON SiC JFET devices, that are designed for maximum conduction with a positive gate bias, the BDSSCB JFETs were designed to have a more normally-ON characteristic for rated conduction at zero gate bias [3]. Figs. 1 and 2 show the JFET I_D versus V_{DS} conduction and blocking curves, respectively. The 0.1-cm^2 (0.07-cm^2 active area) JFETs have a specific ON-state resistance of 9.8 mΩ-cm^2, at a 10-A drain current (211 W/cm^2 at 25 ˚C) for a zero-volt gate-to-source bias. Additionally, the JFETs exhibit extremely low leakage currents and sharp onsets of breakdown at both the drain-to-gate and source-to-gate junctions, resulting in stable and efficient operation [4],[5].

III. BDSSCB CONFIGURATION AND BIPOLAR CURRENT

This BDSSCB design has parallel pairs of common-source connected JFETs, and a bidirectional RCD snubber connected across opposite JFET drain terminals to mitigate

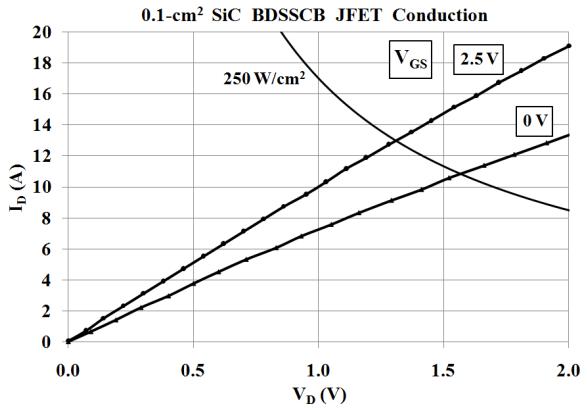

Figure 1. 0.1-cm^2 SiC BDSSCB JFET conduction

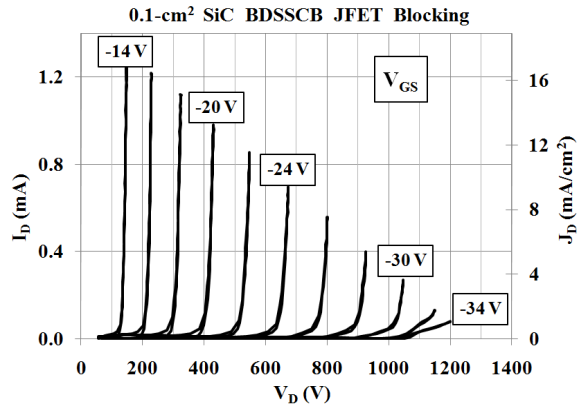

Figure 2. 0.1-cm^2 SiC BDSSCB JFET voltage blocking

voltage overshoot from series inductance. A schematic representation is shown in Fig 3. Individually, under unipolar conduction, the JFETs have nearly symmetric bidirectional conduction curves (I_D vs. V_D and I_S vs. V_S). However, the JFETs do not reverse voltage block (V_{SD}) beyond gate voltage breakdown limits. Bidirectional blocking and bidirectional conduction are achieved using the symmetric common-source structure. Unlike a common-drain structure, the common-source connections allow a single gate driver to be used for BDSSCB control.

When either of the diodes formed between the gate-to-source or gate-to-drain terminals of the JFET conduct due to sufficient forward bias, the JFET transitions from unipolar to bipolar conduction. Bipolar currents are generally undesirable due to the additional stress placed on device terminations and gate drive components. Bipolar current from the gate-to-source can be avoided using low voltage (positive) or zero-volt gate biases. Bipolar current from the gate-to-drain forms in reverse conducting JFETs for source-to-drain voltage drops that cause the gate-to-drain voltage drop to exceed the built-in potential (2.7 V at 25 °C) of the gate-to-drain diode. The effect is illustrated in Fig. 4 for a positive 2-V gate bias. The forward conducting JFET (left) has a conduction drop that reduces its gate-to-drain potential, while the reverse conducting JFET (right) has a conduction drop that increases its gate-to-drain potential. For lower positive gate biases, bipolar gate current forms at higher reverse conduction voltage drops. This results in higher conduction current and/or higher junction temperature operating capability below a point at which bipolar gate current flows.

SiC JFETs in the common-source configuration can operate at rated conduction current at a zero-volt gate bias without bipolar gate current. However, at higher conduction current and/or higher temperature, the positive temperature coefficient of JFET ON-state resistance reduces the conduction current at which bipolar gate current begins to flow. Bipolar gate current can then be sensed and used to enable BDSSCB over-current protection which provides inherent temperature compensation. The high-temperature capability of the SiC JFET provides sufficient margin to meet this operating condition over a range of JFET temperatures and conduction currents.

IV. Bipolar Current Actuated Gate Driver

A method of bidirectional over-current protection triggered by bipolar current was developed. A novel gate driver was designed to sense bipolar gate current in reverse conducting JFETs in the BDSSCB common-source configuration, and to transition the JFETs to the OFF-state. In addition to steady-state over-current protection, the method can provide protection from short duration transient currents. The driver circuit latches the JFETs in the OFF-state after bipolar current is detected, to avoid a possible oscillatory condition. The bipolar current actuated driver (BCAD) also provides two isolated auxiliary inputs for

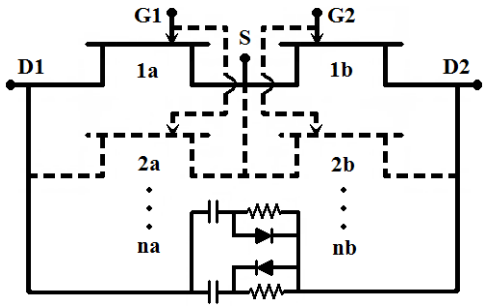

Figure 3. Common-source JFET and bidirectional snubber BDSSCB design

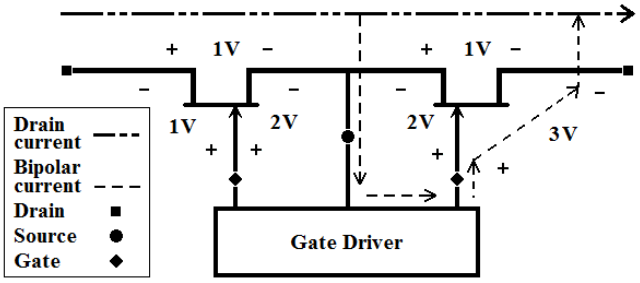

Figure 4. Common-source biasing and bipolar gate current formation

externally triggered independent or synchronized BDSSCB turn-OFF. These lines can be used for manual control or for actuation from the output of other sensors or devices.

Fig. 5 shows a schematic of the BDSSCB BCAD circuit. The BDSSCB is represented by two JFETs connected in the common-source configuration. The driver provides a zero-volt gate bias to the JFETs in the ON-state. The zero-volt bias simplifies the driver design by eliminating the need for an additional gate bias voltage. A resistive element connected across the gate and source terminals of each side of the BDSSCB serves as a passive clamp in this operating mode. The negative gate voltage bias is provided by a DC power supply with the positive terminal connected to the common-sources of the JFETs. A circuit connected to each JFET gate provides actuation from bipolar gate current and from an auxiliary input.

Referring to the symmetric circuit of Fig. 5, when a bipolar current enters the gate of either JFET (Q1, Q2) while reverse conducting, the bipolar current will flow into the gate driver circuit through the common-source connection. A resettable fuse type device (T1, T2) that opens at a set current level conducts the bipolar current, and a resistive voltage drop forms across that resettable device. When the voltage reaches the anode-to-gate trigger voltage or offset voltage of the uni-junction transistor (UJT), (Q3, Q5) connected across the resettable device, the UJT will turn-ON and conduct current from anode-to-cathode sourced by the gate bias DC power supply. A high speed diode (D1, D3) is used with its cathode and anode connected to the gate and cathode, respectively, of the UJT to prevent a gate-to-cathode reverse voltage in excess of the rated value. A capacitor (C1, C2) is connected between the anode and gate of the UJT to prevent undesired triggering of the UJT, and a resistor (R1, R4) is connected in series with the UJT gate to limit gate current. A resistor (R2, R5) and zener diode (D2, D4) connected in series with the UJT provide a fixed gate voltage for the MOSFET (Q4, Q6) that has its drain connected to the gate of the forward conducting JFET (in this example), and its source connected to the negative terminal of the JFET gate bias supply. After the UJT begins to conduct, the MOSFET is gated to the ON-state, connecting the negative terminal of the JFET gate bias supply to the forward conducting JFET gate. The resettable device in parallel with the gate-to-source junction of the forward conducting JFET is forced to conduct current until it reaches its non-conducting state, and the JFET negative gate bias is applied to turn-OFF the forward conducting JFET. Before its transition to a non-conducting state, the current through the resettable device triggered a similar sequence of events on the set of devices controlling the gate potential of the reverse conducting JFET, thereby biasing it to the OFF-state an interval of time after the turn-OFF of the JFET that was previously forward conducting. The time interval between forward and reverse conducting JFET device transitions to the OFF-state is determined by the values of the capacitor and resistor connected to the gate of the UJT and by the turn-OFF delay time of the resettable device. By gating the forward conducting JFET to the OFF-state before gating the reverse conducting JFET to the OFF-state, the reverse conducting JFET is protected from a source-to-drain voltage in excess of its reverse blocking capability.

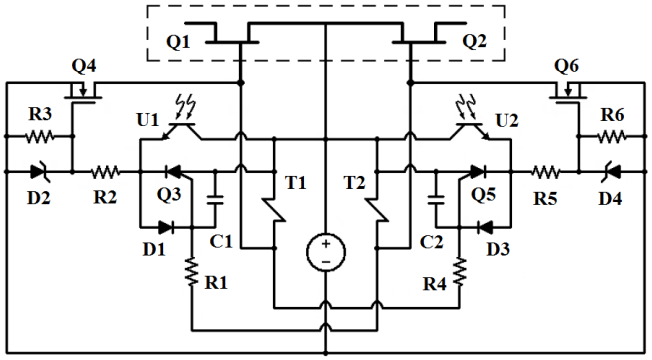

Figure 5. Bipolar current actuated driver schematic

The two optically isolated auxiliary inputs allow gate driver turn-OFF actuation from external sources. The open-collector BJT output of an optocoupler (U1, U2) is connected in parallel with each UJT with the BJT collector and emitter connected to the UJT anode and cathode, respectively. The optocouplers can be turned-ON individually to select the order in which the JFETs are turned-OFF, or the optocouplers can be turned-ON simultaneously to provide synchronized JFET turn-OFF transitions. Actuation can be achieved by either pulsing or holding one or both optocouplers in the ON-state. During either the bipolar current actuated or auxiliary actuated JFET turn-OFF, the gate driver output latches the JFET OFF-state bias. To resume conduction through the BDSSCB, the voltage of the gate bias supply can be reduced to zero or disconnected from the circuit (disconnect not shown). The gate bias supply voltage must be restored or reconnected to the circuit before the next BDSSCB turn-OFF transition.

V. BCAD BDSSCB Evaluation

The BCAD circuit of Fig. 5 was built and tested with a small-scale BDSSCB having two common-source connected 1200-V, 10-A rated 0.1-cm^2 SiC JFETs. Selected BCAD components used are listed in Table 1 with designations corresponding to those of Fig. 5. An isolated DC-DC converter with adjustable output voltage regulation was built to provide JFET gate bias voltages of -34 V, resulting in JFET drain-to-source blocking voltages of 1200 V. Fig. 6

TABLE I. Selected BCAD Components

Component	Manufacturer	Value / Part Number
C1, C2	-	0.01 µF
D1, D3	Fairchild Semi.	1N4148
D2, D4	NXP Semi.	BZX79-C5V1
Q3, Q5	ON Semi.	2N6028
Q4, Q6	Fairchild Semi.	FDS9945
R1, R4	-	10 kΩ
R2, R5	-	2 kΩ
R3, R6	-	36 kΩ
T1, T2	Bourns	P500-G120-WH
U1, U2	NEC	PS2501-1

shows the schematic of the BDSSCB test circuit. An isolated DC power supply was used as a source, and a resistive load of 54 ohms was connected in series with the JFETs. A bidirectional snubber, considered part of the BDSSCB, was connected as shown in Fig. 3 with resistor and capacitor values of 51 kΩ and 0.15 µF, respectively. The test circuit power supply connections were interchanged for bidirectional evaluation.

The gate driver and BDSSCB were tested bidirectionally for bipolar gate current actuation. The BDSSCB heat sink temperature was raised to 80 ˚C to increase JFET conduction voltage drops, resulting in bipolar gate current at reverse conduction currents slightly above 10 A. The supply voltage of the test circuit was increased until the turn-OFF transition was observed at a BDSSCB current of 11.0 A. The drain connections of the BDSSCB were then reversed and the test was repeated. With BDSSCB current in the opposite direction, the turn-OFF transition was observed at 11.5 A. The 0.5-A difference in BDSSCB currents for driver actuation was not unexpected, and can be attributed to small differences in device parameters.

Waveforms from the first of the two described bipolar current actuated turn-OFF transitions are shown in Fig. 7. The top waveform shows the BDSSCB conduction current. The middle two waveforms (from top to bottom) correspond to the drain-to-source voltages of the forward conducting or blocking JFET (channel 3) and the reverse conducting JFET (channel 4). The reverse conducting JFET shows a negative drain-to-source voltage after turn-OFF, as it shares a small portion of the blocked circuit voltage. Although individual JFET turn-OFF transitions occur on the nanosecond time scale, the parallel bidirectional snubber slowed the total BDSSCB transition time to approximately 20 µs in this evaluation. In both directions, a 2-µs delay was observed between the turn-OFF of the forward and reverse conducting JFETs. These results confirm the functionality of the BCAD BDSSCB driver.

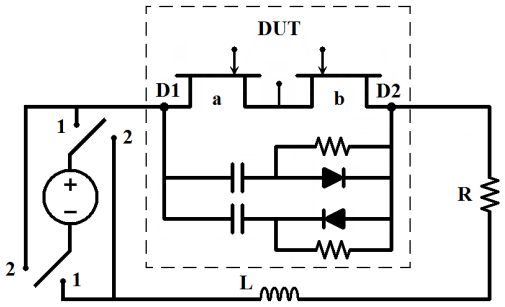

Figure 6. BDSSCB and test circuit schematic

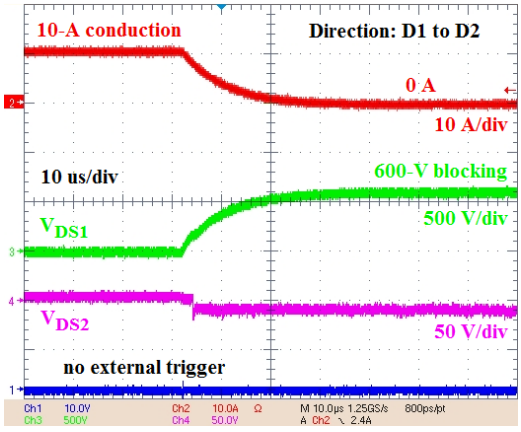

Figure 7. Bipolar current actuated turn-OFF (Ch1: active-high external trigger, Ch2: current, Ch3: forward JFET V_{DS}, Ch4: reverse JFET V_{DS})

VI. 600-V/60-A BDSSCB Demonstration

To evaluate the current scalability of the BDSSCB approach using parallel strings of common-source connected JFETs, multi-chip SiC JFET modules were fabricated. Three pairs of JFETs (6 devices) having a universally common-source, were packaged to form each 30-A module as shown in Fig 8. Following the successful evaluation of a single module, as discussed in [6], two such modules were connected in parallel for a 60-A BDSSCB demonstration. A larger implementation of the test circuit of Fig. 6 was used with the same bidirectional snubber connected across the paralleled modules to mitigate the transient voltage sourced by a larger series line inductance of 20 µH (100-kHz sinusoidal measurement). In the module evaluations, the series line inductance corresponded to a distribution bus length of 6 m (12-m total supply and return line loop).

Tests were begun with the BDSSCB in the ON-state at a fixed heat sink temperature of 30 ˚C. The test circuit supply voltage was raised in 100-V, 10-A test increments to a maximum 600 V, 60 A (36 kW) with a fixed 10-Ω resistive load. After the BDSSCB modules reached thermal equilibrium at each test condition, indicated by a load current drift of less than 0.1 A, the BCAD was triggered externally with a common input pulse for synchronized JFET turn-OFF. In the first set of tests, the supply provided current flow into side 1 (D1) of the BDSSCB. Subsequently, an identical set of tests was performed with the power supply polarity reversed for current flow into side 2 (D2) of the BDSSCB. Current and voltage waveforms of the BDSSCB turn-OFF transitions were nearly symmetrical across both test sets having opposite current directions. Figs. 9 and 10 show BDSSCB turn-OFF transition waveforms from the 600-V,

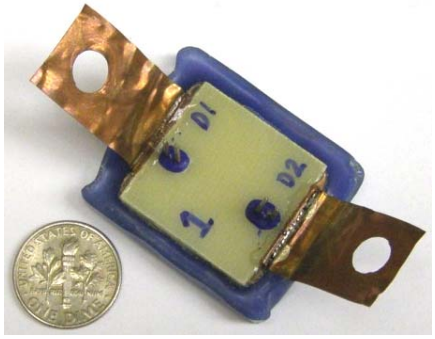

Figure 8. Packaged 30-A BDSSCB JFET module

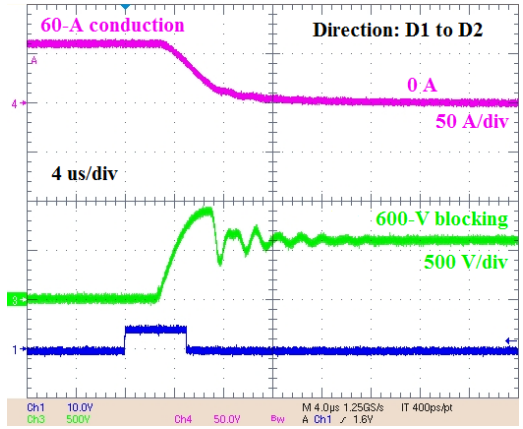

Figure 9. Current direction D1 to D2 BDSSCB 600 V, 60 A turn-OFF transition (Ch1: active-high external trigger, Ch3: BDSSCB voltage drop, Ch4: BDSSCB current)

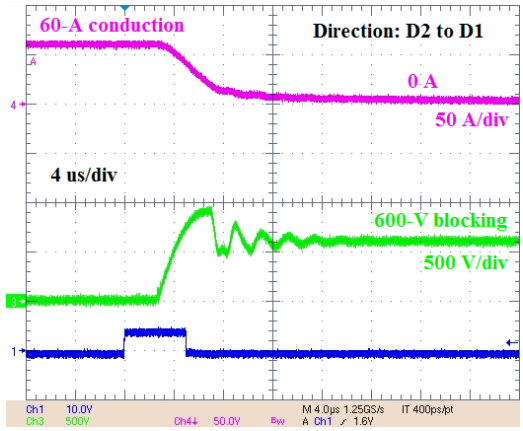

Figure 10. Current direction D2 to D1 BDSSCB 600 V, 60 A turn-OFF transition (Ch1: active-high external trigger, Ch3: BDSSCB voltage drop, Ch4: BDSSCB current)

60-A tests with current flow into side 1 and side 2, respectively, of the BDSSCB. In both tests, BDSSCB current was reduced from 60 A to 0 A in approximately 10 µs. The snubber module of the BDSSCB slowed the current transition less than in the small-scale (two common-source connected JFETs) 600-V tests due to increased line inductance and reduced load resistance. This caused an underdamped BDSSCB blocking voltage response having a peak of approximately 900 V (300-V overshoot), which remained sufficiently below the JFET 1200-V blocking capability. Results of these tests demonstrate that multiple parallel strings of common-source connected SiC JFETs share current and balance turn-OFF transitions with snubber components, thereby enabling the development of high performance scalable BDSSCBs using this approach.

VII. Summary

BDSSCBs can provide fault protection that is more reliable, and three orders of magnitude faster than mechanical fault protection devices. Many AC and bidirectional DC systems, especially those having power electronic components, stand to benefit significantly from these advantages. SiC normally-ON JFETs are well suited to the BDSSCB application due to their: normally-ON state, ability to bidirectionally conduct with low resistance in both the forward and reverse direction, positive temperature coefficient, and high operating temperature capability.

SiC 0.1 cm^2 JFETs were developed to have a more normally-ON characteristic specifically for a common-source BDSSCB design. This development allowed higher bidirectional conduction currents at a zero-volt JFET gate bias, and enabled bipolar gate current to be used as a means of detecting JFET over-current conditions, while inherently compensating for device temperature. A novel BDSSCB gate driver was designed for bipolar current actuated, or externally actuated turn-OFF. The BCAD driver was evaluated successfully on a small-scale 10-A BDSSCB, with current flow in both directions, having two common-source connected 0.1-cm^2 SiC JFETs.

Finally, the current scalability of the BDSSCB design using multiple common-source connected JFETs placed in parallel was demonstrated with two 30-A BDSSCB JFET modules. Turn-OFF tests were run with BDSSCB current flow in both directions over a load range from 10 kW to 36 kW (600 V, 60 A). Turn-OFF transition times of approximately 10 µs were achieved with a bidirectional RCD snubber and a series line inductance of 20 µH.

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