The Formulation and Implementation of an Analog/Digital Control System for a 100-kW dc-to-dc Buck Chopper

R. W. Ashton, J. G. Ciezki, and C. Mak

Abstract—The authors present a description of the design and implementation of an analog-to-digital controller for a 100-kW Ship Service Converter Module that is being used in a U.S. Navy reduced-scale dc zonal electric distribution system. The system requirements, control law, controller modes of operation and validation studies are documented.

I. INTRODUCTION

The remarkable increase in microprocessor technology, coupled with the development of high-power semiconductor devices, has fueled industry-wide interest in employing electromechanical actuators and power electronic converters in terrestrial, aerospace, and marine systems [1]–[4]. An example of such a move toward more-electric technology is the investigation by the Naval Surface Warfare Center (NSWC) into an integrated power system (IPS) for the 21st century naval combatant vessels. The proposed system incorporates a dc zonal electrical distribution system (DC ZEDS). Evaluation of such a system by the Navy has shown that fight-through capability is increased, while real part count and cost are both decreased. An integral part of the Navy's proposed dc distribution system is the Ship Service Converter Module (SSCM), which acts as a buffer between a main dc bus and a specific electrical zone in the ship. (A main bus, port, or starboard is powered from a rectified multiphase alternator which provides the benefit of decoupling prime mover speed and load frequency requirements.)

The authors are reporting on the development of two Reduced Scale Advanced Development (RSAD) 100-kW SSCM's for use at NSWC, Annapolis. The units were fabricated in a cooperative effort between Power Paragon Inc., Anaheim, CA, Lockheed Martin, Syracuse, NY, and the Naval Postgraduate School, Anaheim, CA. The authors were responsible for delivering two identical prototype SSCM controllers incorporating digital signal processing (DSP) technology.

Digital control was implemented utilizing a TMS320-based DSP card by dSPACE of Germany. A reprogrammable power electronics system development testbed was established by merging the prototype 5-kW buck chopper with a personal computer containing the dSPACE card and the Simulink program [5]. An algorithm was modeled in Simulink and downloaded to the dSPACE card for hardware-in-the-loop testing. This test was successful; however, the SSCM controller needed to be an autonomous single board solution. This dictated the use of another commercial board and finally the decision to build an in-house DSP unit.

The controller specifications include a local mode for maintenance and a remote mode controlled by an RS422 serial port. Other issues that were considered while prototyping were stability, paralleling, and fault analysis. Different closed-loop control strategies were analyzed to determine the most robust algorithm requiring the least amount of processing while satisfying the stability and transient specifications.

Manuscript received October 6, 1998; revised March 9, 1999. This paper was recommended by Guest Editors F. Maloberti and R. Newcomb.

R. W. Ashton and J. G. Ciezki are with the Naval Postgraduate School, Monterey, CA 93943 USA.

C. Mak is with Power Paragon Inc., Anaheim, CA 92805 USA.

Publisher Item Identifier S 1057-7130(99)05652-9.

Fig. 1. Power section of a buck chopper.

II. SSCM REQUIREMENTS

The power sections of the SSCM's are 100-kW buck choppers with a switching frequency of 5 kHz (see Fig. 1). The hard-switched units have an inductance of 1.35 mH and an output capacitance of 2.6 mF. The input dc voltage to the RSAD units is 850 V $\pm$ 25 V with a ripple frequency of 720 Hz. Source impedance specifications are not yet available. The units must be able to withstand input voltage transients up to at least 950 V. The general output specification includes four basic modes of operation: standby, regulated, adjustable, and local maintenance. Standby mode disables the output and is initiated when input or control power is first applied, when input power is interrupted, or if the mode is changed between regulated and adjustable. Regulated output mode maintains a fixed nominal voltage of 750 V but is adjustable from 700 to 790 V. In this mode, with the input voltage at either extreme, the output voltage must be within $\pm$ 25 V of nominal, including droop, when stepping the load from 50% to 100% and from 100% to 50%. This mode is also used for paralleling the units. The individual buck control units are not permitted to communicate during paralleling, and the total output buck capacitance consists of the combination of a known component and an unknown component. However, the unknown component is bounded and dependent on the number of attached loads. The adjustable mode is intended for use with a fixed value load resistance and must be stable and adjustable from 0 to 750 V. Finally, the local maintenance mode allows the SSCM to be operated without the use of the RS422 interface. In this mode the units may be operated independently or in parallel. Front panel switches and potentiometers are provided for this mode.

III. CONTROL LAW

Initially a low-cost DSP controller was specified to implement the chosen algorithm [6]–[9]. In order to limit processing, a number of simple control strategies were simulated and compared. The resulting control scheme derives the perturbation term for the duty cycle as follows:

$$\tilde{d}(t) = -h_I \tilde{i}_O(t) - h_V \tilde{v}_O(t) - h_N \int \tilde{v}_O(\varepsilon) d\varepsilon. \quad (1)$$

The load current $\tilde{i}_O(t)$, the output voltage $\tilde{v}_O(t)$, and the integral of the output voltage as listed in (1) are perturbation terms.

The perturbations in the load current were established by subtracting the slower moving inductor current $i_L(t)$ from the actual load current i_R . The inductor current is continuous for all loads greater than 9% of rated and required no filtering for application in (1).

The variation in the input voltage $v_{in}(t)$ was shown to create excessive ripple feedthrough at the output. Thus, a feedforward term was used to establish the base duty cycle $D_{SS}(t)$ by dividing the reference voltage (or desired output voltage) $v_{REF}(t)$ by the input

Fig. 2. Plot of the inductor current and output voltage during a transient. (a) From 100 to 50 kW at 0.4 s. (b) From 50 to 100 kW at 0.5 s.

voltage

$$D_{SS}(t) = \frac{v_{REF}(t)}{v_{in}(t)}. \quad (2)$$

Additionally, the output reference voltage was modified by subtracting a portion of the load current from a set dc reference voltage V_{REF} to create droop for paralleling

$$v_{REF}(t) = V_{REF} - \frac{i_O(t)}{10}. \quad (3)$$

The amount of droop was fixed at 1 V per 10 A. Since there could be no communication between the two units, other paralleling schemes were not investigated in this endeavor. Therefore, the final overall duty cycle algorithm is a modified multiloop control with feedforward and droop given by

$$d(t) = D_{SS}(t) - h_I[i_L(t) - i_O(t)] - h_V[v_O(t) - v_{REF}(t)] - h_N \int^t [v_O(t) - v_{REF}(t)] dt. \quad (4)$$

As a note, variations of the final algorithm included an adaptive system, which adjusted gains based on bus capacitance and output power level. The bus capacitance was determined through a constant current ramp during start up. This more complicated algorithm did not significantly improve transient response and required more processing time. It was ultimately abandoned for the simpler algorithm listed in (4).

Several standard protection functions were included. A pulse-by-pulse current limit at 250 A protects the 400-A 1700-V IGBT's. A current-limit time-out circuit was set to trip at 125% load after 2 s, and at 150% load after 1 s. However, any current in excess of 100% load (133 A) will eventually time out, based on the percent overload. An over-temperature trip, monitored at the heatsink, was set at 70 °C. This temperature was established by carefully monitoring the operation of an IGBT during a thermal-failure experiment. Lastly, a loss of control voltage for the power section was deemed to be catastrophic and required the inclusion of a shutdown circuit that trips at -10% nominal.

The drifting of the PWM frequency with respect to the crystal frequency of the DSP board when paralleling two converters created a beat-frequency as a result of the moving inductor current. Locking the PWM oscillator to the DSP board clock with a phase-locked-loop circuit ensured that the inductor current was sampled at the same location every cycle and eliminated this problem.

IV. SIMULATION RESULTS

The state-space averaged and detailed-switching model of the converter with the modified multiloop controller were constructed in Simulink. The poles of the state-spaced averaged model can be derived from the system matrix expressed in (5), shown at the bottom of the page. Conversely, gains may be uncovered by selecting appropriate poles and using (6)–(8)

$$h_I = \frac{L}{V_{in}} \left(k_2 - \frac{1}{RC} \right) \quad (6)$$

$$h_V = \frac{LC}{V_{in}} \left(k_1 - \frac{1}{LC} \right) \quad (7)$$

$$h_N = \frac{k_0 LC}{V_{in}}. \quad (8)$$

In (6)–(8), the nominal input voltage V_{in} is 850 V, and k_0 through k_2 are determined by pole placement in conjunction with the desired polynomial

$$s^3 + k_2 s^2 + k_1 s + k_0. \quad (9)$$

Poles that produced negative or complex gains, or were not at least one decade below the switching frequency, were not considered in this study.

After a number of simulation runs, which considered operating conditions from 10% to 100% load and various values of bus capacitance, the following poles were chosen using a full-load resistance of 5.625 Ω

$$s_1, s_2 = -276 \pm j159 \text{ r/s} \quad \text{and} \quad s_3 = -3106 \text{ r/s}.$$

As can be seen, the magnitudes of s_1 and s_2 are ten times smaller than s_3 and 100 times smaller than the switching rate (5 kHz). These poles result in the following gains:

$$h_I = 0.00646; \quad h_V = 0.00717; \quad h_N = 1.47.$$

$$\frac{d}{dt} \begin{bmatrix} i_L \\ v_O \\ d \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} & \frac{V_{in}}{L} \\ \frac{1}{C} & \frac{-1}{RC} & 0 \\ \left(\frac{-h_V}{C} + \frac{h_I}{RC} \right) & \left(\frac{h_I}{L} + \frac{h_V}{RC} - \frac{h_I}{R^2 C} - h_N \right) & \frac{-h_I V_{in}}{L} \end{bmatrix} \begin{bmatrix} i_L \\ v_O \\ d \end{bmatrix}. \quad (5)$$

Fig. 3. State-space averaged Simulink model of the converter and controller.

With these gains, the load resistance at $R = 22.5 \Omega$ and the total output capacitance set at 10.4 mF, the poles shifted to the following locations:

$$s_1, s_2 = -62 \pm j137 \text{ r/s} \quad \text{and} \quad s_3 = -3,469 \text{ r/s}.$$

Further, when adding droop for parallel operation, pole locations were not significantly influenced.

The algorithm is robust and not particularly sensitive to load capacitance. In addition, the algorithm is stable for constant power loads, even if the inductor current becomes discontinuous. Fig. 2 shows a plot of the inductor current and the output voltage for a step change in the load from 100 to 50 kW at 0.4 s and 50 to 100 kW at 0.5 s. The averaged Simulink model, illustrated in Fig. 3 at the very end of this brief, was used for this plot. As can be seen, the output voltage transient was less than ± 3 V. In addition, a settling time of less than 70 ms was deemed satisfactory.

V. HARDWARE IMPLEMENTATION

The controller has the capability to be placed in either analog or digital mode. The analog section of the unit is capable of all functions, while the DSP section requires the analog protection circuitry and the PWM chip.

The analog section consists of ten integrated circuits (IC's) and an assortment of discrete components. The main control law is implemented on one quad op amp with the aid of an analog voltage multiplier for the feedforward term. The DSP card interface is accomplished with use of a 26- and a 40-pin ribbon cable while the power unit is accessed through a 25-pin D-sub connector. To guard against ground-loops and noise, the analog card establishes a common ground point, and buffers all current and voltage sensor signals. The sensors in the power section are all floating with twisted-pair connections to the D-sub connector. The scaling factor for the

Fig. 4. Plot of the output voltage for a single SSCM during a transient from 50 to 100 kW and from 100 to 50 kW (10 V/div and 0.1 s/div).

Hall effect current sensors is 1 V/50 A and the voltage sensors is 1 V/100 V. The control law will either be implemented by the DSP board or the analog circuitry, depending on the position of a user provided hardware jumper.

An autonomous single-board TMS320-based DSP controller by Innovative Integration was the first step toward a digital solution [10]. This card was initially tested on slower speed hardware without incorporating any serial port operation. Because preliminary results were satisfactory, the cost was low and no other commercial boards matched the perceived needs as well, development proceeded with this board. Unfortunately, at the project completion time, the DSP board was found to be inadequate for this application. The number of wait-states required for accessing the A/D converters delayed the

Fig. 5. Plot of the output voltage for two parallel SSCM's during a transient from 100 to 150 kW and from 150 to 100 kW (10 V/div and 0.1 s/div).

speed of the algorithm significantly. Therefore, the card was not used for the main control algorithm, but was used to set the converter switching frequency, monitor-sensored voltages and currents, and establish an RS422 port. With the control law jumper in digital mode, the chopper operated, but was unable to maintain a nominal output voltage within ± 25 V, given a 50% step load change. Further, when paralleling two units while operating in regulated mode, the output voltage oscillated at approximately 1 Hz (the frequency difference between each of the SSCM control units' crystal clocks). A final complete digital solution is now being implemented using a programmable universal controller developed at NSWC. The new digital card is the subject of a future paper.

VI. EXPERIMENTAL RESULTS

The SSCM with analog control was found to satisfy all system specifications during each hardware test. A step load change of 50%–100%–50% caused a transient in the output voltage (750 V nominal) of less than ± 7 V, as shown in Fig. 4.

The transient performance of the two SSCM units operating in parallel is documented in Fig. 5 for a step load change of 100–150–100 kW. The output bus voltage transient decays rapidly with a variation of less than ± 5 V from the nominal value. While paralleling the units at 200 kW, the output current was matched to within 1%. However, at 25 kW, which is near discontinuous conduction, the matching was only within 15%, but quickly improved to within 3.5% as the power level was increased to 50 kW. The mismatch at low power levels is more pronounced, since the converters were calibrated at full load. Consequently, there is a small variation in the droop slope between units.

Isolated units remained stable over all ranges of voltage and power. The units operating in the discontinuous region had significantly longer settling times and larger output voltage transients when given step load changes.

VII. CONCLUSION

The U.S. Navy has selected dc distribution and a more-electric approach for the 21st century surface combatant vessels. The SSCM

is a crucial component in the DC ZEDS, and this first set of units has established a landmark for future endeavors. Control algorithms were evaluated based on specification requirements and implementation issues. DSP hardware was iteratively designed to meet all transient and paralleling requirements. Further, the units are now being retrofitted with a programmable universal controller that is TMS320 based. This will present a totally digital solution for the controller and allow flexibility in algorithm modification.

REFERENCES

- [1] T. Dade, "Advanced electric propulsion, power generation, and power distribution," *Naval Eng. J.*, vol. 106, no. 2, pp. 83–92, Mar. 1994.
- [2] C. Petry and J. Rumburg, "Zonal electrical distribution systems: An affordable architecture for the future," *Naval Eng. J.*, vol. 105, no. 3, pp. 45–51, May 1993.
- [3] N. Doerry and J. Davis, "Integrated power system for marine applications," *Naval Eng. J.*, vol. 106, no. 3, pp. 77–90, May 1994.
- [4] J. Mayer and F. Salberta, "High-frequency power electronic converter for propulsion applications," Dept. Elect. Eng. Applied Res. Lab., Pennsylvania State Univ., University Park, PA, Jan. 1997.
- [5] J. Dabney and T. Harman, *Mastering SIMULINK 2*. Englewood Cliffs, NJ: Prentice-Hall, 1998.
- [6] P. Liu and P. Sen, "A novel method to achieve zero-voltage regulation in buck converter," *IEEE Trans. Power Electron.*, vol. 10, pp. 292–301, May 1995.
- [7] B. Choi, B. Cho, F. Lee, and R. Ridley, "Three-loop control for multimodule converter systems," *IEEE Trans. Power Electron.*, vol. 8, pp. 466–474, Oct. 1993.
- [8] F. Garofalo, P. Marino, S. Scala, and F. Vasca, "Control of DC-DC converters with linear optimal feedback and nonlinear feedforward," *IEEE Trans. Power Electron.*, vol. 9, pp. 607–615, Nov. 1994.
- [9] J. Kassakian, M. Schlect, and G. Verghese, *Principles of Power Electronics*. Norwell, MA: Addison-Wesley, 1991.
- [10] *SBC31 Hardware Manual*, Innovative Integration, Westlake Village, CA, 1994.

RF Low-Noise Amplifiers in BiCMOS Technologies

Flora Carreto-Castro, Jose Silva-Martinez,
and Roberto Murphy-Arteaga

Abstract—This paper deals with the design of low-noise amplifiers (LNA) fabricated in BiCMOS technologies. The LNA's are based on an active inductor, which makes the topologies less sensitive to temperature variations and reduces the effects of process parameter tolerances. Experimental results show a 10-dB voltage gain at 1 GHz and unity-gain frequencies of 3.6 GHz. The noise figure, measured at 1 GHz, is 3.4 dB. The preamplifier has been fabricated using a 10-GHz BiCMOS technology.

I. INTRODUCTION

Due to the growing demand for monolithic radio frequency (RF) receivers for wireless communications, much attention has been paid to the design of low-noise amplifiers (LNA's) and mixers

Manuscript received October 16, 1998; revised March 12, 1999. This work was supported in part by CONACYT under Contract 2112-90-5-CO32A. This paper was recommended by Guest Editors F. Maloberti and G. Roberts.

The authors are with the National Institute for Astrophysics, Optics, and Electronics, Electronics Department, Integrated Circuits Design Group, 72000 Puebla, Mexico.

Publisher Item Identifier S 1057-7130(99)05650-5.