Circuit Improvements for a Voltage Multiplier

V.K. Semenov and Yu. A. Polyakov

Abstract—A voltage (or flux) multiplier is a device which multiplies applied SFQ pulses. Due to the quantum nature of an SFQ pulse the device can be used as a voltage (or flux) amplifier with a fundamentally accurate (integer) gain. Earlier we showed that the device can be used for improvement of dc and ac voltage standards. Recently we have found that a long voltage multiplier can display complex dynamic behavior, which can lead to undesirable collective oscillations. This report is devoted to theoretical optimization and experimental investigation of long voltage multipliers connected in series for dc current. Experimentally we have obtained accurate current steps with about 0.1 V voltage drop for a 5 mm x 5 mm chip fabricated in Nb technology and tested at 4 K.

Index Terms—AC Voltage Standard, Flux amplifier, Quantum metrology, Programmable Voltage Standard.

I. INTRODUCTION

A few years ago we presented experimental results of our investigation of a prototype superconducting Digital-to-Analog Converter (DAC) based on processing Single Flux Quantum (SFQ) pulses [1, 2]. Two unique features make the device potentially attractive for metrology applications: i) The generation of output voltage is based on the fundamentally accurate Josephson frequency-to-voltage relationship. ii) The device contains its own frequency multipliers and therefore dramatically lower frequencies, a few hundred megahertz rather than tens of gigahertz, can be utilized as the external reference frequency. We expected that the DAC would become a key component of novel standards and calibrators of ac voltage with frequency up to 1 MHz. However, the implemented prototype had small (about 10 mV) output voltage which was far lower than the expected 1 V to 10 V target magnitude. More importantly, we found that the generated voltage did not agree well with the expected quantized values. At the time we believed that both flaws could be fixed easily, but it took about two years to find the origins of those deviations from the Josephson frequency-to-voltage relationship. As a result we made significant progress in the quality of the primary components of our DAC. However, the whole system is still not ready for testing at a metrology lab. So, this manuscript is a kind of a

progress report on the development of our fundamentally accurate digital-to-analog converter.

There are two competitive techniques to synthesize very accurate waveforms and utilizing unique properties of overdamped Josephson junctions. One of them is using only voltage reproducers (or voltage multipliers with the gain equals to one). These voltage reproducers are rather simple; in fact, they are either two [3] or three [4] junction interferometers. However, the simplicity of the technique has evident back side: much larger parasitic capacitance between the injectors and the reproducers, which dramatically shunts high-frequency components of the synthesized waveforms.

Fig. 1. Block diagram of DAC based on processing SFQ pulses.

The other technique originated from a conventional voltage standard based on synchronization of an array of Josephson junctions by an external wave. But now the

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external wave is not a sine wave but a train of very short pulses. Each pulse causes 2π leaps in the every junction of the array. The required variation of the output voltage is provided by corresponding variation of the frequency of these pulses. The known experimental results are rather promising [5, 6]. The major drawback of this technique (from our point of view) is extremely high requirements for the hardware that provide generation of short pulses with non-uniform time intervals and their propagation along the Josephson junction array.

II. DAC DESIGN

The DAC based on processing SFQ pulses [7] consists of (see Fig. 1) a frequency multiplier and a frequency divider providing two local reference frequencies; a set of RSFQ based [2] frequency synthesizers SD controlled by an external input code; and a set of voltage amplifiers with integer gains or Voltage Multipliers (VM) [7-9]. Operation of the DAC is based on the Josephson frequency-to-voltage relationship. Namely, SFQ pulses generated by a synthesizer with a variable frequency (that may be as high as 50 GHz for our recent implementation based on 1 kA/cm² fabrication technology at HYPRES, Inc.) and are converted to a proportional variable voltage (that may be as high as 0.1 mV) by the first Josephson junction of the VM. All the VMs, which may have different gains and be fed by different synthesizers, are ac coupled with the digital circuitry and therefore can be connected in series for dc current, so the output voltage produced by the DAC is the sum of the partial voltages produced by the VMs.

III. FREQUENCY MULTIPLIER

Fig. 2. The structure of the pulse multiplier that effectively doubles the frequency.

An elementary frequency multiplier (Fig. 2) also utilizes the Josephson frequency-to-voltage relationship. It is based on the duplication of SFQ pulses generated by junction J1. It is easy to show that the pulse repetition frequency is accurately duplicated. A low-pass filter (right side in Fig.2) should convert these SFQ pulses to dc voltage so that the SFQ pulses generated by the junction in the next elementary multiplier are separated by uniform time intervals. However, because of thermal fluctuations SFQ pulses are generated by junction J1 with significant time jitter. In other words, the frequency multiplier probably has a significant phase noise. Underestimation of this noise was one of our misjudgments.

IV. VOLTAGE MULTIPLIERS

A. Design

Fig. 3 shows three main stages of our latest version of the voltage multiplier. The injector (INJ) allows pulses to be transfer or "injected" into a floating (galvanically isolated) VM. The regular stage (REG) [3] operates as an elementary voltage source with the voltage drop corresponding to the frequency of passing SFQ pulses. It also transmits SFQ pulses to the next stage. Both stages are situated between superconductor films, which have several superconducting connections near its edges. The third stage (CHK) uses two galvanically isolated shields and behaves as two REG stages.

Fig. 4 shows a possible connection of the fragments in the voltage multiplier as well as its major parasitic capacitances and inductances. First, we would like to note that CHK cells break the ground plane into islands to choke low frequency parasitic oscillations [1].

Fig. 3. Notations and equivalent circuits of the basic stages of the voltage multiplier. The stages are situated between two peripherally shorted superconductor films. These superconductor boxes are shown by dashed lines.

B. Theory

The inductive parasitics of the voltage multipliers are another reason for the improper operation of our first devices. In [10] we pointed out that a variation of the delay τ in propagation of SFQ pulses along a circuit leads to the variation of average magnetic flux. The inductance L corresponding to this effect could be defined as the first derivative of the magnetic flux over current:

$$L = \langle d\Phi / dI \rangle = (f \cdot \Phi_0) \cdot (d\tau / dI_b), \quad (1)$$

where f is the frequency of SFQ pulses and I_b is the bias current of the circuit. For a single VM stage, this inductance is about half of the Josephson inductance associated with an effective critical current of this stage: $L_j = \Phi_0 / I_c$.

Fig. 4. Connection of two voltage multipliers activated by a common source of SFQ pulses via terminals IN. Both multipliers are connected in series for dc bias I_b .

A problem arises when Eq. (1) is applied to multi-stage multipliers. For example, the second stage adds a further delay to the already delayed SFQ pulses. This means that the total delay for n multipliers is $n\tau$. A simple generalization of this observation leads to the conclusion that despite the physical identity of all stages, the inductance of the n -th stage is n times larger than the first one: $L_n = n \cdot L$. The extra inductance is induced by all previous stages. Thus if all stages have inductance L , then each stage is magnetically coupled to all foregoing stages, but it is not coupled with the subsequent stages:

$$L_i = L, \quad M_{i,j} = L, \quad M_{j,i} = 0, \quad i > j. \quad (2)$$

This equation indicates the unusual inductive properties of

these voltage multipliers. Note that conventional software packages are not suitable for an electromagnetic analysis of the system because of unequal values of mutual inductances $M_{i,j}$ and $M_{j,i}$.

C. Experiments

Most of our $5 \times 5 \text{ mm}^2$ chips contain an array of 24 voltage multipliers each having gains 32 times. Maximum voltage drop per stage is about $80 \mu\text{V}$, which is achieved at 40 GHz pulse repetition frequency. The total gain of the array is 768 which corresponds to an output voltage of about 60 mV. The whole array structure occupies an area of about 5 mm^2 (or 20% of the chip area), giving a specific voltage drop of about 1.5 V/cm^2 . Chips are manufactured using 1 kA/cm^2 HYPRES, Inc. fabrication technology. We tested about 20 designs with different variations of the parameters discussed above.

Fig. 5. Detection of the phase noise of the reference signal in section with lengths 96, 192, ..., 768. The effect has been observed only at relatively low frequency, say, below 10 GHz.

The parasitics shown in Fig. 4 are responsible for parasitic resonances. SFQ pulses passing through voltage multipliers can excite undesirable oscillations at these resonant frequencies. As a result the multipliers are biased by ac as well as dc currents causing the multipliers to operate incorrectly. As we showed above, the total inductance of multipliers depend on many parameters (including dc bias). All together, this leads to the appearance of a reproducible fine structure along the current range of what should be a horizontal voltage step. This structure was removed by inserting resistive strips between the voltage multipliers. The next effect is a self-detection of the phase noise. According to Josephson frequency-to-voltage relationship the noise is converted into a high-frequency voltage noise, which induces ac currents flowing in particular via capacitors CJ (Fig. 4). This current increases if a larger number of voltage multipliers is activated. The effect can be observed as a rounding of current step, which is proportional to the number of activated voltage multipliers as shown in Fig. 5.

Fig. 6. Accurate measurement of current steps, showing repeated traces with random noise corresponding to an accuracy of ~ 100 nV. During the measurements we did not observe any deviation from a quantized horizontal voltage step.

Fig. 7. The current range can be reasonably wide $\sim \pm 17\%$. It has been shown experimentally that the range of the current step can be increased if a few voltage multipliers are connected in parallel.

Fig. 8. Output characteristics of voltage multiplier showing multiple current steps for high voltages. The input voltage is changing from 0 to 100 μ V in 5 μ V steps. (A voltage of 60 mV corresponds to about 1.5 V/cm² specific voltage.)

Fortunately most of these problems have been resolved by reducing the phase noise of frequency multipliers and damping resonant oscillations. The next 3 figures illustrate correct operation of the whole structure: Voltage steps are accurate (Fig. 6), wide (Fig. 7) and be located at high voltage (Fig. 8).

V. PROGRAMMABLE VOLTAGE STANDARD AND DAC

We developed room-temperature interfaces for a programmable voltage standard and for a DAC. The former interface can hold up to twenty 5×5 mm² chips. It has been tested with two chips, while a 1 Volt demonstration would require about 17 chips.

The latter interface is fully assembled and passed all tests that can be carried out without superconductor chips.

VI. CONCLUSION

In the frame of the project we encountered several perplexing problems. One of them can be explained in terms of a dynamic mutual inductance, which is developed in voltage multipliers under influence of SFQ pulses. We think, this effect has independent scientific interest. We found also that the effective inductance of the voltage multiplier can be controlled by the frequency of SFQ pulses. Such a variable inductance can be used in future analog SFQ devices.

Finally we have demonstrated that a DAC based on processing SFQ pulses is a practical device, with near-term application to a fast high-precision programmable ac voltage standard.

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