Constant-Voltage Steps in Arrays of Nb-PdAu-Nb Josephson Junctions

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Abstract—Design and fabrication of Nb-PdAu-Nb trilayer Josephson junctions are described. The microwave response of an array of 1000 of these junctions was measured, and constant-voltage step heights were characterized as a function of the microwave amplitude and frequency. Experimental results fit well to point-junction simulations at the 3 GHz design frequency of the microwave distribution network. The observed step height of 3.8 mV shows that the array and microwave distribution are sufficiently uniform for application in programmable Josephson voltage standards.

I. INTRODUCTION

Superconductor-normal-superconductor (SNS) junctions are being developed for application in programmable Josephson voltage standards and for superconducting digital-to-analog (D/A) converters [1]. In particular, Nb-PdAu-Nb junctions have been demonstrated in prototypes of both sinusoidally-driven [1]-[3] and pulse-driven [4] programmable voltage standards. This paper describes the frequency and power dependence of constant-voltage steps for an array of 1000 Nb-PdAu-Nb junctions driven by a sinusoidal microwave drive.

Metallic-barrier junctions are ideally suited to voltage standard applications in a number of ways. First, since the conductivity of a normal-metal barrier is predominately real, SNS junctions have the required nonhysteretic current-voltage (I - V) characteristic. Second, because nonhysteretic junctions are available in high- T_c technology, circuit operation may be extended to temperatures above 4 K [5], [6]. Third, the large critical currents ($I_c > 1$ mA) available from SNS junctions provide greater stability against noise as well as greater output current. Finally, their characteristic voltages, or $I_c R$ products (where R is the junction resistance), are typically between 5 and 30 μ V and enable lower operating frequencies of 2.5–15 GHz.

A. Junction Design and Fabrication

We fabricate Nb-PdAu-Nb junctions using a trilayer that is dc sputter deposited in situ. The trilayers consist of a 220 nm Nb base electrode (BE), a 30–50 nm PdAu (53 % Pd:47 % Au by mass) barrier, and a 120 nm Nb counter electrode (CE). The SNS fabrication process is a simplified version of our standard Nb-Al-AlOx-Nb process [7], two major differences being that junction shunt resistors are unnecessary and the PdAu barrier requires a different wet etch. Figures

1(a) and 1(b) show the top and side views of the first five levels that define the SNS junction array. After the trilayer is deposited, the junctions are patterned with three successive etches. First, the $4 \mu\text{m} \times 4 \mu\text{m}$ Nb counter electrode is reactive ion etched using CF_4 and O_2 . The counter electrodes are protected with $5 \mu\text{m} \times 5 \mu\text{m}$ photoresist before the PdAu barrier is wet etched in 100 ml H_2O , 50 ml nitric acid, 50 ml acetic acid and 5 ml hydrochloric acid for 1 minute. Two counter electrodes are centered $6 \mu\text{m}$ apart center-to-center on a $6 \mu\text{m} \times 12 \mu\text{m}$ base electrode. The base electrode is reactive ion etched in SF_6 . SiO_2 is deposited to a thickness of 350 nm using an electron cyclotron resonance (ECR) deposition system. Via holes $2 \mu\text{m}$ in diameter are etched through the oxide to the counter electrodes by reactive ion etching with CHF_3 and O_2 that results in wall profiles sloped at 45 degrees. For optimal contact to the counter electrode, ion milling (or rf etching) of the wafer is performed in situ prior to sputtering of the 500 nm Nb wiring level (WR). The wiring level is then patterned and reactive ion etched with SF_6 to complete the series array connections between junctions on adjacent base electrodes. The final sixth level (not shown) is a lift-off level of 160 nm PdAu for contact pads and $2.6 \Omega/\text{square}$ resistors.

Fig. 1. Junction layout: (a) top view, (b) side view.

Electrical measurements on series arrays of 100 junctions with square counter-electrodes ranging from 1 to $12 \mu\text{m}$ in diameter were used to determine the junction current density J_c and counter electrode process runout. When calculating J_c we only use junctions with critical currents less than about 5 mA because they are small with respect to the Josephson penetration depth and can be considered point-like junctions [8]. For point-like junctions the critical current follows the form $I_c = J_c (d-b)^2$, where d is the design diameter and b is the total process runout. J_c and b are determined by plotting I_c vs. d . Using a 10% timed overetch, electrical

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measurements of junctions with different counter electrode dimensions show a typical counter electrode runout of $b = 0.25 \mu\text{m}$. Van der Pauw test structures were used to find the resistivity of the PdAu resistor level ($\rho = 41.7 \mu\Omega\cdot\text{cm}$ at 4 K), as well as process runouts for the base electrode ($0.5 \mu\text{m}$), wiring ($0.5 \mu\text{m}$) and resistor level ($0.2 \mu\text{m}$).

B. Circuit Design

In this paper, we describe results for a single 1000-junction array embedded in a coplanar waveguide (CPW) microwave test circuit. For programmable voltage standards, two of the most important requirements are the junction uniformity and microwave power uniformity across the array. In order to achieve power uniformity, three critical circuit conditions must be achieved. First, the junction array must be a small perturbation on the transmission line. This can be achieved if twice the transmission line impedance $\text{Re}(Z)$ is much greater than the total array impedance ($1000 R$). Second, the transmission line must be terminated with a matched load to prevent standing waves that are detrimental to power uniformity. Finally, to maintain power uniformity, the bias leads must appear as open circuits at the microwave design frequency.

Fig. 2. (a) Coplanar waveguide dimensions. (b) On-chip circuit schematic.

In our design, the array junctions are placed along the center conductor of a CPW transmission line, shown schematically in Fig. 2(a), that is designed to be 50Ω on a Si substrate. CPW is used instead of striplines because the larger ratio of line impedance to total array impedance maintains the required power uniformity through a larger number of junctions. CPW designs also require two fewer fabrication levels since the ground conductors can be patterned within the wiring level. The width of the center conductor is $w = 6 \mu\text{m}$, the gaps between the center conductor and ground are both $s = 3 \mu\text{m}$, and the ground conductors are both $g = 18 \mu\text{m}$ wide. The resulting 50Ω characteristic impedance is much larger than the impedance of an array of 1000 junctions, since the junctions have typical resistance of 1–4 m Ω .

Time domain reflectometry (TDR) measurements of an 11 cm length of this CPW transmission line at 4 K showed a 60Ω impedance. This is higher than the expected 50Ω due to process runout as well as the presence of thermal and ECR oxide on the substrate. A higher sheet resistance for the resistor level is thus required for matching the termination

resistors to the transmission line.

Since we need to bias the array and measure its voltage without losing or reflecting microwave power down the dc leads, we include a band stop filter on each lead that makes the lead appear as an open circuit at the design frequency. The filter is a quarter wavelength section of CPW that is capacitively terminated. The section is 1 cm long, has two 180° bends and one 90° bend, and was designed to be 85Ω ($w = 6, s = 24, g = 60$). The filter should appear as an open circuit at 3 GHz and at higher odd harmonics (9 GHz, etc.) TDR measurements showed that the impedance of this transmission line was actually 96Ω , slightly higher than expected for the same reasons previously cited. The termination capacitance was provided by a parallel-plate capacitor measuring $360 \mu\text{m} \times 360 \mu\text{m}$ with an SiO_2 dielectric estimated to provide a capacitance of 13 pF.

The resulting on-chip schematic circuit is shown in Fig 2(b). A single band-stop filter is placed at each end of the 1000-junction array. The distance between the two filters is approximately 7 mm. A semirigid coaxial cable couples microwaves from room temperature to a 50Ω CPW transmission line on a BeCu-clad FR4 finger board. BeCu spring fingers contact the PdAu-covered Nb pads on the $1 \text{ cm} \times 1 \text{ cm}$ chip. A $320 \mu\text{m}$ long Nb CPW taper was used between the pads and the array.

II. EXPERIMENTAL MEASUREMENTS

A. Microwave Frequency Characterization

When a sinusoidal current drive of frequency f is applied to a Josephson junction, the I - V curve exhibits equally spaced constant-voltage steps at voltages $V = nf/K_J$, where $K_J = 483\,597.9 \text{ GHz/V}$ and n is an integer. The appropriate bias condition for junctions in a sinusoidally-driven programmable voltage standard occurs when the microwave power is adjusted to simultaneously maximize the current heights of the $n = 0$ and ± 1 constant-voltage steps [1]. Kautz has shown that SNS junctions have maximum stability

Fig. 3. Current-voltage curves for the 1000-junction array without microwaves and at 3 and 9 GHz with the ac amplitude adjusted for equal step height.

against noise-induced phase slippage when the normalized frequency $\Omega = f/(I_c R K_J)$ is in the range 1–3 [2]. Comparing the step height ΔI_n and power required to achieve equal heights for the $n = 0$ and 1 steps at a given frequency, Kautz concluded that junctions with or without a ground plane have an optimum operating frequency $\Omega \approx 1$ [8]. For junctions larger than the Josephson penetration length λ_J , the maximum step height attainable is about 10 mA for a power of order $I_c f/K_J$ and occurs for a square junction of area $(4\lambda_J)^2$. Furthermore, Borovitskii *et al.* [9] have shown that the greatest tolerance of step position to critical current variation in arrays is obtained for $\Omega \approx 1$.

Our experimental 1000-junction array was first characterized without microwave power. As seen in Fig. 3, the I - V curve is nonhysteretic. The critical current of the array is 4.8 mA, using I_c of the junction with the lowest critical current. The 34 kA/cm² current density of these junctions corresponds to a Josephson penetration length of about 1.9 μ m, approximately half the junction diameter. Thus, these junctions may have some phase variation across their length and width due to finite junction size. The total array resistance is 1.3 Ω , yielding an average junction resistance of 1.3 m Ω and a junction characteristic voltage of 6.3 μ V. Thus, our junctions have a characteristic frequency of 3.0 GHz. Figure 3 also shows the array I - V curve with microwaves applied at the 3 GHz junction characteristic frequency ($\Omega = 1$) and at 9 GHz ($\Omega = 3$). The microwave power at each frequency is adjusted so that the current heights of the $n = 0$ and ± 1 steps are equal. These frequencies are shown because they are at the design frequencies of the band-stop filters. These characteristics are ideal for voltage standards.

Fig. 4. Equal step heights and required microwave power vs. frequency.

The array can be used to determine power uniformity along the 50 Ω transmission line. Figure 4 shows the equal step heights $\Delta I_1 = \Delta I_0$ as a function of frequency. The two lobes centered at 3 and 9 GHz reflect the transfer function of the band stop filters. At frequencies away from these center frequencies, the equal step heights decrease because the power coupled to the array is nonuniform due to standing waves in the array. For example, at 6 GHz and 12 GHz, the filters appear as short circuits rather than open circuits, resulting in

poor power uniformity to the array and correspondingly small step heights. Power nonuniformity can also be seen in the I - V curve by a change in slope at the ends of the constant-voltage steps.

The step height at 9 GHz is somewhat lower than at 3 GHz probably due to junction nonuniformity. Junction uniformity degrades step height more severely at higher frequencies because the steps are at higher voltages, and slight variations in junction resistance makes the current ranges of steps on different junctions less likely to overlap.

B. Microwave Amplitude Characterization

The frequency dependence of the required microwave power is determined by both junction dynamics and the microwave distribution circuit. The microwave power to our probe was measured with a 20 dB coupler and is plotted on the right axis

Fig. 5. $n = 0$ and 1 constant-voltage step heights vs. microwave current amplitude at (a) 3 GHz and (b) 9 GHz.

of Fig. 4. The required power peaks at 6 GHz and 12 GHz, where the filters appear as short circuits. The approximately linear rise as a function of frequency above $\Omega = 1$ is primarily due to the frequency dependence of the Bessel-function argument for the ac voltage-biased case, that is, the ac amplitude required for a given step height is expected to increase in proportion to the frequency. Other structure in the

plot of power vs. frequency is probably due to irregularities in microwave transmission through the probe and fingerboard.

By measuring the step heights as a function of microwave power at the design frequencies of the filter we can get a qualitative measure of the power and junction uniformity. Figure 5 shows the measured height of the $n = 0$ and 1 steps of the 1000-junction array as a function of microwave current amplitude. The experimental data are plotted against simulations of a single resistively shunted point junction for the same two normalized frequencies ($\Omega = 1$ and 3). The simulation method is described elsewhere [10]. The experimental ac current amplitude through the series array I_{ac} is approximated by $I_{ac} = \alpha V_{ac} / (1000 R + R_{term})$, where V_{ac} is the microwave voltage amplitude, R_{term} is the termination resistance, and α is the fraction of current transmitted from room temperature to the array. V_{ac} is measured at room temperature using a 20 dB coupler. The termination resistance was measured to be 54.4Ω , so that $I_{ac} = \alpha V_{ac} / 55.7 \Omega$. By fitting the 3 GHz data at the second zero of the $n = 0$ step, the resulting correction yields an experimental microwave power loss of -2.1 dB ($\alpha = 0.78$) from the room temperature input. The 9 GHz data are limited to $I_{ac} < 6I_c$ due to junction heating. Without a zero in the $n = 0$ step we could not determine a meaningful fit to the simulations, so the data are plotted without correction for any losses ($\alpha = 1$). Comparing the experimental data for the two different frequencies in Fig. 5, it appears that the 3 GHz data are closer to the simulation data than the 9 GHz data. Also the $n = 0$ step data for both frequencies match the simulation data better than the $n = 1$ step. Finally the experimental step heights at higher power appear lower than the simulation data. In summary, higher frequency (Ω), higher step number (n), and higher power all seem to show the largest deviation between the experimental and simulated step heights.

The differences between the experimental data and an ideal resistively shunted junction array are probably due to a combination of three effects. Junction nonuniformity, phase variation across the large junction area, and power nonuniformity resulting from a non-ideal microwave circuit may have all contributed to differences from the point-junction behavior. We did not attempt to ascertain which of these effects is most important here. Nevertheless, the 1000 junction array shows constant-voltage steps at 3 GHz ($\Omega = 1$) that are very nearly as large as those expected for a single point junction. Both the 3 GHz and 9 GHz equal step

heights are of sufficient size (≥ 3.4 mV) to be useful for the sinusoidally-driven programmable voltage standard. We conclude that larger arrays and similar filter designs are appropriate for programmable voltage standards.

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