Superconducting Integrated Circuit Fabrication With Low Temperature ECR-Based PECVD SiO_2 Dielectric Films*

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Abstract — **A superconducting integrated circuit fabrication process has been developed to encompass a wide range of applications such as Josephson voltage standards, VLSI scale array oscillators, SQUIDs, and kinetic-inductance-based devices. An optimal Josephson junction process requires low temperature processing for all deposition and etching steps. This low temperature process involves an electron cyclotron resonance-based plasma-enhanced chemical vapor deposition of SiO_2 films for interlayer dielectrics. Experimental design and statistical process control techniques have been used to ensure high quality oxide films. Oxide and niobium etches include endpoint detection and controlled overetch of all films. An overview of the fabrication process is presented.**

I. Introduction

This paper presents an overview of the state-of-the-art processes used at the NIST Superconducting Integrated Circuit Fabrication Facility, which supports a wide range of device applications and user needs. Some devices fabricated at the facility are used in metrological applications such as the voltage standard, calculable capacitor, infrared radiometer and ac-voltmeter. Other areas of interest include the study of array oscillators, infrared detectors, mixers and bolometers. The overall emphasis at our facility is flexibility. At our facility we employ a methodology that uses a combination of experimental design techniques [1-2] and statistical process control [3]. These studies have resulted in process improvements resulting in a reliable, standard process for multi-level, low-T_c device fabrication. In addition to our standard process, we continue to investigate exotic and novel process development which may ultimately serve the superconductivity community.

All photolithography for the processes is based on a commercial image reversal photoresist used in both positive and negative tone. We use an i-line commercial wafer stepper capable of producing 0.6 μm lines and spaces in the positive tone of the resist over a 76.2 mm (3 in) Si wafer. We have developed standard test reticles for measuring processing parameters such as run-out for each etch process. The standard mask set produces 400-junction series arrays that vary in junction area from 1 μm × 1 μm to 10 μm × 10 μm (used for measuring J_c), single junctions varying in area from 1 μm × 1 μm to 10 μm × 10 μm, and coil and crossover tests with 2 to 4 μm pitch. Nb-to-Nb wiring contacts are evaluated using arrays with via areas ranging from 0.5 μm × 0.5 μm to 4 μm × 4 μm. The mask set also includes capacitor tests, used to evaluate the oxide quality, covering areas ranging from 125 μm × 125 μm to 4 mm × 4 mm. Process runout, the difference between design and final dimensions, for each fabrication step is measured using Van der Pauw and cross-bridge test structures [4].

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II. Trilayer Process

A. Trilayer Deposition Process

Nb/Al-AlO_x/Nb trilayers are deposited in a dedicated load-locked vacuum system. The trilayer system uses 7.62 cm (3 in) dc-magnetron sputter guns for Nb and Al and a 3 cm ion mill gun. Wafers are heat sunk by clamping to Al pucks using In O-rings. The wafers are located 10 cm above the sputter gun targets. Wafer temperature during the trilayer deposition is lower than 77°C. The system is capable of handling 5 wafers per run. The load lock pressure is typically less than 1.3×10^{-4} Pa and that of the chamber is 1.3×10^{-5} Pa.

The intrinsic stress and transition temperature T_c of the sputtered Nb films have been characterized as a function of sputtering parameters and target erosion [5]. We can compensate for the shift in the zero-stress point toward lower cathode voltages as the target erodes. This shift is due to the fact that the zero-stress point is always characterized by the same linear cathode current versus Ar pressure I-P relationship for our system. For constant sputtering power, we can modify the Ar pressure to compensate for the shift of the zero-stress point.

The trilayer deposition is preceded by an ion mill cleaning of the wafer surface for 1 min. This is accomplished with a 3 cm ion mill located 15 cm below the wafers. The Ar pressure is 17 mPa (1.3×10^{-4} Torr), and the ion beam voltage is 350 V. For a 76 mm wafer, the accelerator voltage is 950 V. This spreads the ion mill beam to uniformly cover the entire wafer with a current density of approximately 0.15 mA/cm^2. Immediately after the ion mill cleaning, the 200 nm thick Nb base electrode is deposited at a nominal rate of 100 nm/min at 800 W of sputter power. A 15 min cooling step in argon is then used to ensure that the Al film is deposited on a cool substrate. The base electrode deposition is followed by the deposition of a 6–10 nm thick Al film at a rate of 0.6 nm/s. Al and Nb resistivity measurements are made periodically at room temperature and are used to monitor for potential target problems. For sufficiently high sputter power (>300 W), the room temperature resistivity of Al is approximately 3.4 μΩ·cm and of the Nb 15.2 μΩ·cm. The Nb thin film resistivity is close to that of the bulk Nb resistivity of 14 μΩ·cm. Oxidation is performed in the load-lock chamber in an 100% O_2 for 30 min in the standard process. For the high-J_c process, we use a mixture of 5% O_2 in Ar. Fig. 1 shows the J_c-versus-oxidation exposure E (pressure × time) for the standard trilayer process. The determination of J_c is accomplished using arrays of junctions and discussed in section VI. The wafers are returned to the main chamber after oxidation and the system is pumped back to the base pressure of 1.3×10^{-5} Pa.

A 50–100 nm thick Nb counter electrode deposition completes the trilayer process.

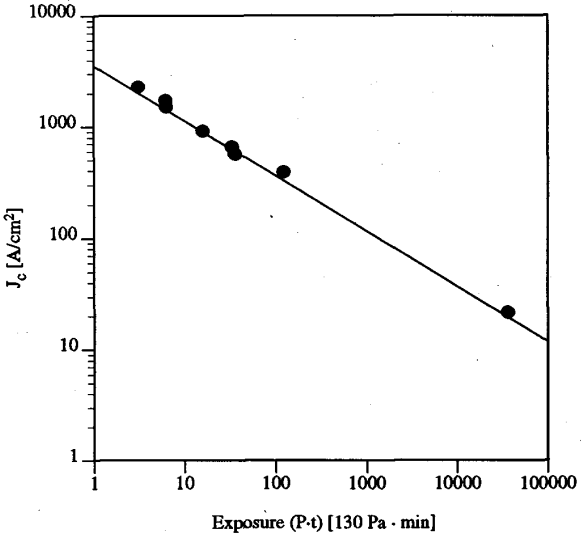

Fig. 1. Critical current density J_c versus exposure E (P·t) for the standard trilayer process. The data has a $J_c \propto (P{\cdot}t)^{-0.49}$ dependence.

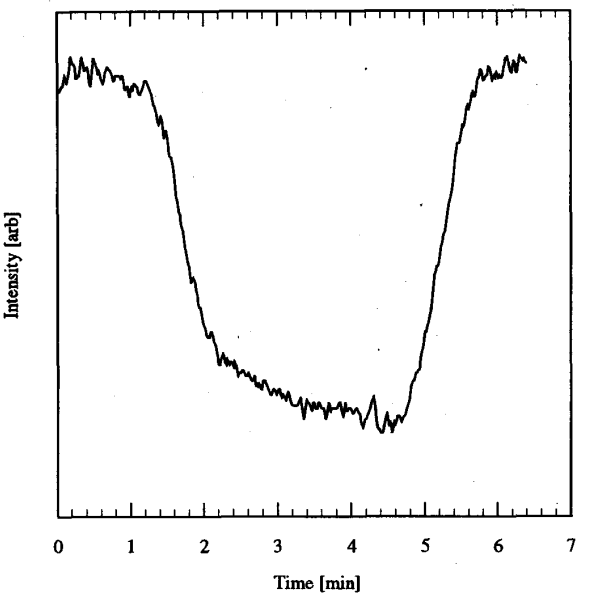

Fig. 2. A characteristic optical emission intensity curve for endpoint detection of the reactive ion etch, using SF_6, of Nb on SiO_2.

B. Trilayer Etch Process

The Nb counter and base electrodes are etched in a load-locked reactive ion etch (RIE) system. We have developed a reproducible Nb etch using a commercial optical emission spectrometer which is used for chamber conditioning and endpoint detection. The system is pumped to a base pressure of less than 6.5×10^{-5} Pa. Prior to loading the wafer, the chamber is conditioned by running the appropriate Nb etch process for a time determined by the intensity of a characteristic emission line. This RIE system is used for both Nb etching and photoresist/polymer ashing. A transient in the intensity of the characteristic emission line is seen even when there is no wafer to be etched in the chamber. We condition the chamber until the intensity transient approaches a steady state behavior resulting in a flat response, typically occurring in less than 20 min. The wafer is loaded into the etch chamber immediately after conditioning.

The counter electrode layer is etched in a 32.5 Pa gas mixture composed of 40 sccm CF_4 and 3 sccm O_2. The rf-power for this anisotropic etch is 25 W resulting in a -35 V self-bias voltage. The etch endpoint is determined by the intensity of the fluorine line at 705 nm. A characteristic emission intensity curve is shown in Fig. 2. The counter electrode etch process produces a nominal etch rate of 40 nm/min etch rate and we use a 10% overetch. The Nb counter electrode etch process was optimized using an orthogonal experimental design involving the effect of the RIE process on the junction quality V_m and junction noise [6].

The Al barrier layer is wet etched in a commercial wet etch consisting of nitric acid and phosphoric acid at 50°C for 15 s. The counter electrode areas are protected from the etch with a patterned photoresist layer.

The Nb base electrode layer is reactive ion etched using 40 sccm SF_6 at 6.7 Pa pressure and 25 W of rf-power. This

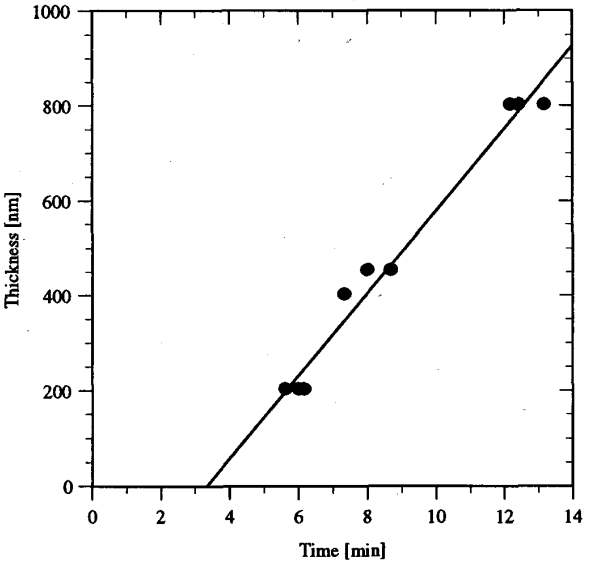

Fig. 3. The thickness versus etch time data show an effective startup time of approximately 3.3 min for the SF_6 reactive ion etch of Nb. The etch rate is approximately 80 nm/min.

process produces a nominal Nb/SiO_2 etch selectivity of 20 to 1. We have studied this etch process for wafers of varying thickness. The total etch time is determined by observing the intensity of the same fluorine line that is used for the counter electrode etch. The thickness versus etch time data presented in Fig. 3 clearly show an effective startup time of approximately 3.3 min and a Nb etch rate of approximately 80 nm/min. This is most likely associated with etch of the native oxide of the Nb base electrode.

The Nb etch is immediately followed by an O_2 ash process. We use 40 sccm O_2, 13 Pa pressure, and 50 W of rf-power, resulting in a -160 V self bias voltage in our system. This O_2 ashing removes polymerized photoresist layer formed during the Nb etch process. The photomask from the Nb etch is removed using a commercial N-methyl pyrrolidone (NMP)-based stripper at 90°C for 20 min followed by 5 min isopropyl alcohol and deionized water rinse. This process results in a run-out of approximately 0.4 μm.

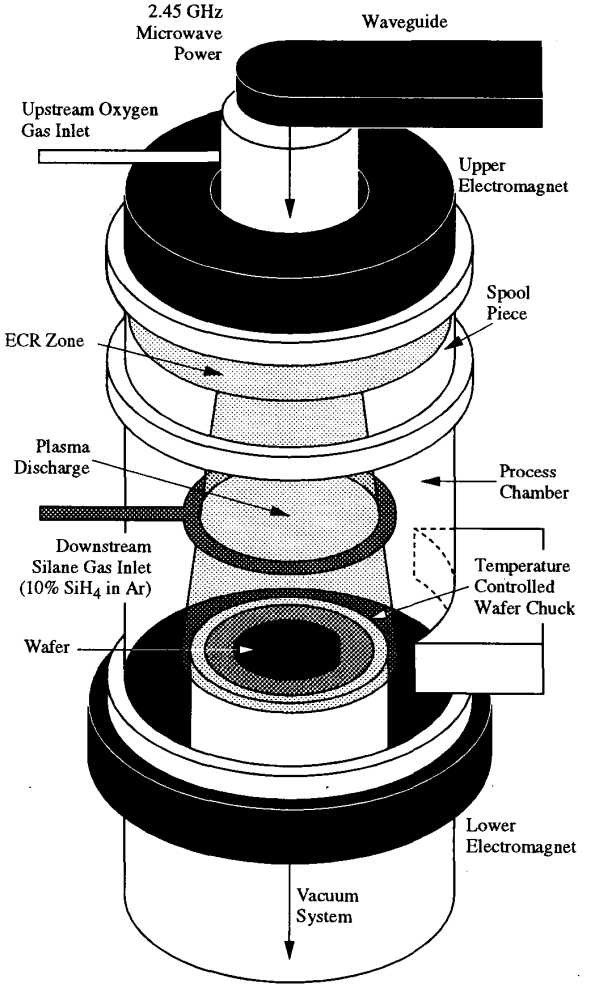

Fig. 4. ECR-based PECVD reactor configuration used for SiO_2 dielectric films.

III. Dielectric Layer Process

A. ECR-based PECVD Oxide

The maximum processing temperature allowable in any part of a superconducting integrated circuit process is determined by the thermal stability of Josephson junctions [7]. The critical current Ic decreases gradually with increasing temperature and annealing time, while V_m remains unchanged up to a "catastrophic" temperature, typically 180–250°C. This temperature depends on the quality of the Al-AlO_x barrier, which in turn is determined by the AlO_x and Al thicknesses, and the Al deposition rate and temperature during trilayer formation. We set the maximum allowable process temperature at 200°C for the circuits fabricated in our facility. Several groups have had reasonable success depositing "low temperature" oxides using plasma-enhanced-chemical-vapor-deposition (PECVD) at processing temperatures ranging from 180–200°C [8-10]. However, the oxide quality, namely the refractive index and film density, at these temperatures is typically much poorer than those films deposited at the nominal PECVD processing temperature of 350°C [11]. Problems have also been reported concerning oxygen diffusion into the Nb films resulting in decreased T_c. We have optimized an electron-cyclotron-resonance (ECR) reactor for PECVD of SiO_2 films at deposition temperature lower than 150°C. The resulting processes, involving deposition at ambient temperatures, produce high-quality SiO_2 films which are used as the dielectric layers in all circuits.

Fig. 4 shows a schematic of the ECR-based PECVD reactor that we use for the oxide depositions. The reactor consists of a turbomolecular-pumped load lock and a deposition chamber. The pressure of the system is typically less than 2.7×10^{-4} Pa prior to deposition, and the ultimate base pressure is 1.1×10^{-5} Pa. The ECR reactor uses an upstream electromagnet that produces the magnetic field for the resonance zone below the quartz window where the 2.45 GHz microwaves are launched. The upper magnet current, fixed at 185 A, produces the electron cyclotron resonance zone below the quartz window at 0.0875 T (875 G). O_2 and Ar gas mixtures are delivered into the ECR source with mass flow controllers. A high-density O_2/Ar plasma is formed in the ECR zone under the top of the chamber. The wafer sits on a graphite platen which is loaded from the load lock onto a temperature-controlled chuck in the center of the chamber. Silane (SiH_4), diluted to 10% in Ar, is injected directly above the wafer. Oxygen ions diffuse from the ECR zone toward the substrate and dissociate the SiH_4, producing SiO_2 on the wafer [12]. The lower magnet and rf-bias are not used in our standard deposition process. The oxide deposition is performed with the wafer at ambient temperature, typically 37°C. Temperature measurements were made using fixed-point thermometers fixed to the wafer surface during deposition.

A response surface methodology [13] was used to optimize the ECR system for high-quality, low-temperature oxide depo-

sitions [14]. The response variables in the study were deposition rate, uniformity, refractive index, film stress and wet-etch rate. We used the response surface to find desired regions of operation. We desire an oxide process which yields oxide layers having a refractive index equal to that of thermally grown SiO_2 (1.462), film thickness uniformity within 3% over a 76 mm wafer, deposition rates greater than 100 nm/min, a compressive stress less than 2×10^8 N/m^2, and wafer temperatures less than 150°C during deposition. The response surface predicts an operating point in the parameter space which yields the desired film properties. We conducted a confirmation study and have established an optimized process having an average deposition rate of approximately 108 nm/min, film thickness uniformity around 1.6%, compressive stress of 1.4×10^8 N/m^2, and a refractive index of approximately 1.458. We have measured the wafer temperature for oxide films with thicknesses ranging from 200 to 1000 nm. The wafer temperature does not exceed 138°C over this range.

We have generated system control charts for the refractive index using the standardized deposition process. The maximum variation in run-to-run deposition rate is 4.8% and 0.6% for refractive index. Since the oxide dielectric layer is common to all superconducting devices fabricated at our facility, this methodology provides a simple check that ensures process repeatability and reliability for the ECR deposition system.

We have found no degradation in the performance of Josephson junctions arrays fabricated with the ECR-based oxide. Breakdown voltages, measured for capacitors with areas greater than 4 mm^2 and 400 nm thick oxide films, typically exceed 100 V. Pinhole density measurements indicate pinhole densities less than 1/cm^2. Thick oxide films (~1 μm) are being used as wet etch masks for Si etching with potassium hydroxide (KOH) in devices requiring Si micromachining [15]. We are presently developing a planarization process using ECR-based oxide films. The planarization process involves etching the oxide using a commercial chemical-mechanical polisher. Recently high-quality, small-area Josephson junctions (less than 1 μm^2) were fabricated using the oxide in this planarization scheme. The etch rate reported is comparable to that of thermally grown oxide, and the results are promising [16].

B. Oxide Etch Process

A dedicated RIE system is used for etching vias in the oxide films. This system has an ultimate base pressure of 5.2×10^{-5} Pa and uses a nominal mixture of 47 sccm CHF_3 and 3 sccm O_2, 5.3 Pa chamber pressure and 150 W power resulting in a self-bias of -450 V. This process produces a nominal oxide etch rate of 40 nm/min. Process parameters must be chosen carefully to minimize polymer formation on the Nb films [17]. Endpoint detection is used with a 5% overetch to minimize polymer formation. The SiO_2 etch selectivity over Nb is approximately 10 to 1 for this process. Two methods have been established for oxide endpoint detection. One method uses the 518 nm optical emission line, while the other method relies on laser reflectance off the oxide and Nb surfaces. An O_2 ash is used following the oxide etch. This etch facilitates polymer removal from the surface of the photoresist and exposed Nb surfaces.

IV. Resistor Layer Process

A resistor sputter deposition process using a 99.95% pure Pd(47%)-Au(53%) alloy target is presently under development. The deposition system has three dc magnetron sputter guns for depositing Nb, Al, and Pd-Au. This provides flexibility for several processes under development for SNS junctions and multilayers. The system base pressure is typically less than 1.1×10^{-5} Pa. Nb contacts are cleaned in an Ar ion-mill for 2 min. The Pd-Au films were characterized by variation of Ar pressure and cathode power. The deposition rate is independent of pressure and proportional to the sputter power, 0.565 nm/(min·W). This rate is 4 to 5 times greater than typical Nb deposition rates. Both the room temperature and 4K film resistivity and sheet resistance of Pd-Au were determined with patterned van der Pauw test structures and 4-probe measurements (equally spaced by 1.27 mm) [18]. As shown in Fig. 5, the resistance is proportional to the inverse of the film thickness t_f. The resistivity of the films at room temperature and 4 K is approximately 42.2 μΩ-cm and 35.9 μΩ-cm, respectively. The resistivity has been found to be independent of sputter power which was varied from 50 to 800 W and indicates that the film characteristics are not influenced by the incorporation of impurities during deposition.

The intrinsic film stress is compressive and ranges from 2 to 4×10^8 N/m^2 for varying sputter power. No dependence of the stress on sputter parameters was observed. The stress and resistivity were not affected by variation of base pressure, in the range of $0.4-7 \times 10^{-5}$ Pa. A process using 1.55 Pa Ar and 700 W

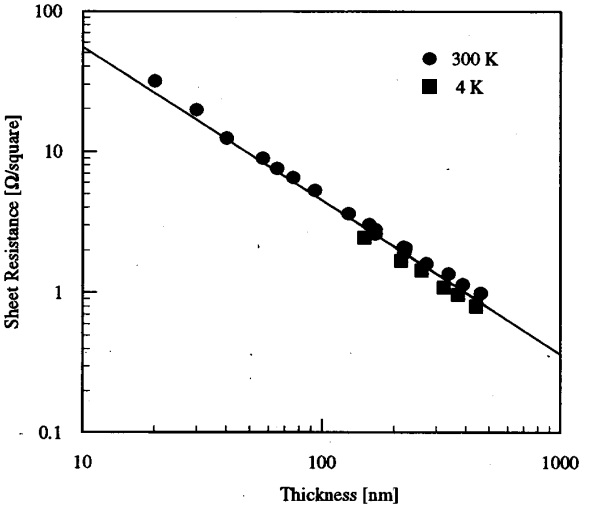

Fig. 5. Sheet resistance vs. film thickness for patterned Pd-Au resistors, measured at room temperature and 4 K. The resistivity at 4 K is approximately 85% of the room temperature resistivity. The data has a general $R_s \propto (t_f)^{-1.09}$ dependence, and t_f^{-1} dependence for $t_f > 150$ nm.

power provides a nominal sputter rate of 388 nm/min and a ~1 Ω/square sheet resistance for a 388 nm thick film.

Pd-Au films are subtractively patterned using a photoresist mask post baked at 120°C for 2 min. A wet etch process using 1:20:60 $HCl/HNO_3/CH_3COOH$ [19] yields a 80 nm/min etch rate and a process run-out of approximately 0.5 μm for a 200 nm thick film.

An alternative liftoff process using Pd(47%)-Au(53%) alloy films, deposited via e-beam evaporation, has also been developed. The Nb contacts are rf-sputter cleaned in-situ using 1.3 Pa Ar and -400 V self-bias for 10 min. The nominal Pd-Au deposition rate is 60 nm/min. The sheet resistance for a 130 nm thick film is approximately 2 Ω/square.

V. Nb Wiring/Contacts Process

The Nb wiring layer is sputter deposited in the trilayer sputtering system. Nb contacts are ion mill cleaned for 2 min using the process described above for pre-trilayer deposition. Approximately 6 nm of Nb is removed before depositing the Nb wiring layer.

The Nb wiring layer is sputter deposited immediately after the ion mill cleaning. A 600 nm Nb film is sputter deposited at 800 W of rf-power and at a pressure which provides a low stress film. The wafer temperature during deposition does not exceed 77°C for Nb films as thick as 1 μm. The Nb wiring layer is reactive ion etched using the same process as that used for the base electrode etch. The current density for the Nb-wiring-layer to Nb-contacts has been measured for 100-via arrays having nominal 1 μm^2 areas. The current density is typically greater than 5×10^5 A/cm^2.

Au contact pads are deposited by e-beam evaporation or thermal evaporation and patterned by liftoff. The Au film thickness is nominally 50 nm and the Nb contacts are sputter-cleaned using Ar.

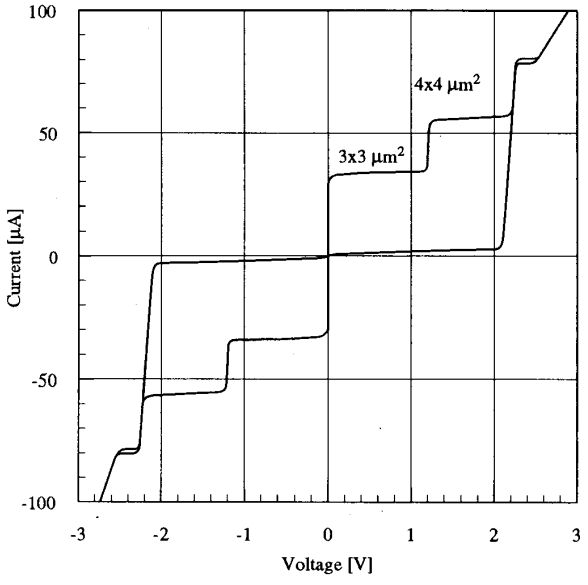

Fig. 6. Current-voltage characteristics for 400-junction series arrays of 3 μm × 3 μm and 4 μm × 4 μm junctions with 1σ-spreads in $\Delta I_c/I_c$ of 2.4% and 0.8%, respectively.

VI. Process Capabilities And Electrical Measurements

A. Process Runout Measurements/Critical Current Uniformity

Electrical measurements are made to determine most processing related runouts and characteristics. The counter electrode etch runout and critical current density is determined by measuring the IV-characteristics of at least two 400-junction series arrays having different junction areas. If two arrays on the same wafer, have mean critical currents I_{c1} and I_{c2} and design areas d_1^2 and d_2^2, then the counter electrode etchback, ε is

$$\varepsilon = \frac{d_2 - d_1 (I_{c2}/I_{c1})^{1/2}}{1 - (I_{c2}/I_{c1})^{1/2}} \quad . \tag{1}$$

Fig. 6 shows the IV-characteristics for two series arrays of 3 μm × 3 μm and 4 μm × 4 μm junctions. Using (1) we obtain a runout for the counter electrode etch process of approximately 0.3 μm. We can provide an estimate of the critical current density J_c for the process using the measurement of the process runout. The current density is given by

$$J_c = \frac{I_{c2}}{(d_2 - \varepsilon)^2} \quad . \tag{2}$$

This method provides a better estimate of current density over that of single junctions where uncertainties due to trapped flux and other deviations can lead to errors [20]. Using arrays, estimates of critical current uniformity can be made in terms of percent deviation at 1σ in $\Delta I_c/I_c$. For our standard process, the critical current uniformity for 2 μm × 2 μm, 3 μm × 3 μm and 4 μm × 4 μm are approximately 5.1%, 2.4%, and 0.8% respectively. This method for measuring the current density is superior to those that use large area junctions. For large junction areas, the process runout or etchback is typically ignored, and current uniformity through the junctions is determined by the Josephson penetration depth. This method is inconvenient for junctions having critical current densities greater than 5 kA/cm^2.

The process runout for the base electrode, wiring and resistor layers is measured at room temperature using cross bridges [21]. Fig. 7 shows a typical cross bridge schematic used in our standard process reticles. The sheet resistance, measured using the Van der Pauw cross, is calculated from

$$R_s = \frac{\pi}{ln2}\left(\frac{V_{cd}}{I_{ab}}\right) \quad . \tag{3}$$

The bridge resistor, used to measure the electrical linewidth W

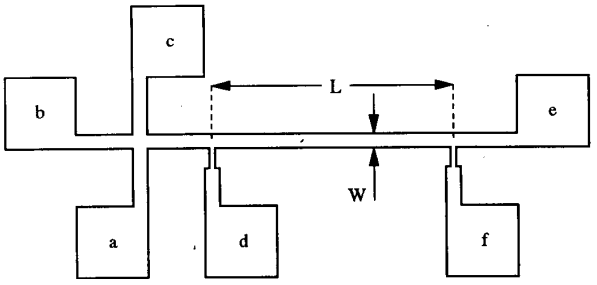

Fig. 7. Cross bridge schematic used in the standard mask set for process evaluation. The sheet resistance R_s is measured using the Van der Pauw cross between pads a, b, c and d. The bridge resistor, between pads d and f, is used to measure the electrical linewidth W, of the conducting channel. Typical cross bridge dimensions are L = 200 μm and W = 6 μm with 2 μm voltage taps on pads d and f.

of the conducting channel, is given by

$$W = R_s L \frac{I_{ae}}{V_{df}} \quad . \tag{4}$$

The process runout is calculated from

$$\varepsilon = W_{design} - W \quad . \tag{5}$$

These process runouts are particularly important for circuit designs which strongly depend on stripline inductances. In our standard process, the typical runouts for the 200 nm thick base electrode and 480 nm thick Nb wiring layers are approximately 0.4 μm and 0.9 μm respectively.

B. Device Applications

A typical IV-characteristic for a junction having a nominal 1.5 kA/cm^2 critical current density is shown in Fig. 8. The V_m for this 10 μm × 10 μm junction is approximately 78 mV.

NIST 10 V Voltage Standard Arrays are fabricated using a variant of the standard process. These devices contain over 20,000 trilayer Josephson junctions which are isolated from the a Nb groundplane by a 1 μm thick oxide layer. The low current density of 20 A/cm^2 required by these devices is achieved by oxidizing the Al barrier in 6.5 kPa O_2 for 12 h. These chips use Nb for all superconductive layers and SiO_2 for all insulating layers. Incorporating these materials into the devices has produced several measurable improvements over chips of the previous design which had lead-alloy wiring and SiO insulators. First, the yield has increased by a factor of two (from roughly 35% to 70%) because of fewer inherent defects in the materials. Second, these refractory materials make the chips much less susceptible to damage from humidity, condensation, and thermal cycling. Finally, these circuits are much less prone to trapping magnetic flux and exhibit a greatly reduced tendency to produce Shapiro steps under microwave irradiation with slopes or sloped tails.

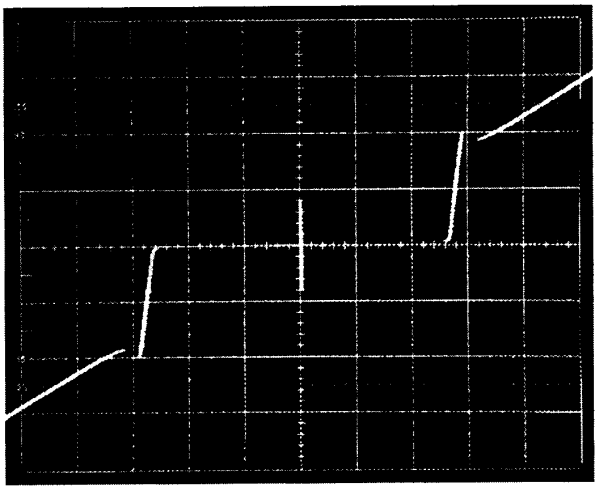

Fig. 8. Current-voltage characteristic for a single 10 μm × 10 μm Josephson junction having a nominal critical current density of 1.5 kA/cm^2 and a Vm of 78 mV. The y-axis is 50 μA/div and the x-axis is 1 mV/div.

We also routinely fabricate SQUIDs having input coils with 2 μm lines and spaces covering 1 mm^2 area. The ECR-based PECVD oxide films are conformal and prevent shorts between the coils and Nb washer. This was not previously possible using thermally deposited SiO.

Kinetic-inductance bridge thermometers have been developed for use in an infrared radiometric standard being developed at NIST [22]. The Nb meanderlines, which constitute the four arms of the bridge, cover approximately 8 mm^2 area.

VII. Summary

The standard process developed at NIST provides the facility users with a flexible and robust means for fabrication of a wide variety of superconducting integrated circuits. High quality oxides, with thickness ranging from 0.2 μm to 1 μm, are deposited by ECR-based PECVD. Endpoint detection is used in all the Nb etch processes to ensure minimal and reproducible process runout. Process variability is monitored using a standard mask set and statistical process control methods have been employed for oxide deposition.

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