A Hardware-Efficient, Multirate, Digital Channelized Receiver Architecture

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An approach is presented to realizing a digital channelized receiver for signal intercept applications that provides a hardware efficient implementation of a uniform filter bank in which the number of filters K is greater than the decimation factor M. The proposed architecture allows simple channel arbitration logic to be used and provides reliable instantaneous frequency measurements, even in adjacent channel crossover regions. In the proposed implementation of the filter bank, K is related to M by $K = FM$ where F is an integer. It is shown that the optimum selection of F allows the instantaneous frequency measurement to be made in the channel crossover region and the arbitration function to be based solely on the instantaneous frequency measurement. The development of a filter bank structure which combines the flexibility of the short-time Fourier transform (STFT) with the implementation efficiency of the polyphase filter bank decomposition, meeting these requirements and leading to a hardware-efficient implementation, is presented.

Manuscript received September 25, 1995; revised August 5, 1996 and February 4, 1997.

IEEE Log No. T-AES/34/1/00184.

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I. INTRODUCTION

In RF signal intercept applications, several highly desirable characteristics of the intercept receiver include broadband instantaneous frequency coverage, good sensitivity and dynamic range, simultaneous signal detection, arbitration and parameter encoding, and fine frequency measurement. The receiver architecture which covers most of these characteristics is the channelized receiver architecture [1, 2]. This receiver follows an antenna and an RF front end which, respectively, intercept RF energy and perform signal conditioning and down conversion to a convenient IF. The analog form of the channelized receiver partitions the instantaneous bandwidth (IBW) into a number of uniform channels using a bank of adjacent analog filters. The output of each filter is then amplitude demodulated using logarithmic video amplifiers. After threshold detection, the amplitude demodulated signals are arbitrated (to decide in which channel the signal truly resides) and the parameters of the arbitrated channel(s) are then estimated and encoded. These parameters are, nominally, the signal center frequency, pulse amplitude, pulsewidth, and time-of-arrival.

The channelized receiver has two limitations. The first limitation is caused by the structure of the filter bank and the pulsed nature of the input signals. In order to have continuous coverage across the IBW, adjacent channel responses are overlapped to a large degree. In this respect, the channelized receiver acts like a spectrum analyzer. Thus, there is a great deal of crosstalk between the channels, even when the input is a CW signal. This situation is exacerbated when a pulsed signal is input because the leading and trailing edges of the pulse contain a great deal of broadband energy which spills into adjacent and nonadjacent channels. The result is known as the "rabbit-ear effect" because the out-of-channel, time-domain output responses have a peak on the leading and trailing edges of the pulse due to the impulse response of the filters. Due to these combined effects, some method must be used to "arbitrate" between the filter channels and determine in which channel the input signal truly resides. The remaining responses would then be classified as out-of-channel responses and be discarded. The frequency resolution capability, or the ability to resolve and process two signals closely spaced in frequency, is limited by the aforementioned input signal, the channel filter characteristics and the arbitration capability of the receiver. Currently, techniques such as amplitude comparison of adjacent channels and techniques that detect the presence of the rabbit-ear effect have been used to perform channel arbitration. Both of these approaches use only the amplitudes of filter bank outputs and have inherent limitations [2].

The second limitation of the channelized receiver is that its frequency accuracy is limited to $\pm 1/2$ the filter channel width. For analog systems, this limitation can be mitigated by placing analog instantaneous frequency measurement (IFM) receivers at the output of each channel [2, 3]. This analog IFM approach can provide reliable fine frequency measurement capability only after the channel has been successfully detected and arbitrated. In a previous paper [4], the authors introduced the concept of a "digital channelized instantaneous frequency measurement receiver" along with a technique for estimating the frequencies of simultaneous signals in the same channel. That paper used a generic short-time Fourier transform (STFT) approach to generate the filter bank and briefly mentioned that simple arbitration logic (based on instantaneous frequency measurements) could be developed, however no details were presented. This work builds on that introductory work by showing how a reliable and accurate IFM in the channel crossover regions and arbitration logic based solely on IFMs can be made possible by an optimum relation between the number of filters K and the data decimation factor M. This work also shows the development of a uniform filter bank structure that combines the flexibility of the STFT with the implementation efficiency of the polyphase filter bank decomposition. This leads to a hardware-efficient implementation of the digital channelizer in which the number of filters is related to the decimation factor by $K = FM$. The development and implementation of the proposed filter bank is compared with a similar approach [5] and is shown to have several implementation advantages for the digital receiver application.

Section II provides a generic overview of the receiver architecture including the filter bank, modulation process, and M-fold decimator. Section III details the operation of the IFM at the output of each channel of the filter bank and the optimum selection of F for frequency measurement and arbitration. Section IV shows the development of the proposed filter bank structure as a polyphase decomposition for the general case of $K = FM$ and its comparison with the Rabiner and Crochiere structure [5]. Details of this comparison are shown in Appendix I. Implementation of the filter bank, the IFM, and the arbitration logic is discussed in Section V. Finally, Section VI provides simulations and performance results for the filter bank and arbitration logic while the last section provides concluding remarks.

II. FILTER BANK, MODULATOR, AND DECIMATOR

A functional block diagram of the digital channelized receiver subsystem is shown in Fig. 1. Here $x[n]$ represents the discrete time output of an analog-to-digital converter which feeds a bank of K

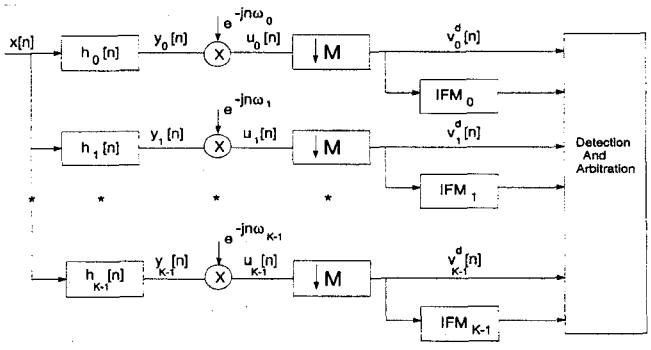

Fig. 1. Digital channelized receiver architecture.

bandpass filters. In the digital receiver application, each of the bandpass filters is derived from a single prototype filter. Let $h_0[n]$ be a causal, symmetric low-pass filter of length N with real coefficients given by

$$h_0[n] = \{h[0] \cdots h[N-1]\}. \tag{1}$$

This low-pass filter can be converted to a set of bandpass filters, where the center frequency of the kth channel is at $\omega_k = 2\pi k/K$, by modulating the prototype coefficients

$$h_k[n] = h_0[n]e^{j\omega_k n} \tag{2}$$

for $k = 0, 1, \ldots K-1$. The frequency response of the kth channel filter is then

$$H_k(e^{j\omega}) = H_0(e^{j[\omega-\omega_k]}). \tag{3}$$

In the digital channelizer application, the prototype filter is designed such that the passband edge frequency ω_p is π/K and the stopband frequency ω_s is $2\pi/K$. The filter is designed in this manner so that adjacent channel responses overlap at the passband edge frequency and the stop-bands of a given channel k occur at the center of channels $k-1$ and $k+1$, respectively. A representation of the magnitude response of the filter bank as a function of the digital frequency ω is shown in Fig. 2. The output of the kth filter, $y_k[n]$ is the convolution sum

$$\begin{aligned} y_k[n] &= \sum_{m=0}^{N-1} h_k[m]x[n-m] \\ &= \sum_{m=0}^{N-1} h_0[m]x[n-m]e^{j2\pi km/K}. \end{aligned} \tag{4}$$

In the previous work [4], the filter bank was implemented with the STFT and it can be shown [6] that (4) can be interpreted as a windowed STFT, as a function of n and k, where

$$h_k[n] = w[-n]e^{j(2\pi kn/K)} \tag{5}$$

and $w[n]$ is the window function. Equivalently, the STFT can be interpreted as the output of a linear

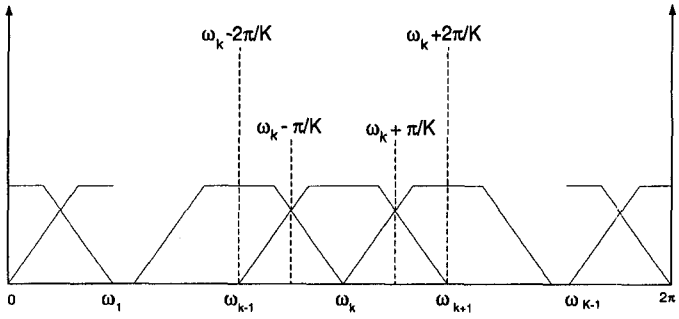

Fig. 2. Filter bank magnitude response.

time-invariant filter bank. In general, for the digital receiver application, $N > K$. If $N = KP$, where P is an integer, then (4) can be written as

$$y_k[n] = \sum_{m=0}^{K-1} \sum_{p=0}^{P-1} h_0[m + pK]x[n - m - pK]e^{j(2\pi km/K)}. \tag{6}$$

To facilitate implementation of the arbitration logic, the spectrum of each bandpass filter output is translated to baseband by the complex exponentials (modulators) as shown in Fig. 1. The baseband signals, $u_k[n]$, are then

$$u_k[n] = y_k[n]e^{-j(2\pi kn/K)}. \tag{7}$$

Ideally, these baseband signals are band-limited to $-2\pi/K \leq \omega \leq 2\pi/K$, and can be decimated by a factor M which gives

$$v_k^d[n] = u_k[Mn] \tag{8}$$

with the associated Fourier transform given by [7]

$$V_k(e^{j\omega}) = \frac{1}{M} \sum_{l=0}^{M-1} U_k(e^{(j(\omega - 2\pi l))/M}). \tag{9}$$

For practical implementations, the stopband attenuation can be controlled, such as the 70 dB shown in Fig. 10, to approximate this ideal case. Hereafter, the d superscript denotes a decimated signal. As can be seen from (9), the decimation of the channel signals serves to attenuate the amplitude by $1/M$ and scale the frequency by a factor of M. After decimation, each channel output is band-limited to $-2\pi M/K \leq \omega' \leq 2\pi M/K$. Here ω' is the digital frequency after decimation. In order to prevent aliasing it can be seen that

$$2\pi M/K \leq \pi. \tag{10}$$

Now, let the input $x[n]$ to the filter bank be a real, pulsed sinusoidal signal $s[n]$ embedded in additive white Gaussian noise $w[n]$. That is, for the time window, $n_0 \leq n \leq N_0 + n_0$ in which the pulse is defined, let

$$x[n] = s[n] + w[n] \tag{11}$$

where

$$s[n] = A\cos(\omega_0 n + \theta) \tag{12}$$

and $w[n] \sim N(0, \sigma_w^2)$. Here A is the peak amplitude, ω_0 is the instantaneous digital frequency, θ is a constant phase shift and σ_w^2 is the noise variance. The input signal-to-noise ratio (SNR) is then

$$\text{SNR}_{\text{in}} = \frac{A^2}{2\sigma_w^2}. \tag{13}$$

Assumming the length of the pulsed sinusoid is greater than the length of the filter, (i.e., $N_0 - N > 0$), the steady state output of the kth filter can be written as [8]

$$y_k[n] = y_{ks}[n] + y_{kw}[n] \tag{14}$$

where $y_{kw}[n]$ is the response due to the noise alone and $y_{ks}[n]$ is the sinusoidal steady state response due to the signal alone

$$y_{ks}[n] = \frac{A}{2}H_k(e^{j\omega_0})e^{j(\omega_0 n + \theta)} + \frac{A}{2}H_k(e^{-j\omega_0})e^{-j(\omega_0 n + \theta)}. \tag{15}$$

The noise response $y_{kw}[n]$ is complex filtered baseband noise, a zero-mean colored Gaussian process with an autocorrelation function $r_{y_{kw}}[l]$, given by [8]

$$r_{y_{kw}}[l] = E\{y_{kw}[n]y_{kw}^*[n - l]\} = \begin{cases} \sigma_w^2 \sum_{m=0}^{N-1-l} h_k[m + l]h_k^*[m] & \text{for } 0 \leq l \leq N-1 \\ \sigma_w^2 \sum_{m=0}^{N-1+l} h_k^*[m - l]h_k[m] & \text{for } -N+1 \leq l < 0 \\ 0 & \text{otherwise} \end{cases}. \tag{16}$$

Given a real input, the output signals are complex, and only half of the filter outputs are unique and needed for further processing (i.e., $0 \leq k < K/2 - 1$ or $K/2 \leq k \leq K - 1$). Taking only one-half of the filter bank outputs and passing them through the modulation process results in

$$u_k[n] = \frac{A}{2}H_k(e^{j\omega_0})e^{j([\omega_0 - \omega_k]n + \theta)} + y_{kw}[n]e^{-j(\omega_k n)} \tag{17}$$

for $k = 0 \cdots (K-1)/2$. The SNR at the output of the modulator is

$$\mathrm{SNR}_{\mathrm{out}} = \frac{A^2}{4\sigma_w^2 \sum_{n=0}^{N-1} |h_k[n]|^2} \approx \frac{A^2 K}{4\sigma_w^2}. \tag{18}$$

Thus, the assumption of an effective noise bandwidth of $2\pi/K$ for each channel filter is valid and the result is a processing gain or noise reduction of approximately $K/2$. After decimation, the filter bank outputs are given by

$$v_k^d[n] = \frac{A}{2} H_k(e^{j\omega_0}) e^{j(\omega_0 - \omega_k)Mn} e^{j\theta} + v_{kw}^d[n] \tag{19}$$

where

$$v_{kw}^d[n] = e^{-j\omega_k Mn} y_{kw}[Mn]. \tag{20}$$

Equation (20) shows the zero-mean colored Gaussian noise sequence $y_{kw}[n]$ is decimated by a factor of M. This is equivalent to decimating the autorcorrelation of the filtered noise by a factor of M. For high SNR, the noise at the output of the filter bank can be converted into an equivalent phase noise [9] and the decimated output can be rewritten as

$$v_k^d[n] = \frac{A}{2} H_k(e^{j\omega_0}) e^{j(\omega_0 - \omega_k)Mn} e^{j\theta} e^{j\eta_k[Mn]}. \tag{21}$$

Here, $\eta_k[Mn]$ is a zero-mean colored Gaussian noise process given by

$$\eta_k[Mn] = \frac{2}{A} \mathrm{Im}\{v_{kw}^d[n] e^{-j(\omega_0 Mn + \theta)}\}. \tag{22}$$

Following (18), the variance is approximated as

$$\sigma_\eta^2 \approx \frac{2\sigma_w^2}{KA^2} = \frac{1}{2\mathrm{SNR}_{\mathrm{out}}}. \tag{23}$$

From the decimated signal in (21), the signal parameters, such as frequency, amplitude and pulsewidth, are then estimated.

III. INSTANTANEOUS FREQUENCY MEASUREMENT, ARBITRATION, AND SELECTION OF F

As noted in the Introduction, the purpose of the IFM in the context of channelized receivers, has been to provide a reliable fine frequency measurement or estimate of the carrier frequency of pulsed sinusoids. In the digital channelized receiver, the IFM still performs this function and can also be used to arbitrate the channels and determine in which channel the signal truly resides. Using (21), the phase of the decimated sinusoid can be written as

$$\begin{aligned} \phi_k^d[n] &= (\omega_0 - \omega_k)Mn + \gamma + \eta_k[n] \\ &= \omega_k^i[Mn] + \gamma + \eta_k[n] \end{aligned} \tag{24}$$

where γ is the sum of the phase introduced by the filter, $\angle\{H(e^{j\omega_0})\}$, and the sinusoid's phase θ. Here, for the kth channel, $\phi_k^d[n]$ represents the instantaneous phase at time index Mn, ω_k^i is the instantaneous digital frequency (hereafter referred to as the instantaneous frequency) of the baseband output, and $\eta_k[n]$ is the phase noise [9, 10]. In the continuous time case, the instantaneous frequency is defined as [11]

$$\omega^i(t) = \frac{d\phi(t)}{dt}. \tag{25}$$

In discrete time, the derivative in (25) can be approximated by the backwards difference operation. Thus, given the instantaneous phase of (24), the IFM or frequency estimate is

$$\hat{\omega}_k^i = \frac{\phi_k^d[n] - \phi_k^d[n-1]}{M} = \frac{\Delta\phi_k^d[n]}{M} \tag{26}$$

where the $\wedge$ denotes the measurement or estimate. There are two issues with respect to the IFM. The first concerns the discontinuities which result when the instantaneous frequency is measured via the phase difference. Because of the periodic nature of the decimated sinusoidal outputs $v_k^d[n]$, the instantaneous phase is defined over the interval $-\pi \le \phi_k^d[n] \le \pi$ and periodic in this interval. This is commonly referred to as phase wrapping. Discontinuities result in the IFM if for a positive phase slope

$$\phi_k^d[n] < \phi_k^d[n-1]. \tag{27}$$

If (27) is true, the phase has crossed the 2π unambiguous boundary. The discontinuities can be removed by unwrapping the phase before the backward phase difference operation is performed.

The second and more important limitation on the instantaneous phase is the implication of the limitation of the unambiguous bandwidth of the IFM and its relation to the bandwidth of the decimated output channels of the filter bank. In order to have an unambiguous frequency measurement

$$-\pi \le \Delta\phi_k^d[n] \le \pi. \tag{28}$$

Thus by (26),

$$-\pi \le \hat{\omega}_k^i M \le \pi. \tag{29}$$

As noted in the Introduction, the determination of the channel in which a pulsed sinusoid resides is called arbitration. Though other methods have been implemented with varying degrees of success, the method presented here combines the characteristics of the filter bank design with the decimation factor to allow a simple arbitration process to be utilized based solely on the IFM. Referring to Fig. 2, a signal can be assigned to channel k based solely on an IFM in channel k if the signal lies in the passband of channel k

$$\omega_k - \omega_p \le \hat{\omega}_0 \le \omega_k + \omega_p \tag{30}$$

where $\omega_p = \pi/K$. An out-of-channel assignment would result for either

$$\hat{\omega}_0 > \omega_k + \omega_p \quad \text{or} \quad \hat{\omega}_0 < \omega_k - \omega_p. \tag{31}$$

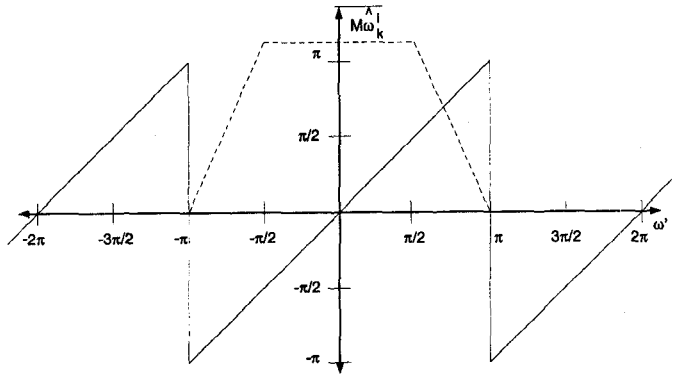

Fig. 3. Instantaneous frequency response for $F = 2$.

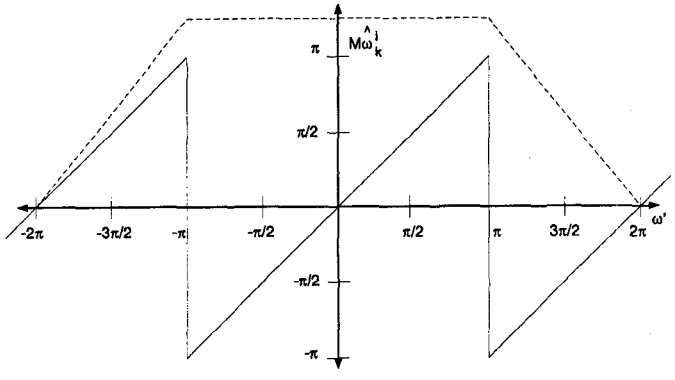

Fig. 4. Instantaneous frequency response for $F = 1$.

Ideally, signal energy would, at most, be generated in the channel in which the input signal truly resides and a single adjacent channel. This can be seen by referring to Fig. 2 and noting that for signals which occur in channel k and above the channel center ω_k, ideal responses are generated in channels k and $k+1$ only. On the other hand, signals which occur below ω_k generate responses only in channels k and $k-1$. In practical situations, the filter stopband gain can be adjusted to approximate this ideal case. For the moment, the broadband energy caused by the leading and trailing edges of pulses, rabbit ears, has been neglected. The removal of these responses is discussed in Section V. Thus, in order to perform channel arbitration as outlined in (30) and (31), the IFM must be unambiguous over the range $\omega_k - 2\pi/K \leq \hat{\omega}_k^i \leq \omega_k + 2\pi/K$. After modulation and decimation by M, this constraint for each channel is

$$-2\pi M/K \leq M\hat{\omega}_k^i \leq 2\pi M/K. \tag{32}$$

Using (29) and (32), the IFM for each channel will be unambiguous if

$$F = K/M \geq 2. \tag{33}$$

Using maximal decimation with respect to (33), (i.e., $F = 2$), the arbitration process based solely on a single sample IFM will assign a signal to channel k if

$$-\pi/2 \leq M\hat{\omega}_k^i < \pi/2. \tag{34}$$

An out-of-channel assignment results for

$$|M\hat{\omega}_k^i| > \pi/2. \tag{35}$$

The mapping of $M\hat{\omega}_k^i$ versus ω' is shown in Fig. 3 for $F = 2$. Note the folding of the IFM response and its relation to the passband and stopband frequencies of the overlayed filter magnitude response.

Maximum decimation of the filter bank channels is attractive from a processing standpoint because the operations can be performed at the lowest computational rate. It can be shown that the maximum decimation relation for general analysis/synthesis applications is $K = M$ or $F = 1$ [5, 7]. However, arbitration, as proposed here, and also reliable frequency measurement at the channel passband edges is not possible for $F = 1$. This is due to the folding of the IFM response at the channel passband edges as opposed to the stopband edges for $F = 2$. The mapping of $M\omega_k^i$ versus ω' is shown in Fig. 4. The frequency measurement beyond the channel passband is ambiguous which makes the arbitration process based solely on the IFM, ambiguous. To use $F = 1$, amplitude comparison must be used in conjunction with IFM arbitration to resolve the ambiguity. The second consideration for $F = 1$ is the validity of the frequency measurement itself. If an input occurs on either of the channel passband edges (adjacent channel crossover points), the IFM will toggle between $-\pi$

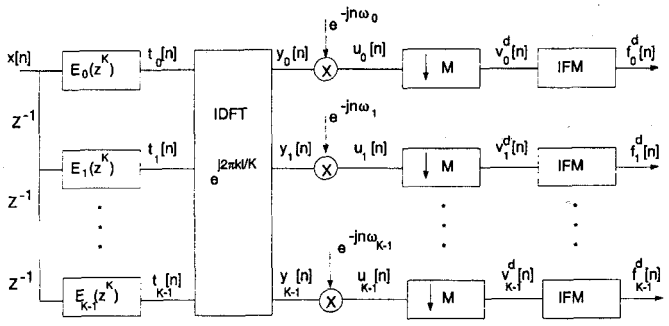

Fig. 5. Polyphase UDFT filter bank.

and π. For signals embedded in noise, this occurs not only at the passband edges but also in a region, near the passband edges, which widens with decreasing SNR. A simple and accurate method of obtaining an estimate of the carrier frequency of a signal is to average the IFMs over a number of samples [4]. For $F = 1$, the estimate will be highly biased for signals in the channel crossover regions. This is not the case for $F = 2$, since the response is continuous to the stopband edge.

IV. PROPOSED FILTER BANK STRUCTURE

This section describes the development of a filter structure as a polyphase decomposition for the general case of $K = FM$. To implement the bank of bandpass filters as the polyphase uniform discrete Fourier transform (UDFT) filter bank shown in Fig. 5, let $h_0[n]$ be the causal prototype filter described by (1). This filter can be decomposed into K polyphase components $E_k(z)$ as [7]

$$H_0(z) = \sum_{l=0}^{K-1} z^{-l} E_l(z^K) \tag{36}$$

where

$$E_l(z^K) = \sum_{n=0}^{P-1} h_0[nK + l] z^{-nK} \tag{37}$$

and $P = [N/K]$, where $[x]$ indicates that the next lowest integer greater than x is the length of the lth polyphase filter. Now let $y_k[n]$ be the output of the kth channel of the inverse discrete Fourier transform (IDFT) matrix at time n. Then, from Fig. 5

$$y_k[n] = \sum_{l=0}^{K-1} t_l[n] e^{j2\pi lk/K} \qquad \text{for} \quad k = 0 \cdots K-1 \tag{38}$$

where $t_l[n]$ is the output of the lth polyphase component. Thus

$$Y_k(z) = \sum_{l=0}^{K-1} e^{j2\pi kl/K} z^{-l} E_l(z^K) X(z) \tag{39}$$

so that the transfer function for the kth channel can be written as

$$H_k(z) = \frac{Y_k(z)}{X(z)} = \sum_{l=0}^{K-1} (e^{-j2\pi k/K} z)^{-l} E_l(z^K). \tag{40}$$

Evaluating (36) at $z = ze^{-j2\pi k/K}$, since $(e^{-j2\pi k/K} z)^K = z^K$, then

$$H_k(z) = H_0(ze^{-j2\pi k/K}). \tag{41}$$

Thus, $y_k[n]$ is the output of a bandpass filter centered at $\omega = 2\pi k/K$. In order to reduce the speed at which the filter, discrete Fourier transform (DFT), and modulator operate, the M-fold decimators can be translated from the output of the modulators to the input of the polyphase filters as shown in Fig. 6. Let $v_k^d[n]$ be the decimated output of the kth channel so that $v_k^d[n] = u_k[Mn]$. Then

$$v_k^d[n] = y_k[Mn] e^{-j\omega_k Mn} = \sum_{l=0}^{K-1} t_l[Mn] e^{-j2\pi kl/K} e^{-j\omega_k Mn}. \tag{42}$$

Since the first exponential term in (42) is independent of M, the M-fold decimators can be moved to the inputs of the IDFT to allow calculation of the IDFT and modulators at the decimated rate. Decimating the output of the lth polyphase filter gives the sequence $s_l^d[n] = t_l[Mn]$ so that

$$\begin{aligned} S_l(z) &= \frac{1}{M} \sum_{m=0}^{M-1} T_l(z^{1/M} e^{-j2\pi m/M}) \\ &= \frac{1}{M} \sum_{m=0}^{M-1} E_l(z^{K/M} e^{-j2\pi Km/M}) \\ &\quad \times X(z^{1/M} e^{-j2\pi m/M})(z^{1/M} e^{-j2\pi m/M})^{-l}. \end{aligned} \tag{43}$$

Since $F = K/M$ is an integer and $e^{-j2\pi Km/M} = 1$ for all integers m

$$S_l(z) = E_l(z^F) \frac{1}{M} \sum_{m=0}^{M-1} X(z^{1/M} e^{-j2\pi m/M})(z^{1/M} e^{-j2\pi m/M})^{-l}. \tag{44}$$

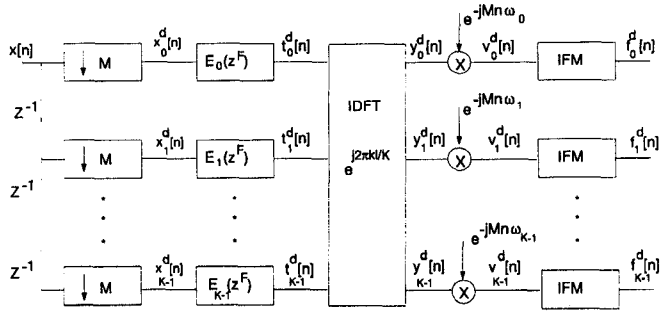

Fig. 6. Polyphase UDFT filter bank with translater decimators.

This is equivalent to replacing the filter $E_l(z^K)$ with $E_l(z^F)$ and moving the M-fold decimator to the front of the filter bank as shown in Fig. 6. Note that the zero-padding factor is now $F-1$ instead of $K-1$. All operations in the filter bank are now accomplished at $1/M$th the rate of the input data. In terms of the time domain

$$e_l[n] = \begin{cases} h_0\left[\dfrac{Kn}{F} + l\right] & \text{for} \quad n = pF \text{ for integer } p \\ 0 & \text{otherwise} \end{cases}. \tag{45}$$

As in Section II, for $N = KP$, this equation allows the decimated output of each polyphase component to be written as

$$t_l^d[n] = \sum_{p=0}^{P-1} h_0[l + pK]x[Mn - l - pK]. \tag{46}$$

The IDFT output is then

$$y_k[n] = \sum_{l=0}^{K-1}\sum_{p=0}^{P-1} h_0[l + pK]x[Mn - l - pK]e^{j2\pi kl/K}. \tag{47}$$

This expression is equivalent to (6) for the decimated case where $n = Mn$. Thus, (47) is equivalent to performing the STFT with an overlap of $N - M$ data points.

In summary, the proposed filter bank structure for implementing a polyphase filter bank for $K = FM$ consists of zero-padding each polyphase component filter with $F-1$ zeros and decimating by M the input across all K channels prior to taking the IDFT. As shown in the Appendix, this architecture for performing channelization via a nonmaximally decimated polyphase filter bank is mathematically related to a similar method used by Rabiner and Crochiere [5]. However, our particular architecture requires only N unique filter coefficients to produce the equivalent STFT. On the other hand, the architecture derived by Rabiner and Crochiere requires the installation of K, F-fold expanders following decimators and uses F subsets of M unique filters, each of length N/M, for a total of FN filter coefficients to produce the equivalent STFT.

V. IMPLEMENTATION OF THE FILTER BANK, IFM, AND ARBITRATION LOGIC

A. Filter Bank

As shown in Section III, the selection of $F = 2$ provides a simple channel arbitration process to be used in the digital receiver which is based solely on the IFM of each channel. In the proposed filter bank structure of the previous section, this implies an overlapping of the data to the polyphase channels by a factor of two. Using (45), we can define the data outputs for the decimators as shown in Fig. 6 as

$$x_l[n] = x[Mn - l] \qquad \text{for} \quad l = 0 \ldots K-1. \tag{48}$$

Close examination of this equation reveals that for $F = 2$, the data distribution to the polyphase filters can be split into two subsets given by

$$\begin{aligned} x_{l_1}[n] &= x[Mn - l_1] \qquad \text{for} \quad l_1 = 0, 1, \ldots K/2 - 1 \\ x_{l_2}[n] &= x_{l_1}[n-1] \qquad \text{for} \quad l_2 = l_1 + K/2. \end{aligned} \tag{49}$$

Thus, the decimated data entering polyphase filters $E_{K/2}(z^F)$ through $E_{K-1}(z^F)$ is a one-sample delayed version of the data entering the filters $E_0(z^F)$ through $E_{K/2-1}(z^F)$. From (42), the exponential term, $e^{-j2\pi kMn/K}$, which provides the modulation of each channel to baseband reduces, for $F = 2$, to

$$e^{-j\pi kn} = \begin{cases} 1 & \text{for} \quad k \text{ even} \\ (-1)^n & \text{for} \quad k \text{ odd} \end{cases}. \tag{50}$$

Utilizing the commutator model concept [5, 7], with (48) and (49), Fig. 6 can be redrawn as shown in Fig. 7. In this model of the proposed filter bank, input data is commutated in a counterclockwise fashion only to the upper $K/2$ polyphase filter channels. The lower $K/2$ channels receive a delayed set of the upper $K/2$ channel inputs. The commutator of Fig. 7 can be implemented using a $1 : K/2$ demultiplexer; the unit delays by storage registers. The polyphase filters, defined by (45), can each be implemented in direct transpose form. Since alternating coefficients are zeros, the associated multiplications and additions can be eliminated. Thus, even though the original prototype filter $h_0[n]$ of length N is effectively

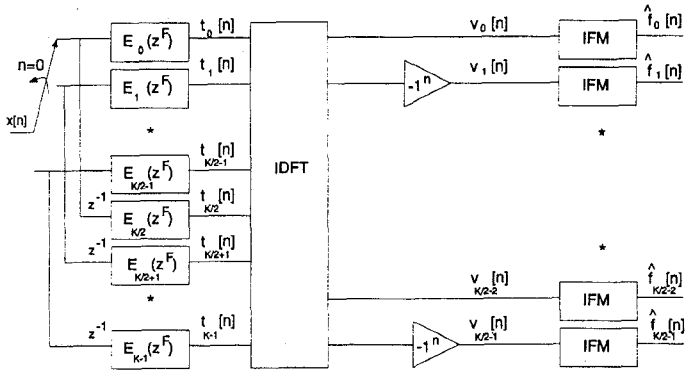

Fig. 7. Polyphase UDFT filter bank commutator diagram ($F = 2$).

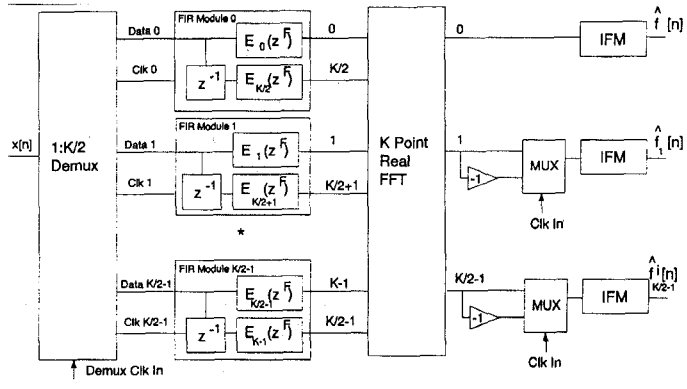

Fig. 8. Polyphase UDFT filter bank hardware block diagram ($F = 2$).

zero padded to length $2N$, the number of required multiplications and additions is N and $N-1$, respectively. The IDFT can be implemented using a real K-point fast Fourier transform (FFT) engine for efficiency. Fig. 8 shows a digital hardware implementation of the filter bank. In Fig. 8, the polyphase filters in each finite-duration impulse response (FIR) filter module are grouped such that the delay elements are included in the filter module, thus reducing input connections to the module. It is envisioned that using 0.25 μm complementary metal-oxide-semiconductor (CMOS) technology, all $K/2$ FIR modules will be able to be implemented on one Application Specific Integrated Circuit (ASIC) chip by 1998.

The proposed filter bank structure for $F = 2$ has the following digital hardware advantages compared with the Rabiner and Crochiere approach.

1) Only $K/2$ unique demultiplexer data outputs are required as opposed to K. This is very important since the number of demultiplexer outputs, and hence FIR inputs, can become large even for modest filter bank sizes. Integration of functions on a single IC, may, in the future, be limited not by circuit density but by physical I/O. Reducing the demultiplexer outputs also reduces required circuitry and power dissipation.

2) Each polyphase filter is required to store half as many coefficients. This is because there are K unique filters in which to distribute the prototype filter coefficients as opposed to $K/2$. This leads to a reduction in silicon area required to implement the filters.

The proposed structure does require a post-filter bank multiplication for the odd output channels, but as shown in Fig. 8, this can be implemented as an alternating sign change. Also, the demultiplexer must run at a clock rate which is twice that of the Rabiner and Crochiere approach. This is not as detrimental as it may seem since the demultiplexer is usually implemented in gallium arsenide (GaAs) technology due to the high-speed requirements. In GaAs logic elements, the power dissipation is largely independent of the frequency of operation (as opposed to CMOS where it is proportional to the frequency of operation), therefore, the output rate increase does not adversely affect the power dissipation.

B. IFM and Arbitration Logic

A simplified functional block diagram of the IFM and the detection and arbitration logic for channel k is shown in Fig. 9. The complex outputs $v_k^d[n]$ of the filter bank are converted into an associated magnitude

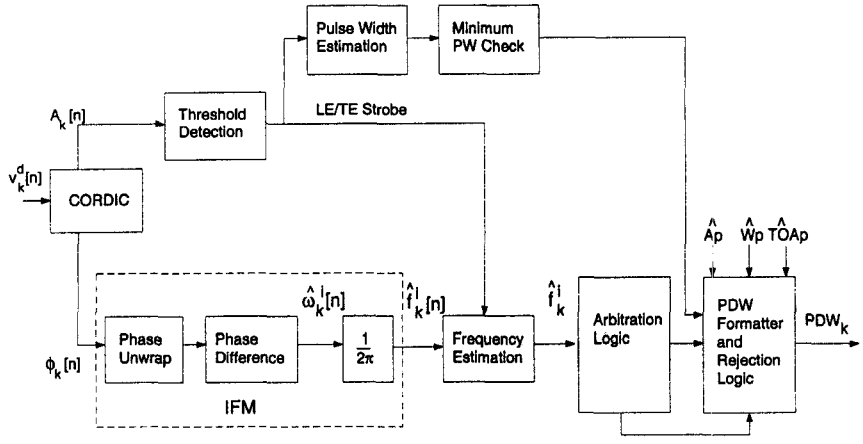

Fig. 9. Channel detection, arbitration and parameter estimation block diagram.

and phase $A_k[n]$ and $\phi_k[n]$ by a Coordinate Rotation Digital Computer (CORDIC) algorithm [12] which functionally solves the following equations

$$A_k[n] = \sqrt{R_k^2[n] + I_k^2[n]} \tag{51}$$

$$\phi_k[n] = \tan^{-1}\left\{\frac{I_k[n]}{R_k[n]}\right\}. \tag{52}$$

The magnitude samples are routed to the signal detection logic and the phase samples to the IFM. The IFM unwraps the phase, implements the backwards difference operation of (26), and scales the output by $1/2\pi$. The output of the IFM $\hat{f}_k^i[n]$ is the IFM on a sample-by-sample basis. Note that we use the term frequency here even though at this point $\hat{f}_k^i[n]$ is a dimensionless quantity. Only after scaling by the channel sample rate does the quantity have the units of Hertz. The outputs of the IFM are averaged to provide a more accurate frequency estimate for an entire input pulse. The detection logic, as shown in Fig. 9, provides pulse leading edge/trailing edge strobes to the frequency estimator logic which defines the number of samples of $\hat{f}_k^i[n]$ that are to be averaged. The pulse frequency estimate is given by

$$\hat{f}_k^{\text{avg}} = \frac{1}{N}\left[\sum_{n=0}^{N-1} 2\hat{f}_k^i[n] + 1/2\right] \tag{53}$$

where N is the number of samples of $\hat{f}_k^i[n]$ between the leading and trailing edge strobes. The pulse frequency estimates $\hat{f}_k^{\text{avg}}$ are then sent to the arbitration logic which determines whether the signal is an in-channel response (valid) or an out-of channel response (invalid).

Equations (34) and (35) describe the arbitration process for a simple IFM. In the implementation of the arbitration process, (53) is used to scale and average the frequency estimates. The arbitration logic based on $\hat{f}_k$ will assign a signal to channel k if

$$0 \le \hat{f}_k^{\text{avg}} \le 1. \tag{54}$$

An out-of-channel assignment results for

$$-0.5 \le \hat{f}_k^{\text{avg}} \le 0 \quad \text{or} \quad 1 \le \hat{f}_k \le 1.5. \tag{55}$$

The arbitration logic is very simple to implement and does not require communication between adjacent channels. The implementation requires two multibit digital comparators, one NAND gate and one OR gate, for each channel, to generate the valid/invalid channel signals.

C. Pulse Descriptor Word (PDW) and Rejection Logic

All pulse parameters (frequency, amplitude, pulsewidth, and time-of-arrival) are fed into the Pulse Descriptor Word (PDW) Formatter and Rejection Logic of the channel. If a channel is valid, as determined by the arbitration logic, the signal parameter estimates are formatted into a PDW, and passed on for further processing. If not, the channel estimates are dropped.

Channels that contain broadband energy that is the result of the leading and trailing edges of the input pulses (i.e., rabbit ears) and that are above the threshold level are automatically rejected from further processing by setting the minimum allowable pulsewidth slightly greater than the impulse response of the filters in the filter bank. If the estimated pulsewidth of a channel is less than the minimum, the PDW Formatter and Rejection Logic drops all pulse estimates.

VI. SIMULATIONS

Simulations of the filter bank structure and the performance of the arbitration logic and frequency estimation were done using MATLAB. The simulation results presented are a part of a larger simulation

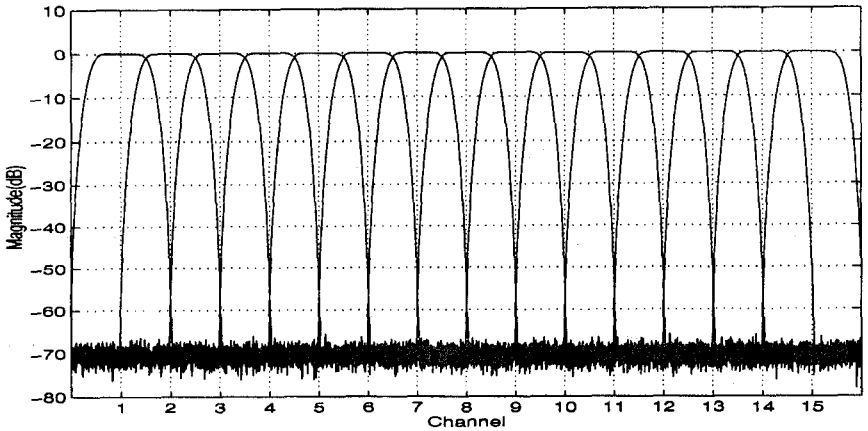

Fig. 10. Filter bank magnitude response.

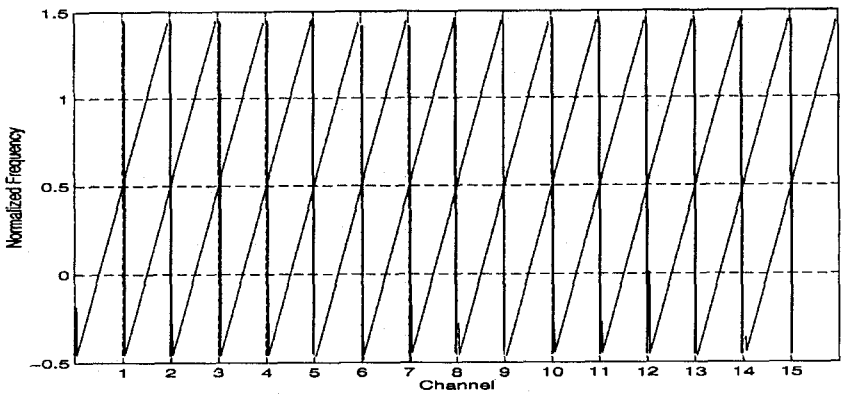

Fig. 11. Phase difference (normalized frequency) response.

program which includes the noise effects of the digital receiver front end, the ADC quantization and jitter noise effects and outputs all of the pulse parameters. For this simulation, the number of channels K was set to 32 and, for $F = 2$, the decimation factor was $M = 16$. All computations were performed using floating point arithmetic with the effective number of bits (ENOBs) of the ADC set to eight. For the purposes of the simulation the threshold level was set to 12 dB SNR.

Fig. 10 shows the realized magnitude response for the filter bank. The number of output channels is $K/2$ or 16; however, the two half channels being used as guard channels in the receiver are not shown. The prototype filter $h_0[n]$ was designed using the Parks–McClellan filter design algorithm and consisted of 256 coefficients which resulted in 8 coefficients per polyphase component. Fig. 11 shows the realized IFM responses, for each channel, using the frequency estimate output from (53). Note that the response is continuous from the center of the channel $k-1$ through channel k to the center of channel $k+1$.

For the purpose of demonstration, an input signal was placed in channel four at a scaled frequency of 0.8. The input signal had a pulsewidth of 3200 samples (100 samples at the filter bank output) and a pulse amplitude of -22 dBfs (decibels below the full scale of the ADC) which results in an SNR of 30 dB at the output of the filter bank. The time domain output of the filter bank (magnitude $A_k[n]$ and IFM $\hat{f}_k[n]$) for channels four and five is shown in Figs. 12 and 13, respectively. As can be seen from the figures, the resultant IFM in channel four is at 0.8 while for channel five it is at -0.2. Thus the arbitration logic would declare channel four as the valid channel and channel five as invalid.

The performance of the frequency estimation and arbitration logic is illustrated by performing a frequency error test and two different dynamic range tests across the entire filter bank bandwidth (all 15 channels). For all of these tests, the pulsewidth was set to 100 samples at the output of the filter bank. The rms frequency error results are shown in Fig. 14. The frequency step size for the input was 1/100th of the channel bandwidth and the SNR was 20 dB at the output of the filter bank. The maximum rms pulse frequency error reported was 0.13% of the channel bandwidth. The pulse frequency estimate was calculated using $N = 40$ samples in (53). In contrast, the typical maximum rms frequency error using $F = 1$ was simulated to be on the order of 30% of the channel bandwidth.

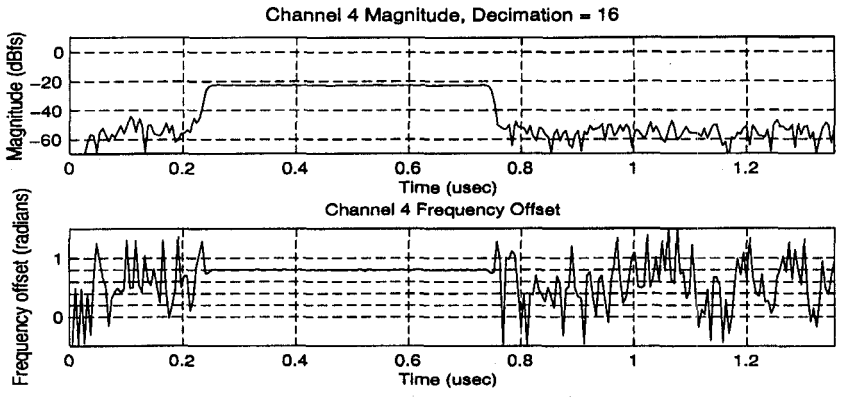

Fig. 12. Magnitude and instantaneous frequency output (channel 4).

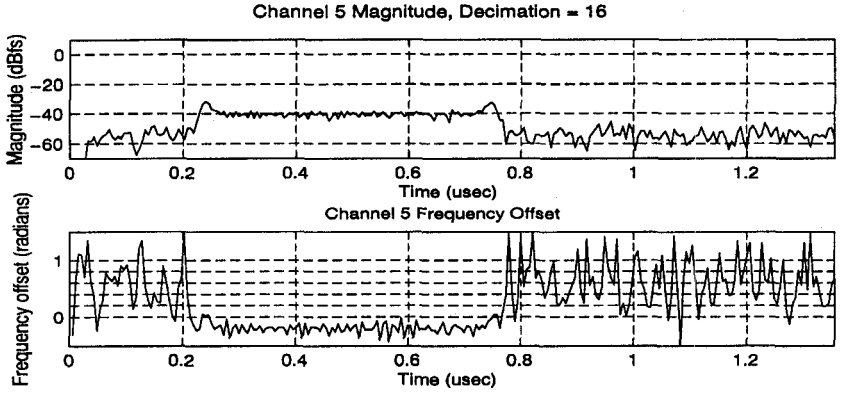

Fig. 13. Magnitude and instantaneous frequency output (channel 5).

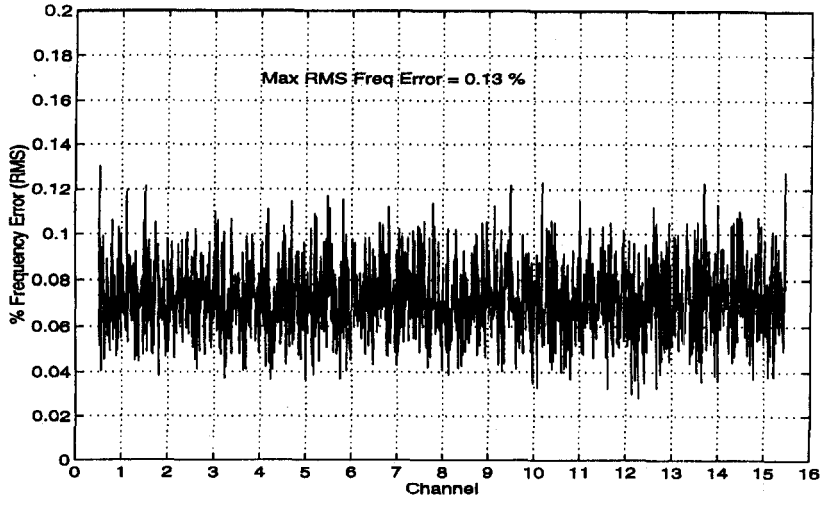

Fig. 14. RMS frequency error.

The Single Signal Dynamic Range (SSDR) is the minimum power range, across the filter bank bandwidth, over which one input signal can be detected and the signal parameters can be encoded to within a given accuracy [2]. In this test, and input signal is set at the noise floor and the signal power is incremented until the signal is correctly detected and encoded. The point in frequency/amplitude space is then marked and the signal is then incremented in power beyond this point until spurious outputs due to saturation effects are reported. This point in frequency/amplitude space is then marked. In between these points, the PDW outputs are checked for spurious error events such as no output PDW, incorrect parameter estimation (in this case frequency measurement) and multiple PDW outputs (which

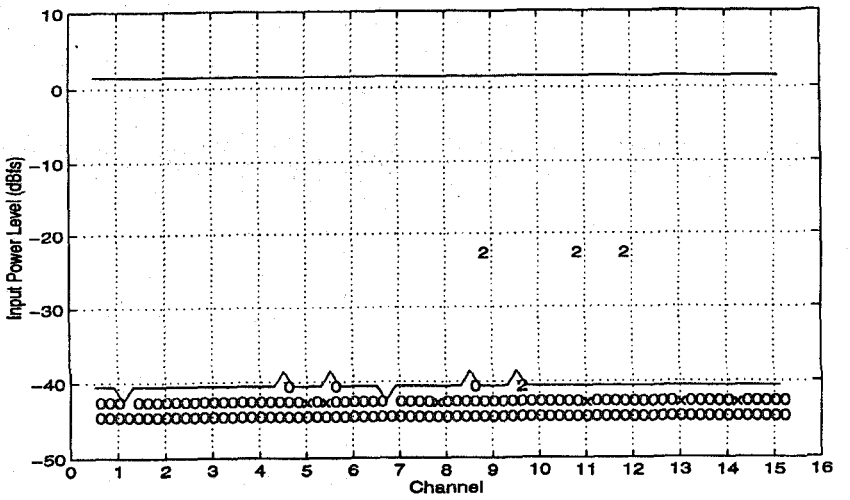

Fig. 15. Single signal dynamic range.

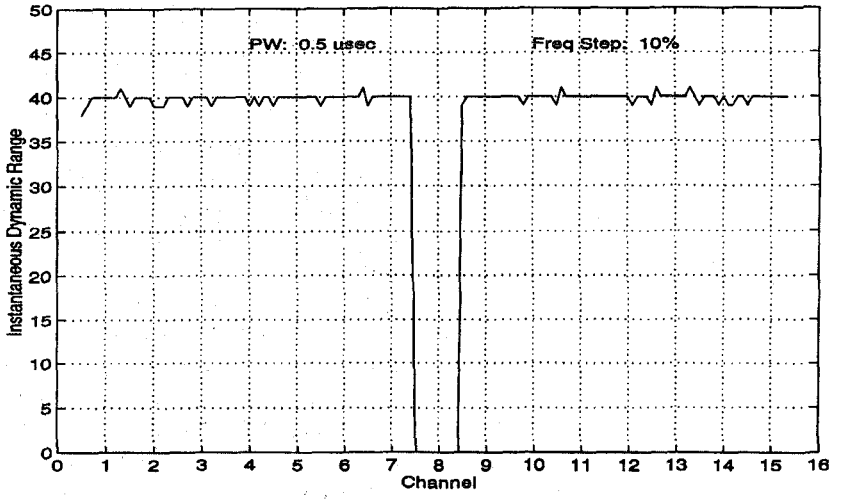

Fig. 16. Instantaneous dynamic range.

would indicate poor arbitration of the channels). A detection of these errors is marked using the following symbols: 0 is no output PDW, X is inaccurate frequency measurement, and 2,3,... is multiple PDWs generated.

After the dynamic range is found at one location, the input frequency is incremented and the process is repeated until the entire bandwidth of the filter bank has been covered. Fig. 15 shows the results of the SSDR test. In this figure, the SSDR is the difference in dB between the upper and lower solid lines. As shown in the figure, only three spurious events were detected across the entire bandwidth and the SSDR is roughly 42 dB. The very low number of spurious error events shows the robustness of the arbitration logic and the frequency measurement.

The instantaneous dynamic range (IDR) is the minimum power range, across the filter bank bandwidth, over which two simultaneous input signals (at different frequencies and different power levels) can be detected and encoded within a given accuracy. This test shows the resolution capability of the receiver arbitration process for signals of different power levels. In this test, one of the input signals is centered at the middle of the band (in this case the center of channel three) at a power level of -1 dBfs. The second signal is set at the noise floor and incremented in power until both signals are correctly detected and encoded. The point in frequency/amplitude space is then marked. The frequency is incremented and the process repeated until the entire filter bank bandwidth is covered. The IDR is the difference, in dB, between the strong signal input power and the marked point. The results of the IDR test, shown in Fig. 16, indicate that the IFM-based arbitration can resolve two signals separated by one-half channel width over a power range of 40 dB.

VII. CONCLUSIONS

This paper has presented a hardware efficient approach and structure for implementing a digital

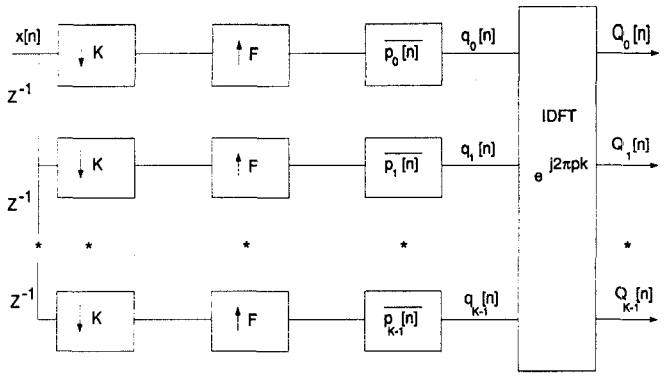

Fig. 17. UDFT filter bank architecture (Rabiner and Crochiere).

channelized receiver for signal intercept applications. It was shown that the proposed filter bank approach leads to implementation advantages in terms of I/O and silicon area reduction. By making an optimum selection of the factor F in the relation $K = FM$, the channel arbitration logic was shown to be very simple and reliable IFMs were made possible in the adjacent channel crossover regions. The simulated performance of the proposed digital receiver in terms of frequency measurement accuracy, arbitration resolution, and spurious errors was shown to be exceptional and, to our knowledge, has never been demonstrated before in a broadband channelized receiver.

APPENDIX

This Appendix shows how the proposed method of implementing the nonmaximally decimated polyphase UDFT filter bank, though architecturally different, is mathematically related to the method proposed by Rabiner and Crochiere when the decimation factor M is related to the number of filters K by $K = FM$ for integer F [5].

1) *Proposed Method*: As shown in Fig. 6, the method proposed for implementing the nonmaximally decimated UDFT filter bank is to zero pad each polyphase component filter with $F-1$ zeros and decimate, by M, the input signal across all K channels prior to taking the IDFT of the filter outputs at time n. Let $h_0[n]$ be a causal low pass filter of length N

$$h_0[n] = \{h[0] \ldots h[N-1]\}. \tag{56}$$

Without any loss of generality, this filter can be decomposed into K polyphase components $E_k(z)$ as [7]

$$H_0(z) = \sum_{k=0}^{K-1} z^{-k} E_k(z^K) \tag{57}$$

where

$$E_k(z^K) = \sum_{n=0}^{\infty} h_0[nK+k] z^{-nK}. \tag{58}$$

In terms of the time domain, the filter coefficients can be written as

$$e_k[n] = \begin{cases} h_0\left[\dfrac{Kn}{F} + k\right] & \text{for} \quad n = pF \text{ for integer } p \\ 0 & \text{otherwise} \end{cases}. \tag{59}$$

Since $e_k[n]$ is non-zero only for integer multiples of F, the output of each polyphase component can be written, without any loss of generality, as

$$t_k[n] = \sum_{i=0}^{\infty} h_0[Ki+k] x[Mn-k-Ki]. \tag{60}$$

At time n, the output of the lth channel is the IDFT of the sequence $t_k[n]$ and can be written as

$$T[l] = y_l[n] = \sum_{k=0}^{K-1} \sum_{i=0}^{\infty} h_0[Ki+k] \, x[Mn-k-Ki] e^{j2\pi kl/K} \tag{61}$$

which is equivalent to calculating the STFT of $x[n]$ over the window $w[n] = h_0[-n]$, overlapped with $N-M$ data points, and evaluating at $\omega = 2\pi l/K$.

2) *Rabiner and Crochiere's Method*: As shown in Fig. 17, in the method proposed by Rabiner and Crochiere, the data is decimated by K, expanded by F, and filtered with K polyphase filters prior to performing the IDFT on these filter outputs [5]. Alternatively, as shown in Fig. 18, this implementation is equivalent to partitioning the polyphase filter coefficients into F separate blocks, indexed by $1 \le l \le F$. Each block is comprised of M separate branches, indexed by $0 \le m \le M-1$, with the mth branch in each block containing the polyphase filter $P_m(z)$ where

$$p_m[n] = h[Mn+m] \quad \text{for} \quad n \ge 0. \tag{62}$$

The kth component of the polyphase representation for $0 \le k \le K-1$ can be evaluated in terms of the block index l and the branch index m as

$$k = M(l-1) + m. \tag{63}$$

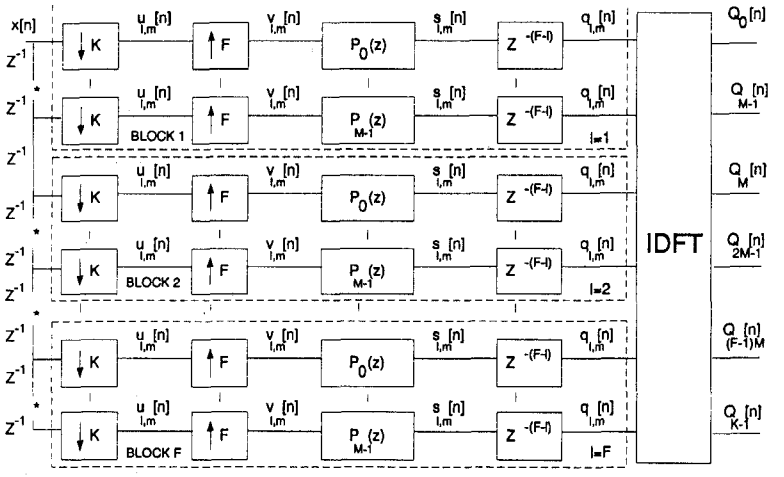

Fig. 18. Equivalent UDFT filter bank architecture.

The data entering the mth branch of the lth block, $x_{l,m}[n]$, is simply the signal $x[n]$ shifted by $M(l-1)+m$

$$x_{l,m}[n] = x[n - M(l-1) - m]. \tag{64}$$

This data is then decimated to produce the sequence

$$u_{l,m}[n] = x_{l,m}[Kn] = x[Kn - M(l-1) - m]. \tag{65}$$

Upon expanding by the factor F, the new sequence becomes

$$v_{l,m}[n] = \begin{cases} u_{l,m}\left[\dfrac{n}{F}\right] & \text{when} \quad n = Fn_l \text{ for integer } n_l \\ 0 & \text{otherwise} \end{cases} \tag{66}$$

Thus, the output of the mth branch of the lth block can be written as

$$s_{l,m}[n] = \sum_{i=0}^{\infty} p_m[i] v_{l,m}[n-i]. \tag{67}$$

Taking into account the $F-1$ zeros between the samples of $v_{l,m}[n]$ gives

$$s_{l,m}[n+f_l] = \sum_{i=0}^{\infty} p_m[Fi+f_l] \; x\left[\frac{Kn}{F} - Ki - M(l-1) - m\right] \tag{68}$$

where $f_l = 0,1,\ldots,F-1$ and $n = Fn_l$ for integer n_l. In terms of the prototype filter, $h_0[n]$

$$s_{l,m}[Fn_l + f_l] = \sum_{i=0}^{\infty} h_0[Ki + Mf_l + m] \; x[Kn_l - Ki - M(l-1) - m]. \tag{69}$$

Since $q_{l,m}[n]$ is just $s_{l,m}[n-F+l]$ we can write

$$q_{l,m}[Fn_l + f_l + F - l] = \sum_{i=0}^{\infty} h_0[Ki + Mf_l + m] \; x[Kn_l - M(l-1) - Ki - m]. \tag{70}$$

At a specific time n_0, the IDFT is performed over the outputs from the polyphase filters. Then, for time synchronization of each delayed filter output, $q_{l,m}[n_0]$, we must have

$$Fn_l + f_l + F - l = n_0 \tag{71}$$

for $l = 1,2,\ldots F$ and $f_l = 0,1,\ldots F-1$. Using the first block, $l=1$, of M filter outputs as the reference

$$Fn_1 + f_1 - 1 = Fn_l + f_l - l. \tag{72}$$

Since $0 \le f_l \le F-1$, then, for time synchronization, $n_l = n_1 + g_l F$ where

$$g_l = \begin{cases} 0 & \text{for} \quad l \le F - f_1 \\ 1 & \text{for} \quad l \ge F + 1 - f_1 \end{cases} \tag{73}$$

so that $f_l = f_1 - 1 + l - g_l F$. Then, the output of the pth channel of the IDFT at time n_0 is

$$Q_p[n_0] = \sum_{l=1}^{F} \sum_{m=0}^{M-1} q_{l,m}[n_0] e^{j(2\pi p/K)[M(l-1)+m]}. \tag{74}$$

Alternatively, in terms of k, the output of the pth channel of the IDFT at time n_0 can be written as

$$Q_p[n_0] = \sum_{k=0}^{K-1} q_k[n_0] e^{j2\pi kp/K}. \tag{75}$$

3) *Methodology Relationships*: In this section, the relationships between the two methods for nonuniform decimation of the channel filters are derived. First, from (60) for $t_k[n]$, let $k = Mf_l + m$ and $n = Fn_l + f_l -$

$l+1$. Then substitution yields

$$t_{Mf_l+m}[Fn_l + f_l - l + 1] = \sum_{i=0}^{\infty} h_0[Ki + Mf_l + m] \, x[M(Fn_l - l + 1 + f_l) - Ki - Mf_l - m]. \tag{76}$$

Thus, referring to (70), shows

$$t_{Mf_l+m}[Fn_l + f_l - l + 1] = q_{l,m}[Fn_l + F - l + f_l]. \tag{77}$$

Making the substitution for $n_0 = Fn_1 + F - 1 + f_1$ and using (73) with $l = 1$ yields

$$q_{l,m}[n_0] = t_{M(f_1 - g_l F)+m}[Fn_1 + f_1]. \tag{78}$$

Using $k = M(l-1) + m$ gives

$$q_k[n_0] = \begin{cases} t_{Mf_1+k}[Fn_1 + f_1] & \text{for } 0 \le k \le M(F - f_1) - 1 \\ t_{k-M(F-f_1)}[Fn_1 + f_1] & \text{for } M(F - f_1) \le k \le K - 1 \end{cases} \tag{79}$$

or equivalently

$$q_k[n_0] = t_{\mathrm{mod}(Mf_1+k)_K}[Fn_1 + f_1]. \tag{80}$$

This shows the outputs of the channels of the K polyphase filters proposed by Rabiner and Crochiere are time related to the outputs of the proposed method. At the output of the IDFT for a fixed sample time n_0, with $Q_p[n_0] = Q[p]$ and $T[p] = y_p[Fn_1 + f_1]$ where

$$Q[p] = \sum_{k=0}^{K-1} q[k] e^{j2\pi kp/K} \tag{81}$$

$$T[p] = \sum_{k=0}^{K-1} t[k] e^{j2\pi kp/K}. \tag{82}$$

Using the MOD_K operation defined by (80) gives

$$Q[p] = e^{-j2\pi pMf_1/K} T[p]. \tag{83}$$

This shows the outputs for the channels of the K filter banks introduced by Rabiner and Crochiere are related, via a time-dependent phase term, to the outputs the channels of the filter banks using the new method.

REFERENCES

[1] Wood, G. (1991)
Advanced channelization technology for rf, microwave and millimeterwave applications.
Proceedings of the IEEE, **7** (Mar. 1991), 1296–1297.

[2] Tsui, J. (1986)
Microwave Receivers with Electronic Warfare Applications.
New York: Wiley, 1986.

[3] Higgins, T. (1994)
Modular channelizer encoder final report.
Report 7, Texas Instruments Inc., Oct. 1994.

[4] Fields, T., et al. (1994)
Digital channelized IFM receiver.
IEEE MTT-S Digest, **3** (May 1994), 1667–1670.

[5] Rabiner, L. R., and Crochiere, R. E. (1983)
Multirate Digital Signal Processing.
Englewood Cliffs, NJ: Prentice-Hall, 1983.

[6] Oppenheim, A. V., and Schafer, R. (1989)
Discrete-Time Signal Processing.
Englewood Cliffs, NJ: Prentice-Hall, 1989.

[7] Vaidyanathan, P. (1993)
Multirate Systems and Filter Banks.
Englewood Cliffs, NJ: Prentice-Hall, 1993.

[8] Therrien, C. W. (1992)
Discrete Random Signals and Statistical Signal Processing.
Englewood Cliffs, NJ: Prentice-Hall, 1992.

[9] Tretter, S. (1985)
Estimating the frequency of a noisy sinusoid by linear regression.
IEEE Transactions on Information Theory, **IT-31** (Nov. 1985), 832–835.

[10] Kay, S. (1989)
A fast and accurate single frequency estimator.
IEEE Transactions on Acoustics, Speech and Signal Processing, **37** (Dec. 1989), 1987–1991.

[11] Boashash, B. (1994)
Estimating and interpreting the instantaneous frequency of a signal, Parts i and ii.
Proceedings of the IEEE, **80** (May 1994), 520–568.

[12] Hu, Y. (1992)
Cordic-based vlsi architecture for digital signal processing.
IEEE Signal Processing Magazine, **3** (June 1992), 16–35.

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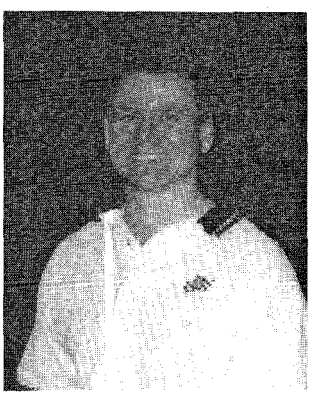

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