Worst-Case Test Vectors for Functional Failure Induced by Total Dose in CMOS Microcircuits with Transmission Gates

A. A. Abou-Auf, IEEE member, D. F. Barbe,* IEEE Fellow, M. M. Rushdi**
U.S. Army Research Laboratory, 2800 Powder Mill Rd, Adelphi, MD 20783

Abstract

Fault models for total-dose induced functional failure in CMOS microcircuits containing transmission gates have been developed for the automatic generation of worst-case test vectors.

I. INTRODUCTION

We have recently developed fault models for functional and leakage-current failures induced in circuits containing static CMOS gates (e.g., INV, NOR and NAND) [1-4]. We used these fault models to automatically generate worst-case test vectors (WCTV) for circuits composed of the above gates as basic building blocks. However, CMOS circuits can be composed from other building blocks in addition to static CMOS gates. One of these is the transmission gate (TG) shown in Figure 1. Static CMOS gates and TGs together makeup the majority of CMOS circuits. Unfortunately, functional failures induced in circuits containing TGs have received little attention in the past. Moreover, we are not aware of previous effort to identify WCTV for CMOS circuits containing TGs. Our focus in this paper is to develop fault models for CMOS circuits containing TGs, then use these models to identify the combinations of irradiation and postirradiation test vectors that can result in a worst-case failure level of the circuit under test. In our analysis, we will use the circuits in the CMOSN Cell Library [5]. This analysis is supported by SPICE simulation that utilizes experimentally extracted transistor parameters. We have also used our analysis to interpret data from a previous total-dose testing a test chip designed using the CMOSN Cell Library and fabricated using 1 μ technology.

II. FAILURE MECHANISM

We analyze the functional failure induced in TG by total dose. The basic CMOS circuit containing a TG is shown in Figure 1, where C_L is the load capacitance, which could be the parasitic capacitance from the input of the following gate. In its normal operation, the TG acts as a switch to charge and discharge C_L according to the voltage values applied at the input and control terminals of the gate, V_i and V_c , respectively. When the control input is at logic 1, the TG is on, and the logic at the input of the TG is passed to the output

of the TG by charging or discharging the C_L through the gate. If the control input is at logic 0, the TG will be off, and the charge in the load capacitance remains stored; thus, the output of the TG will not follow from any transition of logic values at the input of the TG.

Figure 1: Basic circuit containing TG.

When circuits containing TGs are exposed to total-dose radiation, transistor parameters are degraded. If during irradiation the control input is held at logic 1 and the logic value of the input is 0, then there will be a negative shift of the threshold voltage of the parasitic field-oxide transistor or the n-channel MOS transistor (NMOS) or both [6,7]. At failure level, the above irradiation bias will make the TG on all the time, regardless of the logic value applied at its control input during postirradiation. This means that the TG will not be able to hold the charge at its output when there is an attempt to turn it off, i.e., logic 0 is applied at the control input. Therefore, there will be a leakage path between the input and the output, and the gate will fail to act as a switch. Moreover, the leakage current caused by total dose can be large enough to cause logical failure at the output of the gate.

We compared the functional failure levels of CMOS circuits containing TGs to others containing static CMOS circuits by SPICE simulation, where we used experimental transistor parameters of 1.2 μ radiation-tolerant technology. We found that CMOS circuits with TGs exhibits functional failures around 25 Krads. On the other hand, CMOS circuits with static CMOS gates fail functionally around 200 Krads which is about a factor of 8. This means that the worst-case failure levels of CMOS circuits containing both static gates and TGs can be achieved by test vectors manifesting functional failures at the output of TGs.

In the literature of testing VLSI devices from failures produced by manufacturing defects, this kind of failure is modeled as stuck-on fault at the transistor level [7-8]. In the following sections we will develop fault models for TG in

* University of Maryland, College Park, MD.

** George Mason University, Fairfax, VA

combinational as well as sequential circuits so that we can automatically generate WCTV for CMOS circuits containing TGs.

III. COMBINATIONAL CIRCUITS

TGs are used with both combinational and sequential circuits. We first consider faults induced by total dose in combinational circuits. Consider, for example, the circuit of the MUX3 cell of the CMOSN Cell Library shown in Figure 2. The TGs of this multiplexer are organized in pairs such that only one TG can be on at a time.

Figure 2: Gate-level circuit representation of the MUX3 cell.

In order to find the worst-case test vectors of the above circuit we first need to develop a fault model for the pair of TGs shown in Figure 3. A fault model is an abstraction of a failure at a certain level of circuit representation for the purpose of automatically generating test vectors [8]. A test vector is a combination of logic values applied at the primary inputs of the circuit under test that meets two requirements: first, the test vector must excite a fault and, second, it must be able to propagate the fault so that it can be observed at the primary outputs of the circuit under test [8]. We have previously proven that both the irradiation bias vector and the postirradiation vector contribute to the excitation and observation of faults [4].

Figure 3: Pairs of TGs as a basic building block for MUX2.

The control inputs of the gates are set in such a way that the switching states of the gates are mutually exclusive—when one gate is on, the other is off. If the inputs in0 and in1 have

opposite logic values, then the on-gate will charge or discharge the load capacitance with current several orders of magnitude higher than the normal leakage current of off-gate which will discharge or charge the load capacitance; respectively. The result will be that the on-gate will dominate the voltage value of the output capacitance all the time. Therefore, the steady-state logic value at the output node will be the same as that for the input of the TG, regardless of the previous logic value of the output node. This means that these kind of circuits can be used as combinational circuits and the TG can be used as a static switch.

In order to achieve worst-case degradation of the parameters of NMOS transistor, the logic input at the gate terminal of the NMOS transistor during irradiation must be at logic 1 and its source terminal must be at logic 0. Therefore, the worst-case condition of the inputs to this circuit (MUX) during irradiation must satisfy the following Boolean equation:

$$\bar{I}_{sel} \cdot \bar{I}_{in0} + I_{sel} \cdot \bar{I}_{in1} = 1, \quad (1)$$

where I_s are the logic values during irradiation.

Note that if the first term of equation (1) equals logic 1, then TG0 is stuck-on and if the second term is 1, then TG1 is stuck-on.

In order to excite this fault at the output of the MUX, the postirradiation inputs must manifest a logic failure at the output of the MUX. This can be achieved by applying logic 0 at the control input of the stuck-on TG. Therefore, if the irradiation inputs make TG0 stuck-on, then the postirradiation inputs can manifest the faults if they satisfy the following condition:

$$P_{in0} \cdot P_{in1} \cdot \bar{P}_{sel} = 1, \quad (2)$$

and if TG1 is stuck-on instead then, the condition becomes

$$P_{in0} \cdot \bar{P}_{in1} \cdot P_{sel} = 1, \quad (3)$$

where P_s are the postirradiation logic values.

Therefore, the excitation condition that includes both the irradiation and postirradiation inputs can be modeled by the Boolean equation

$$E_{TG} = \bar{I}_{in0} \cdot \bar{I}_{sel} \cdot \bar{P}_{in0} \cdot P_{in1} \cdot \bar{P}_{sel} + \bar{I}_{in1} \cdot I_{sel} \cdot P_{in0} \cdot \bar{P}_{in1} \cdot P_{sel}. \quad (4)$$

The excitation condition means that the fault will be manifested at the output of the MUX if and only if the logic values of the irradiation and postirradiation inputs of the MUX result in $E_{TG} = 1$. From equation (1), we can conclude that of the eight different combinations of logic values applied at the MUX inputs during irradiation, only two can cause one TG to be stuck-on. And from equation (4), there is only one of the eight different combinations of logic values applied at postirradiation can manifest the stuck-on fault of that TG.

Applying the above model for the MUX3 circuit shown in Figure 3, we can now automatically identify worst-case test using exhaustive search for all possible combinations of logic values applied at the primary inputs of the MUX3 circuit. The first part of Table 1 shows the irradiation test vectors that induce stuck-on fault in TG0s of the three MUXs shown in Figure 3. The second part of the table shows the corresponding postirradiation test vectors that can manifest any of the above faults at the primary output of MUX3. Note that any single combination of an irradiation test vector and

postirradiation test vector from Table 1 will sufficiently test the MUX3 at its minimum total-dose failure level.

Table 1. WCTV for MUX3

Test Vector	IN4	IN3	IN2	IN1	SEL2	SEL1
Irradiation	1	1	1	1	1	1
	1	1	0	1	1	1
	0	1	1	1	1	1
	0	1	0	1	1	1
Post-irradiation	1	1	0	1	1	0
	1	0	0	1	1	0
	0	1	0	1	1	0
	1	0	1	1	0	1
	0	0	1	1	0	1
	0	0	0	1	0	1
	0	1	1	1	0	0
	0	1	1	0	0	0
	0	1	0	1	0	0
	0	1	0	0	0	0
	0	0	1	1	0	0
	0	0	0	1	0	0
	0	0	0	0	0	0

IV. SEQUENTIAL CIRCUITS

In this section, we develop a gate-level fault model for TGs used in sequential circuits like the CLAT cell shown in Figure 4. In such circuits, the output of the TG is used as a temporary storage device that holds the voltage of the output node capacitance while the TG is off. However, this storage can only last for a short time since TG is not a perfect switch and there is a very small leakage current while the gate is off. Therefore, TGs are used for storage when the output node can be refreshed periodically or when the storage is needed for an amount of time that is relatively much less than the time it takes to lose the voltage at the circuit's output node through normal off-state leakage current.

Consider, for example, the CLAT is a clocked latch with RESET input. The latch holds its output value Q when the CLOCK input is at logic 1, and Q assumes the value of DATA input when CLOCK is at logic 0. If RESET is at logic 0 then Q is 0. The functionality of the latch can be described by the following logic equation:

$$Q^n = (DATA \cdot \overline{CLOCK} + Q^{n-1} \cdot CLOCK) \cdot \overline{RESET}, \quad (5)$$

where Q^n is the current output of the latch and Q^{n-1} is the previous output.

Figure 4: Gate-level circuit representation of CLAT cell.

We need to develop the excitation condition of TG in sequential circuits, taking into account the effect of the previous output of the TG. For the TG shown in Figure 1, the gate will be stuck-on if the inputs during irradiation satisfies

$$\bar{I}_i \cdot I_c = 1. \quad (6)$$

The postirradiation inputs will manifest the stuck-on failure as a logic failure if there is an attempt to turn off the TG and at the same time the logic at its input terminal has to be the complement of the previous logic value output terminal of the gate. This condition can be modeled as

$$\bar{P}_c \cdot (P_i \cdot \bar{P}_o^{n-1} + \bar{P}_i \cdot P_o^{n-1}) = 1. \quad (7)$$

Therefore, the excitation condition for both the irradiation and postirradiation input is

$$E_{TG} = \bar{I}_i \cdot I_c \cdot \bar{P}_c \cdot (P_i \cdot \bar{P}_o^{n-1} + \bar{P}_i \cdot P_o^{n-1}). \quad (8)$$

In the case of sequential circuits, test vectors will be a sequence of inputs applied at the primary inputs and satisfy equation (8) and at the same time propagate the failure to the primary outputs of the circuit under test.

Consider, for example, the CLAT circuit. The first part of Table 2 shows the irradiation input that makes TG0 stuck-on and the second part of the table shows the sequence of inputs that can manifest logical faults induced at the output of TG0 and manifested at Q and $QBAR$. Note that we used the D-notation in Table 2 [3], where D represents logic 1 at the fault-free circuit and logic 0 in the faulty circuit and $\bar{D}$ is the complement of D.

Table 2. WCTV for CLAT cell.

Test Vector	No.	DATA	CLOCK	RESET	Q
Irradiation input		0	0	0	0
		0	0	1	0
Post-Irradiation input sequence	$n-1$	0	0	1	0
	n	1	1	1	$\bar{D}$
	$n-1$	1	0	1	1
	n	0	1	1	D
	$n-1$	1	1	1	1
	n	0	1	1	D
	$n-1$	0	0	1	0
	n	1	1	1	$\bar{D}$

V. HIERARCHICAL FAULT MODELING

In all of our previous work about the automatic generation of WCTV [1–3], we developed various gate-level fault models. This approach significantly improves the search speed for WCTV. That is because, there will be less information needed to represent the circuit of the device under test (DUT). However, according to the previous definition of fault modeling, we can develop fault models for total-dose induced failures using higher levels of circuit presentation, which will result in further enhancement of the search speed.

Consider, for example, the CLAT cell shown in Figure 4. We can present CLAT as a black box that encapsulates the gate components of CLAT as shown Figure 5. The logic function of CLAT will be as described in equation (5).

Figure 5: Cell-level presentation of CLAT cell.

Equation (8) models the excitation condition of the stuck-on fault of any of the TGs of CLAT. A stuck-on fault in TG0 makes CLAT no longer a storage device. TG1 refreshes the charge at the output of TG0 when it is off. If TG0 is stuck-on then a stuck-on fault in TG1 does not disturb the functionality of CLAT. Therefore, the excitation condition for CLAT will be similar to that of TG0, except that we also need to take into account the propagation of the fault from the output of TG0 to the output of CLAT. This can be done by maintaining the RESET input during postirradiation at logic 1. Consequently, the excitation condition of CLAT can be described by

$$E_{CLAT} = \bar{I}_{DATA} \cdot \bar{I}_{CLOCK} \cdot P_{CLOCK} \cdot (P_{DATA} \cdot \bar{P}_Q^{n-1} + \bar{P}_{DATA} \cdot P_Q^{n-1}) \cdot P_{RESET} \quad (9)$$

Equation (9) gives the same set of worst-case test vectors as those shown in Table 2.

Conceptually, we can further enhance the search a speed for WCTV by developing fault models for higher circuit presentation. For example if we have a buffer consisting of four CLATs as shown in Figure 6 and this buffer is used several times within a particular circuits, we can develop a fault model for that buffer at a level that encapsulates the 4 CLATs. The excitation condition for such a buffer is shown in equation (10).

$$E_{BUFFER} = P_{RESET} \cdot \bar{I}_{CLOCK} \cdot P_{CLOCK} \cdot \sum_{i=0}^3 \bar{I}_{Xi} (P_{Xi} \cdot \bar{P}_{Zi}^{n-1} + \bar{P}_{Xi} \cdot P_{Zi}^{n-1}) \quad (10)$$

Figure 6: Cell-level presentation of a 4-bit buffer

VI. EXPERIMENTAL RESULTS

The work in this paper was initiated as a follow-on investigation of the results of total-dose testing done at the US Army Research Laboratory on a test chip. The test chip was designed using all cells from the CMOSN Cell Library and it was fabricated using 1 μ radiation-tolerant technology. The experiment was done using Co 60 at room temperature. Both all zeros and all ones inputs were used as irradiation biases. The dose rate were set to 100 Rad/s. The total-dose testing of individual MOS transistors of the test chip suggested that the primary reason for failure of the chip would be the leakage current due to degradation in the field oxide. Also, 30,000 carefully selected test vectors were applied to test the functionality of every cell in the test chip. However, the functional failure levels of all the applied test vectors were almost exactly the same. This suggests that either all cells in the CMOSN Cell Library have the same hardness level or that the input/output circuitry has the lowest hardness level. The first reason contradicts what was reported earlier about the effect of the circuit design on the functional failure induced by total dose [1–4], [11, 12]. We closely examined the design of the input/output circuitry of the test chip and found that all inputs and outputs in the test chip were buffered by the DFF cell of the CMOSN Cell Library as shown in Figure 7.

The gate-level presentation of DFF is shown in Figure 8. The DFF cell contains three TGs and based on the schematic of the cell, any logic applied at the clock input during irradiation will cause at least one of the TGs to fail. As mentioned previously, TGs cause the device under test to fail at levels much lower than those caused by cells with static gates. Consequently, the 30,000 test vectors were not actually testing the functionality of the cells inside the ASIC test chip, but were causing the input/output circuitry to fail and mask the other failures that took place inside the chip at higher dose levels.

The above experiment shows that if the DUT has transmission gates, then worst-case failure level is achieved by selecting test vectors to target the transmission gates within the DUT.

Figure 7: Block diagram of the test chip.

Figure 8: Gate-level representation of the DFF cell.

VII. CONCLUSION

Identifying worst-case test vectors for total testing of complex VLSI devices is an essential task for the hardness assurance of such devices when used in a radiation environment. Unfortunately, very little effort has been exerted in this area. This paper is a continuation of our previous effort in developing gate-level fault models and automatically generating worst-case test vectors for CMOS microcircuits. We analyzed and modeled the functional failure induced by total dose in CMOS microcircuits with TGs. We showed that total dose will induce stuck-on faults in TGs. We also showed that the failure levels of microcircuits containing TGs as components are much lower than those containing static CMOS gates. We developed fault models for TGs that were used in combinational as well as sequential circuits. We used those models for the automatic generation of worst-case test vectors for microcircuits from the CMOSN Cell Library, a cell library used in conjunction with ASIC design fabricated through MOSIS foundry. We introduce a new hierarchical methodology for identifying WCTV which can significantly enhance the search speed for WCTV a very important step for automatically identifying WCTV for complex VLSI devices. We used the above analysis to interpret the total-dose testing result of a test chip designed using CMOSN Cell Library. We concluded that there should be more research needs to be done for the design of test chips used as vehicles in the assessment of the failure levels of CMOS macro cells.

Finally, identifying WCTV for complex VLSI devices is still a very challenging task. More research is needed for the failure analysis of other types of CMOS building blocks. Also, more research is needed for the development of fault models and algorithms to enhance the search speed for WCTV.

REFERENCES

- [1] A. A. Abou-Auf, "Stochastic Worst-Case Test Vectors for CMOS Circuits Exposed to Total Dose," GOMAC 1997, pp. 89-92.
- [2] A. A. Abou-Auf, "Gate-Level Modeling of Leakage Current Failure Induced by Total Dose for the Generation of Worst-Case Test Vectors," *IEEE Trans. Nucl. Sci.*, NS-43, No. 6, pp. 3189-3196, 1996.
- [3] A. A. Abou-Auf, D. F. Barbe, and H. A. Eisen, "A Methodology for the Identification of Worst-Case Test Vectors for Logical Faults Induced in CMOS Circuits by Total Dose," *IEEE Trans. Nucl. Sci.*, NS-41, No. 6, pp. 2585-2592, 1994.
- [4] A. A. Abou-Auf, "Failure Analysis and Worst-Case Generation of Test Vectors for CMOS Circuits Exposed to Ionizing Nuclear Radiation," Ph.D. Thesis, Electrical Engineering Department, University of Maryland at College Park, MD, 1993.
- [5] CMOSN Cell Library Notebook, Rev. 3.0 A, MOSIS Services, Marina del Rey, CA, 1992.
- [6] T. R. Oldham, A. J. Lelis, H. E. Boesch, J. M. Benedetto, F. B. McLean, and J. M. McGarrity, "Post-Irradiation Effects in Field-Oxide Isolation Structures," *IEEE Trans. Nucl. Sci.*, Vol. NS-34, No. 6, pp. 384-389, 1987.
- [7] J. M. Terrell, et al, "Time Dependent Annealing of Radiation Induced Leakage Currents in MOS Devices," *IEEE Trans. Nucl. Sci.*, Vol. NS-36, No. 6, pp. 2205-2210, Dec. 1989.
- [8] K. M. Butler, Ph.D. Dissertation, "Techniques for assessing fault model and test quality in automatic test pattern generation for Integrated Circuits," University of Texas at Austin, Austin, TX, 1990.
- [9] E. Vandris and G. Sobelman, "A Mixed Functional/ I_{DDQ} Testing Methodology for CMOS Transistor Faults," pp. 608-614, International Test Conference 1991.
- [10] R. K. Gulati, W. Mao and D. K. Goel, "Detection of Undetectable Faults Using IDDQ Testing," pp. 770-777, ITC 1992.
- [11] J. Wall, "The NASA ASIC Guide: Assuring ASICs for SPACE," Draft version 0.5, April 1993.
- [12] D. R. Alexander, "Design Issues for Radiation Tolerant Microcircuits for Space," Short Course, NSREC 1996.