Evidence for Two Types of Radiation-Induced Trapped Positive Charge

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Abstract

New experimental evidence is presented that supports a model that assumes two distinguishable types of positive oxide charge following x-irradiation. Two new experiments have been performed designed to separate the annealing properties of the two types of trapped positive charge. It is found that one type of trapped positive charge can be permanently removed at room temperature using substrate hot electron injection. The second type of trapped positive charge is found to be stable at temperatures up to 160°C

I. INTRODUCTION

Over the past decade several researchers have studied the effects of switched-bias anneals on radiation-induced trapped positive oxide charge [1-6]. One characteristic often observed is that a fraction of the defects can be repeatedly charged and discharged by alternating the gate bias. The basic mechanism for this reversibility of charge state remains unclear.

Similar results have been observed following other methods of defect generation [7-9]. In one study, it was found that the annealing behavior of positive oxide charge was determined by the method used to damage the devices [7]. In particular, oxides damaged by avalanche electron injection generated defects that could be repeatedly charged and discharged by the appropriate change of gate bias, whereas oxides damaged by avalanche hole injection generated defects that permanently annealed regardless of the gate bias. In other studies by Trombetta et al. [7,9] and Freitag et al. [6] it was found that the annealing behavior of defects generated by Fowler-Nordheim (FN) tunneling was polarity dependent. Most of the defects generated by Fowler-Nordheim tunneling with a positive gate bias could be repeatedly charged and discharged, whereas FN tunneling with a negative gate bias generated mostly defects whose charge state was not reversible. That is, for a given device, the annealing behavior of the trapped oxide charge generated by electrical stressing depends upon the conditions <u>during</u> the stress.

The fact that the manner in which the oxide is damaged determines the post stress behavior of the defects suggested to Trombetta et al. that two types of defects can be generated in gate oxides. Further, Freitag et al. [6] showed that the annealing behavior of radiation-induced defects was similar to that following FN tunneling. They concluded that radiation also generates two types of trapped charge.

As mentioned above, Trombetta et al. [7] proposed a model that assumes two distinct species of trapped positive oxide charge. Following the terminology of Trombetta et al. we will refer to these two defects as "trapped holes" and "anomalous positive charge" (APC). These two defects are distinguished by their behavior following generation. It was suggested [6,7,9] that the trapped hole is a defect located below the silicon bandgap and does not reversibly exchange charge with the silicon substrate. This defect is permanently removed by tunneling into the silicon valence band or by thermal emission to the SiO_2 valence band. This process occurs with any applied oxide field but the annealing rate is field dependent. The second defect, the APC, is a donor state energetically located near the silicon conduction band, and is stable at temperatures up to about 160°C, but does permanently anneal at about 200°C. The APC defects will be either charged positively or neutral depending upon the applied gate bias.

This work extends our previous work by showing the results of new experiments where the two species of trapped positive charge can be separated and studied. A first set of experiments involves bias-anneals that suggest two mechanisms are involved in the annealing process. The second set of experiments show that the trapped holes can be removed, allowing the APC's to be studied independently.

II. EXPERIMENTAL DETAILS

The devices used in this study were polysilicon gate n-channel transistors fabricated by the NRL nanoelectronics facility. The gate oxide thickness was 50 nm. Irradiations were performed at room temperature using ~10 keV x-rays. The dose rate during irradiation was approximately 200 krad/min. For all irradiations a +1.5 MV/cm oxide field was applied.

Following irradiation, two types of measurements were made to separate the properties of the two types of trapped charge. In the first set of measurements, three irradiated devices were annealed with three different bias protocols. After the transistors were annealed at constant applied gate bias for a sufficient time to characterize their annealing behavior, one transistor was subjected to alternating biases for the remainder of its anneal. From the results it will be shown that two processes are occurring simultaneously during the anneals, and that they can be studied independently.

To separate more clearly the behavior of the two defects, Substrate Hot Electron (SHE) injection was used following irradiation. A second set of devices was irradiated to generate trapped charge. Then the devices were subjected to SHE injection to neutralize this trapped positive charge (see [10] for details). During the SHE injection, the gate oxide field was maintained at +1.5 MV/cm, source and drain were grounded, and -10 V was applied to the substrate. The substrate electrons were supplied from a nearby forward biased n^+/p junction on the same wafer. This procedure readily neutralizes almost all of the trapped positive charge in a relatively short time. The main advantage of this technique is that electrons can be injected into the gate with sufficiently small oxide fields so that no additional defects are generated in the oxide. Unirradiated control samples were subjected to this procedure for the same length of time to ensure that this technique did not generate new defects in the oxide. At the completion of the injection procedure, the device was subjected to isochronal bias-anneals and measurements were made as a function of applied oxide field.

The amount of net trapped positive charge in the oxide was determined from the midgap voltage shift by using the subthreshold technique.

III. EXPERIMENTAL RESULTS

The first set of experiments was designed to separate the annealing properties of the APC's from those of the trapped holes. It will be shown that, in these devices, the total number of APC's is constant, but the fraction of charged APC's is field dependent. Figure 1 shows the annealing behavior of three transistors irradiated to a total dose of 750 krad. Following irradiation the devices were annealed at 100°C with three different biases. One transistor was maintained with an applied oxide field of -2 MV/cm for the entire anneal. A second had gate and substrate connected and grounded (applied bias was 0 MV/cm). The third transistor was subjected to a set of different applied oxide fields. For the first 10^3 minutes the applied field was +2 MV/cm. This length of time allowed us to determine the annealing characteristic at this bias. After the first 10^3 minutes the bias conditions were altered to investigate the effect of anneal bias on the APC's. First the applied field was changed to 0 MV/cm (region A) for about 1200 minutes. The applied field was then changed to -2 MV/cm (region B). Following this negative bias anneal, the field was then returned to +2 MV/cm for approximately one month (region C). It can be seen that during the time period marked region A the midgap voltage shift of the transistor initially biased positive is approaching the midgap voltage shift of the transistor that was continually maintained at zero bias. Similarly, during the time period marked B the midgap voltage shift approaches that of

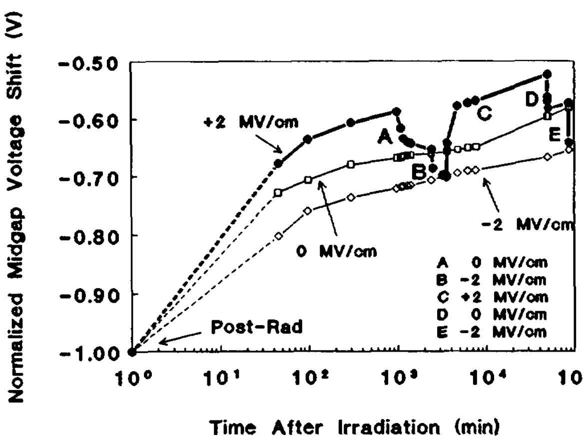

Figure 1. Annealing behavior of three transistors at 100°C following a 750 krad irradiation . Squares show the results of a continuous zero-bias anneal. Diamonds show the results of a continuous negative-bias anneal. Filled circles show the results of alternating-bias anneal (see legend).

the device biased negative throughout. Then, during the period marked region C, the midgap voltage shift returns to a value that appears to be an extension of the earlier positive bias anneal curve (the first 10^3 minutes).

To investigate the reproducibility of the behavior displayed in regions A, B, and C, the field was again changed to 0 MV/cm and maintained for approximately an additional month (region D). Finally, the field was reversed and maintained at -2 MV/cm (region E). Regions D and E show that the earlier switched bias behavior is, in fact, reproducible.

Following the anneal sequence described in the previous paragraphs, the transistor subjected to the alternating bias anneal was then injected with electrons using low field SHE injection to neutralize almost all of the remaining trapped positive charge. Only about 4% of the original charge remained. As will be discussed later, a reasonable interpretation of the status of the oxide at this point is that the trapped holes had been removed, while the APC's were in a charge neutral state, having trapped electrons.

Once the positive charge was neutralized, the device was annealed at 100°C with an applied field of 0 MV/cm for about 2000 minutes. At this time the applied field was switched to -2 MV/cm. The results of this anneal sequence are shown in figure 2. Note that following the injection almost all the trapped charge had been neutralized (the post-rad midgap voltage shift was -2.5 V, while the post-injection midgap voltage shift was -.095 V). During the time that the device was maintained at 0 MV/cm, the midgap voltage shifts to a more negative value suggesting that electrons are tunneling out of the oxide linearly in log-time. As was stated above, following the zero bias anneal the device was maintained with a -2 MV/cm applied field and the midgap voltage shift was measured as a function of time. Note that the time scale for

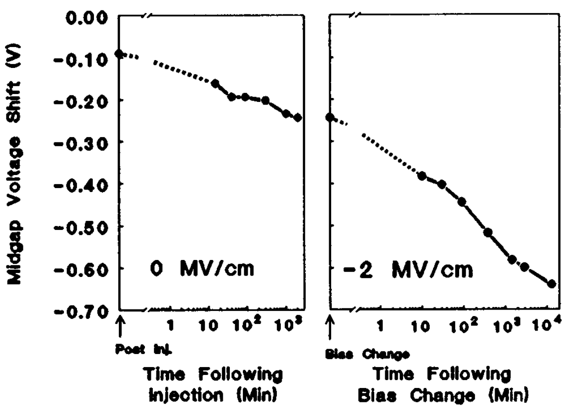

Figure 2. Annealing behavior following SHE injection. Annealing bias: initially 0 MV/cm, then -2 MV/cm.

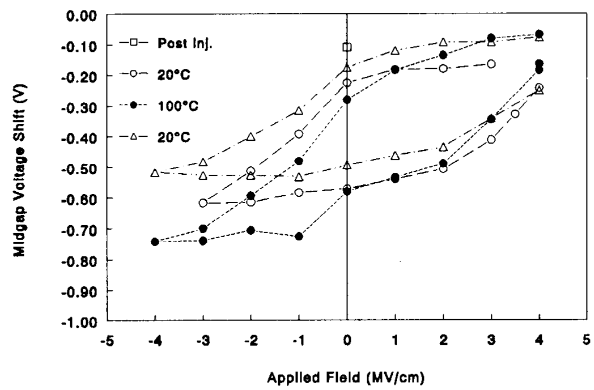

Figure 3. Three isochronal bias-anneals. The transistors were irradiated followed by SHE injection. Each point represents a 24 hour anneal at the applied field shown. See text for procedure used.

the right hand panel of figure 2 is re-started at zero.[1] Again the rate of charge recovery was linear in log-time, but with an increased slope. Clearly much more charge had been retrieved than would have been if the device had been maintained at zero bias for the entire time. It is important to note that the two panels show independent log-linear behaviors.

To further investigate the reversible nature of the APC's, another transistor was irradiated and immediately subjected to SHE injection. The initial midgap voltage shift following the irradiation was -2.5 V. After the injection procedure the midgap voltage shift was only -0.122 V (indicated as "post-inj." point at 0 V in figure 3), which shows that the electron injection successfully neutralized about 95 percent of the initial trapped charge. That the midgap voltage shift did not go positive for any of the devices suggests that very few neutral electron traps are generated during the irradiation in these devices.

After completion of the SHE injection, the transistor was subjected to an isochronal bias-anneal at room temperature. The results of this procedure are shown in figure 3. Upon completing the electron injection the device was maintained at +3 MV/cm for 24 hours. The midgap voltage shift measured at this time is represented by the open circle data point near the upper right corner of figure 3. On each subsequent day the applied field was reduced by 1 MV/cm until the 24 hour anneal at -3 MV/cm in figure 3 was completed. The data up to this time are a set of open circles connected by a dashed line. Each point shows the midgap voltage shift after a 24 hour anneal at the applied field shown. After completing the -3 MV/cm anneal, the bias procedure was reversed and the applied fields were increased by 1 MV/cm until +3 MV/cm was reached. The final two points in this sequence were also 24 hour anneals, but the bias increment was reduced to 0.5 MV/cm. This finished the first cycle at room temperature. This cycle is shown by the open circles connected by dashed lines.

The experiment described above was then continued with a series of bias-anneals at 100°C. First, the temperature was raised to 100°C and the device was allowed to anneal for another 24 hours with an applied field +4 MV/cm. The cycle was restarted and the results of this second cycle are shown by the solid circles connected by a dotted line. At the completion of this elevated temperature cycle, the transistor was left with an applied field of +4 MV/cm for an extra 24 hours to see if all of the charge could be neutralized. After this 48 hour anneal, the SHE injection procedure was repeated. The temperature was then lowered to room temperature and the annealing cycle started for a third time. The results of this third cycle are shown by open triangles connected by dash-dot lines. The results of this last cycle are similar to the first two.

Following the irradiations described above there was also an initial buildup of interface states (as determined by the stretchout of the subthreshold curve). During the bias-anneals, however, only very small changes in the subthreshold slope were found for temperatures below 160°C. No large variations in the subthreshold slope were observed, in contrast to results of similar experiments on different devices that have been seen by others [12,13]. At temperatures higher than about 160°C, the subthreshold slope increased, consistent with some annealing of the interface states. It should be noted that the small changes in the subthreshold slope seen in this work has also been observed in similar experiments on different devices used in ref. 6.

[1] Note also that the dashed line in both panels of Fig. 2 is merely a guide to the eye. The shape of the curve for times smaller than 10 min is unknown. McLean [11] has suggested, on theoretical grounds, that data of this type may show significant curvature at small times.

As shown by figure 1, and by the SHE injection experiment, the trapped holes can be removed permanently at 100°C (or lower). The question remains, at what temperature can the APC's be removed. To investigate this question, the following procedure was used. Upon completion of the last bias-anneal cycle shown in figure 3, the device was maintained with an applied field of -4 MV/cm for two days at 100°C. This is sufficient time to remove most of the electrons compensating the APC's. At this point the temperature was raised incrementally each day by 20°C. No significant change in the midgap voltage was observed up to 160°C. Small changes were observed beginning at 180°C, and all the positive charge was removed at 200°C. This result is similar to that reported by Stahlbush et al. [13].

IV. Discussion

A. Experimental Results

Studies of the effects of electrical stress on MOS devices often show a similar reversible component during post-stress anneals. The fraction of the total charge generated by electrical stressing that can be charged and discharged repeatedly has been shown to depend upon the stressing procedure used [7-9]. To explain this phenomenon, Trombetta proposed a model that assumes two defects that are located at different energy levels in the SiO_2 bandgap. This model is depicted schematically in figure 4. The trapped holes are located below the silicon bandgap, whereas the APC's are located near the silicon conduction band. The trapped holes can be permanently removed by a tunneling process to the substrate or by thermal emission to the SiO_2 valence band. The APC's are located near the silicon conduction band, appear relatively stable at temperatures up to at least 160°C, and can exchange charge with the substrate. Since the APC's are near the conduction band it is expected that the number of defects that are positively charged will depend upon the applied field.

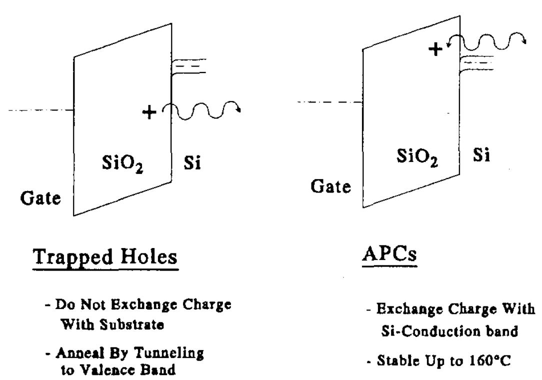

Figure 4. Schematic illustration of the Trombetta model.

The data presented in figure 1 may be interpreted in the context of this model as follows: During the initial 10^3 minutes a significant fraction of the initial trapped charge is removed under any bias condition. For each of the three curves, trapped holes are annealing at similar rates. The difference among the three curves is consistent with differences in the charge state of the APC's. For the top curve (+2 MV/cm) the majority of the APC's are in their neutral state. For the bottom curve (-2 MV/cm) the majority of the APC's are in their positive state. The middle curve (0 MV/cm) is an "in between" case. When the bias of the transistor that was initially positively biased is switched to 0 MV/cm after 10^3 minutes, the midgap voltage shifts to a more negative value (region A). This change suggests that electrons that were compensating the positively charged APC defects are tunneling out of the oxide. It is important to note that the electrons are tunneling out of the oxide into the substrate although the local field across the interface due to the work function difference and the remaining trapped charge is positive. This charge recovery continues until the midgap voltage approaches the midgap voltage of the transistor maintained continuously with a 0 MV/cm applied field. A similar result is obtained when the applied field is switched to -2 MV/cm (region B). The midgap voltage approaches the midgap voltage of the transistor that was negatively biased the entire time. When the bias is returned to +2 MV/cm electrons tunneling back into APC's cause the midgap voltage to shift in the positive direction and eventually return to a value that is an extension of the first part of the curve when the device was positively biased. The last two bias changes reproduce the first two, suggesting a reversible mechanism that is responsible. The number of APC's that are positively charged or neutral appears to depend upon the applied bias.

An important annealing characteristic can be seen in figure 2 showing bias-annealing following SHE injection. During the zero bias anneal, the midgap voltage shifts negatively with a time dependence that is linear in log-time. This linearity is consistent with electrons tunneling out of the oxide from a spatially uniform distribution of defects. Following the switch to -2 MV/cm, log-linear behavior in time is again observed, but with a significantly different slope. It is clearly not an extension of the zero bias anneal. Log-linear behavior suggests that during the negative bias anneal electrons are still tunneling from the silicon, but from a slightly different uniform-spatial-distribution of defects. The change in slope also suggests that during the negative bias anneal the electrons are tunneling from a different distribution of defects.

To explore further the charging and discharging of the APC's, consider the isochronal bias-anneal data of figure 3. Qualitatively, all three cycles are similar. The fact that the magnitude of the total changes of the midgap voltage during the two room temperature cycles (open symbols) are approximately equal suggests that the number and location of the APC's are fairly stable and can be repeatedly charged and discharged. Note that this stability remained even though the two room temperature cycles were separated by a 100°C cycle. Note also that the total time represented by the three cycles shown in figure 1 is more than 45 days. During each 24 hour anneal at a given applied bias the APC's charge or discharge linearly in log-time, similar to the data shown in figure 2. The linearity can be explained by electrons tunneling in or out of the oxide from a spatially uniform distribution of defects. The independent log-linear behavior following each voltage change can be explained by electrons tunneling in or out of defects from a different range of energies. This will be discussed more fully in the next section.

B. Discussion of the Model

Insight into the energy locations of the APC's can be gained from the results of figure 3. Consider for example the elevated temperature data (solid circles). Note the midgap voltage shifts to a more negative value as the applied field is changed from +4 MV/cm to less positive values. At the completion of the anneal with 0 MV/cm applied field (this corresponds to a small positive field across the Si-SiO_2 interface) the midgap voltage has shifted negatively by more than 0.2 volts. That is, electrons must be tunneling out of the oxide even though there is a net positive field across the Si-SiO_2 interface.

In the model proposed by Trombetta it is assumed that the APC's are energetically located near the silicon conduction band. Figure 5 schematically illustrates such a distribution for positive bias where the shaded region represents APC's occupied by electrons. Further, it is suggested by figure 5 that electrons whose energy is above the silicon conduction band edge have been removed from the APC defects by a tunneling process. As the applied bias is adjusted to less positive values there will be less band bending and additional APC's occupied by electrons will have their energies raised above the silicon conduction band. Therefore, following each bias switch more of the APC's occupied by electrons will have energy levels suitable for electron tunneling to the silicon conduction band.

Now consider the negative bias portion of the curve where the field is incrementally switched from 0 MV/cm to -4 MV/cm. Figure 6 schematically illustrates the mechanism for this set of anneals. After each change of applied field to a more negative value, the energy bands are bent further upward. As the bands are bent upward a new portion of the APC distribution is raised to energy levels equal to or above the silicon conduction band. The electrons, in the APC's raised to levels at or above the conduction band edge, can now tunnel out of the oxide. Recall that during each successive anneal the midgap voltage shifts linearly in log-time. After each bias change a new tunneling front starts from the interface and moves into the region of the oxide that is depicted schematically by the vertical line of the cutout portion of the distribution shown in figure 6.

Following the anneal with -4 MV/cm, the changes in field were increased by 1 MV/cm each day until +4 MV/cm was reached. It could be speculated that when the polarity of the bias changes is reversed that the curve would simply retrace the original curve. As can be seen in figure 3 this is not the case. The data remain flat until 0 MV/cm is reached for the 100°C case, and remains approximately flat until +2 MV/cm is applied in the room temperature case. This overall hysteretic behavior shown in figure 3 needs to be addressed in terms of the Trombetta model described above.

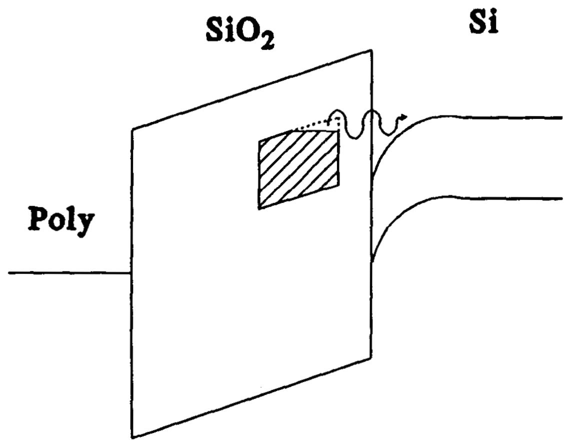

Figure 5. Schematic energy band diagram for positive bias. The shaded region represents APC's occupied by electrons. The wedge at top represents region where electrons can tunnel from.

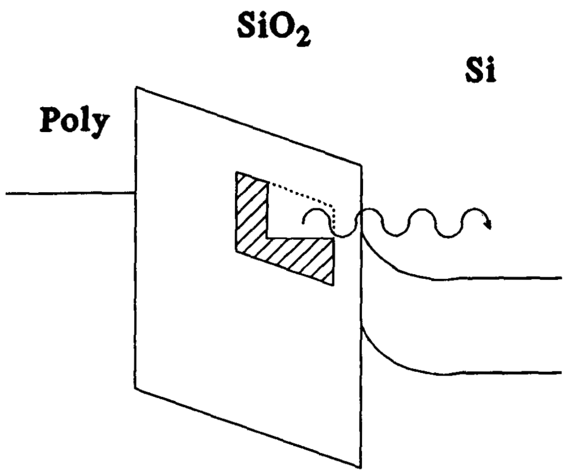

Figure 6. Schematic energy band diagram for negative bias. The shaded region represents APC's occupied by electrons. The unshaded region represents APC's that are positively charged.

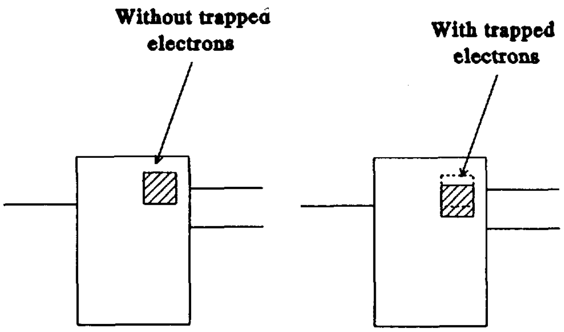

Figure 7. Schematic representation of the Zvanut model.

Hysteretic behavior similar to that shown in figure 3 has been observed by Zvanut et al. [14], during isochronal bias-anneal experiments, and supported by theoretical calculations by Fowler et al. [15] To explain their hysteresis, Zvanut et al. proposed a model that assumes the energy level of the defect is lower when occupied by an electron than when positively charged. This model is schematically illustrated in figure 7. The essence of this model can be described by the following. Consider a lone defect that is positively charged and at an energy level just above the silicon conduction band at flatband conditions. If the gate bias is adjusted positively just enough to lower the energy of the defect below the silicon conduction band edge and the defect captures an electron, it becomes charge neutral, and the energy level of defect will then be lowered. If the gate bias is returned to flatband condition the defect will remain charge neutral because it is now in a lower energy state. It is necessary to apply a negative gate bias to raise the energy level of the defect above the silicon band edge to allow the electron to escape. Upon releasing the electron the energy level of the defect is raised to its original state. Returning to the flatband condition then leaves the defect positively charged as it originally was.

Let us return to a discussion of the results shown in figure 3. Starting at the most positive applied field all of the APC defects are charge neutral and in their lower energy state. The +4 MV/cm (+3 MV/cm in the first cycle) applied field is sufficient to keep all of the APC defects below the silicon conduction band edge and charge neutral. As the applied field is lowered the degree of band bending is reduced, and at some applied field the most energetic defects are raised above the conduction band edge. Electrons in these defects can then escape to the substrate. This occurs at about +2 MV/cm for the room temperature case, and around 0 MV/cm for the elevated temperature case. Each time the voltage is subsequently reduced (1 MV/cm increments) a different energy band is raised sufficiently to allow electrons to tunnel out of the oxide. Finally when -4 MV/cm is reached, most of the defect distribution is raised above the bandgap. Since the APC defects are now positively charged they are in their higher energy state. The difference in energy levels of the two charge states is large enough so that the first few incremental bias changes to more positive values have very little effect on the number of defects positively charged, which explains the flat portions in each cycle shown in figure 3.

Further support for this model can be seen by comparing the two zero bias anneals during any cycle shown in figure 3. Note that in one case the electrons are tunneling into the oxide and in the other the electrons are tunneling out. During the sequence going from positive to negative, most of the APC's are compensated by electrons and are in the lower energy state with few above the silicon conduction band. Therefore most remain charge neutral. During the sequence going negative to positive most of the APC's are positively charged and thus the APC's are now in the higher energy state with most being above the silicon conduction band. Thus few electrons can tunnel into these defects until a more positive bias is applied, which explains why the midgap voltage shift is so much larger at zero applied field when the field has been changing from negative to positive.

C. Temperature Dependence of APC Charging

Comparing the 100°C data with the room temperature data in figure 2 shows the tunneling of electrons into and out of the APC's is slightly temperature dependent. There are several possible explanations for this. First, there might be a small temperature dependence of the tunneling rates. A second possibility is that there is a temperature dependence of the energy level distribution. Still a third possibility is that there is a small thermal component involved in this exchange of charge between the trap distribution and the silicon conduction band. Further work examining the temperature effects is needed to understand the differences seen in this data set.

V. COMPARISON WITH OTHER EXPERIMENTS

In this work it is shown that radiation-induced trapped positive can be separated into one of two types based upon their electrical properties following irradiation. Although it cannot be determined from these electrical measurements alone what the microscopic structure of these defects might be, it is interesting to consider the microscopic nature of the trapped holes and APC's. Several researchers have compared electrical measurements following irradiation with Electron Spin Resonance (ESR) measurements in an effort to determine the microscopic nature of radiation-induced trapped charge [16,17]. Lenahan et al. showed an approximate 1-to-1 correspondence between the number of E' centers determined by ESR and the number of trapped charges determined by C-V measurements. On the other hand, more recently Warren et al. have compared ESR measurements with C-V measurements, and found the number of trapped charges present was greater than the number of spins detected [17]. Furthermore, Trombetta et al. have generated APC's and observed no measurable ESR signal [18]. It seems clear that some of the trapped charge is in E' centers. Indeed, the majority of trapped positive charges may be in E' centers for some devices. Nevertheless, it is likely that a defect not to date detected by ESR measurements is responsible for some of the trapped charge.

Electrical measurements have also been compared with Thermally Stimulated Current (TSC) measurements by Fleetwood et al. [12]. The results of ref.11 show the majority of trapped positive charge annealing out between about 180°C and 250°C. As noted above, the APC's studied in this work were seen to be permanently removed at about 200°C. This temperature range lies within the dominant peak in the current vs. temperature data reported by Fleetwood et al. Based on this observation, it is unclear whether TSC measurements can distinguish APC's from trapped holes.

VI. SUMMARY

We have presented results from experiments designed to separate the electrical properties of two types of radiation-induced trapped positive oxide charge. During these experiments several important properties were observed regarding the annealing behavior of radiation-induced trapped positive charge. The data presented above is consistent with a model that assumes two species of trapped charge. The trapped holes can be removed by SHE electron injection leaving only the APC's, which can then be studied independently.

During this study, four important features were observed. The first is that the APC's charge and discharge approximately linearly in log-time. The second is that the charge state of the APC's is strongly field dependent. The third observation is that the APC defect is stable up to 160°C. Finally, and most interesting, is that the charging and discharging of the APC's is hysteretic.

From the above observations the following conclusions can be drawn. First, the APC's charge and discharge by electrons tunneling to and from the silicon conduction band. Secondly, the number of APC's that are positively charged is a complicated function of the applied oxide field. Third, the hysteretic behavior displayed during the isochronal anneals is due to a reduction in the energy level of the APC when occupied by an electron.

VI. ACKNOWLEDGEMENTS

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