Experimental Evidence of Two Species of Radiation Induced Trapped Positive Charge

R.K. Freitag, D.B. Brown, C.M. Dozier
Naval Research Laboratory
Washington, D.C. 20375

ABSTRACT

The effects of alternating bias anneals of MOS transistors following either x-irradiation or Fowler-Nordheim Tunneling have been studied. It is found that some of the generated defects can be repeatedly charged and discharged with a change of applied oxide field. Two models to explain this phenomenon are discussed. One assumes a single defect, the E' center. The other model assumes a two defect model. The results of this work are shown to be more consistent with the two defect model.

INTRODUCTION

In recent years, several studies have examined the annealing behavior of trapped positive oxide charge following a variety of electrical stresses [1-5]. In one such study by Trombetta et al. [1], MOS capacitors electrically stressed using either avalanche electron injection, Fowler-Nordheim tunneling, or avalanche hole injection resulted in fundamentally different annealing behavior of positive oxide charge depending upon the particular technique used. Capacitors stressed by avalanche electron injection resulted in some defects that could be reversibly charged or discharged by alternately applying gate biases of opposite sign. That is, these defects seem to charge and discharge with alternating bias, while showing little evidence of true annealing. Similar results to these were found following Fowler-Nordheim (FN) tunneling. In contrast to these FN tunneling and electron injection experiments, oxides exposed to avalanche hole injection showed very little charge reversibility, but showed a net removal of positive charge from the oxide when exposed to an alternating bias anneal.

More recently, Trombetta et al. [2] found an injection direction dependence in the type of defects generated by high field stressing of MOS capacitors. Specifically, when electrons are tunnel injected into the silicon dioxide, the nature of the positive charge generated depends upon whether the electrons are injected from the gate or from the substrate. Electrons tunnel injected from the substrate results in positive charge that is predominantly reversible with subsequent reverse bias anneals. On the other hand, electrons tunnel injected from the gate generate positive charge that is largely not reversible. From these experiments, it was inferred that two distinct species of positive oxide charge can be generated in the silicon dioxide layer of a MOS capacitor. Following the terminology of the above authors, we shall call the irreversible positive charge "trapped holes" and the reversible charge "Anomalous Positive Charge" (APC). The fundamental difference between the two is their behavior during switched bias anneals. The APC is a donor state that can repeatedly exchange charge via a tunneling mechanism with the silicon substrate and reverse its charge state with a change of the applied oxide field. A trapped hole does not exchange charge with the substrate but is irreversibly removed by tunneling of the hole out of the oxide to the substrate (or equivalently by an electron tunneling into the oxide).

Over the past ten years, several researchers studying the effects of ionizing radiation on MOS devices have shown that radiation-induced trapped positive charge can "reverse anneal" [6-9], a phenomenon quite reminiscent of the effects summarized above for charge injection experiments. A model proposed by Lelis et al. [7,8] assumes that radiation-induced positive charge is due to a single defect. In this model it is assumed that the radiation-induced holes are trapped close to the $Si\text{-}SiO_2$ interface. The observed annealing (reverse annealing) process is explained by electrons tunneling from (to) the silicon substrate. Under a positive applied bias an electron may tunnel from the silicon to the site of a hole trapping defect and recombine with the hole thereby irreversibly removing the defect. Alternatively, the electron may become trapped at a site nearby the hole trapping defect but not annihilate it. If a negative bias is applied this electron can tunnel back to the substrate. This second process is used to explain the reverse annealing that has been observed.

In this work we will report the results of several alternating bias annealing studies following FN injection or x-irradiation. The results of our injection experiments will be shown to be very similar to the results of previous studies [1,2]. The results of our radiation experiments will be compared to the two models summarized above.

EXPERIMENTAL PROCEDURE

Two types of MOS transistors were used in this study. The first was a set of n-channel transistors fabricated by the NRL Microelectronics Facility, and the second was a radiation hardened CMOS/SOS technology supplied by a commercial vendor. The NRL oxide thickness was 49 nm, and the CMOS/SOS oxide thickness was 35 nm. Both types of transistors used enclosed geometries. These devices were chosen to eliminate field oxide charging effects. Both device types have gate oxides that are relatively hard to radiation effects. Two sets of experiments were performed on the NRL devices. In the first set of tests, transistors were subjected to

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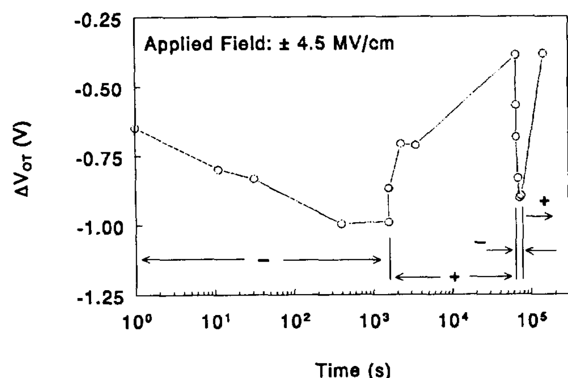

Figure 1. Annealing results following tunnel injection from substrate. Initial point immediately following injection. See text for annealing times and biases.

Fowler-Nordheim tunneling from either the gate or the substrate to see if we could reproduce the results of Trombetta et al. [1,2]. In the second set of tests devices from the same wafer were irradiated and the annealing properties studied as a function of applied bias and time. Similar radiation experiments were performed on the CMOS/SOS parts.

Several NRL devices were subjected to Fowler-Nordheim tunneling by applying an oxide field of approximately 8 MV/cm to generate positive charge in the oxide. Both positive and negative fields were applied. Following the FN injection, changes in the trapped positive charge were studied using several bias protocols. The bias switching protocol consisted of either an initial +4.5 MV/cm or -4.5 MV/cm field followed by one or more alternations of the bias. No measurable current flowed through the oxide layer at these fields. During these alternating bias experiments, changes in the net positive oxide charge were monitored by changes in the midgap voltage shifts, (ΔV_{OT}).

A second set of NRL devices was irradiated using a W-target x-ray source at a dose rate of about 165 krad(SiO_2)/

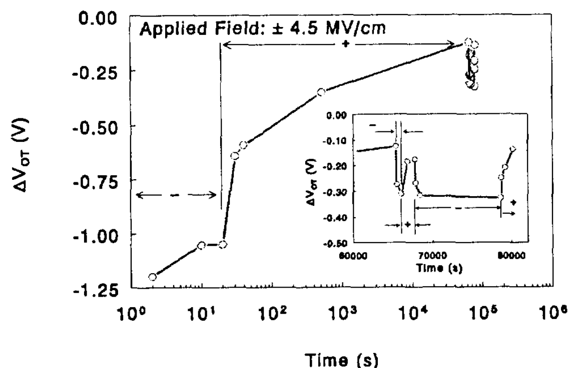

Figure 2. Annealing results following tunnel injection from the gate. Initial point immediately following injection. See text for annealing times and biases.

min. The total dose was 500 krad(SiO_2) and the applied field during irradiation was +1 MV/cm. Following irradiation these devices were subjected to alternating bias anneals to determine if both APC's and/or trapped holes were generated by the irradiation.

The transistors on the CMOS/SOS devices were irradiated with the x-ray source. The applied field was +1 MV/cm and the irradiation was to total doses of 250, 500, and 1000 krad(SiO_2). Following irradiation, the devices were subjected to various switched bias anneals.

EXPERIMENTAL RESULTS - FN INJECTION

In Figures 1 and 2, we present the results of the FN tunnel-injection from the substrate and gate respectively. In both figures the first data point represents the midgap voltage shift immediately following injection. Figure 1 (injection from the substrate) shows the results where the bias was held negative for the first 20 minutes, then switched positive for about 19 hours. Note that during this first positive bias anneal subsequent to the negative bias anneal about 60% of the trapped charge appears to have been removed. At this point, a negative bias was applied for 72 minutes, and 85% of the charge that seemed to be removed under positive bias returned. Finally a positive bias was reapplied and again it appears that the positive charge has been removed.

The behavior following injection from the gate, shown in Figure 2, is significantly different. After an initial 20 s negative bias anneal, the field was switched positive for 18 hours. About 85% of the positive charge appears to have been removed during this time. The insert shows the behavior following this positive bias anneal. The field was then switched negative for 11 minutes, then positive for 30 minutes, and then negative for about 3 hours. Note that during this 3 hour negative bias anneal, only about 15% of the charge that appears to have been removed during the 18 hour positive anneal returns. Finally, a positive bias anneal for 30 minutes again appears to remove positive charge from the oxide.

These FN tunnel injection data are consistent with the work of Trombetta et al. [1,2]. Tunnel injection from the gate generates trapped positive charge that can be largely removed by the application of a positive oxide field. This charge does not return under negative bias. On the other hand, tunnel injection from the substrate also results in trapped oxide charge. However, at least 50% of this charge cannot be permanently removed by the application of a positive oxide field at room temperature. Instead, these defects can be repeatedly charged and discharged by exchanging electrons with the substrate. These experiments support the hypothesis that both types of defects (trapped holes and APC) can be generated in this process technology.

EXPERIMENTAL RESULTS - IRRADIATION

To compare the effects of FN injection with the results of irradiation, we began with a 500 krad irradiation of

Point No.	Oxide Field (MV/cm)	Temp (C)	Time (min)	ΔV_{OT} (V)
0		R.T.	Pre Rad	0
1		R.T.	Post Rad	-1.24
2	2	R.T.	1020	-0.80
3	-4	R.T.	57	-0.94
4	+4	R.T.	50	-0.77
5	-4	R.T.	51	-0.89
6	+4	125	15	-0.72
7	-4	125	15	-0.87
8	+4	R.T.	1320	-0.60
9	-4	R.T.	66	-0.76
10	+4	R.T.	51	-0.60
11	+4	125	320	-0.46
12	-4	R.T.	66	-0.62
13	+4	125	1260	-0.40
14	-4	R.T.	66	-0.56

Table I Summary of Test Protocols for Fig. 3

a 49 nm NRL n-channel transistor. Following irradiation this device was subjected to an exploratory series of room temperature and elevated temperature anneals. Details of this annealing series are summarized in Table I. The results of this bias switching experiment are summarized in Figure 3 where the midgap voltage shift is plotted for each data point shown in Table I. Note that after each positive bias anneal ΔV_{OT} is less negative, while after each negative bias anneal ΔV_{OT} is more negative. This behavior implies there is a component of the radiation-induced positive charge that reversibly charges and discharges. Of interest in this figure is the fact that the shift following each negative bias anneal is of approximately the same magnitude for essentially the same anneal time. During each of these negative bias anneals, ΔV_{OT} shifts to a more negative value linearly at a rate of 25 mV per decade in log-time. This change, and in particular, this rate of change to a more negative value of ΔV_{OT} is reproducible independent of the amount of annealing/ compensation that has taken place during previous positive bias anneals. This behavior suggests that during each of these negative bias anneals, the electrons are tunneling out of a very similar oxide defect distribution.

A more systematic exploration of the results of positive and negative bias anneals is summarized in Figure 4. This figure shows the results of the annealing behavior of a 35 nm n-channel transistor on the CMOS/SOS device following irradiation to 1 Mrad with a +1 MV/cm applied field. The first and third panels show ΔV_{OT} as a function of time for an applied oxide field of +3.5 MV/cm. The second and fourth panels show ΔV_{OT} vs. time for an applied field of -3.5 MV/cm. First, note the linearity in log time of the curves during the negative bias anneals. This linearity is consistent with a model [10] that electrons are tunneling out of a uniform distribution of traps. Secondly, ΔV_{ot} at the end of panel 4 is about 0.1 volts less negative than the last point shown in panel 2. From the end of panel 2 to the end of

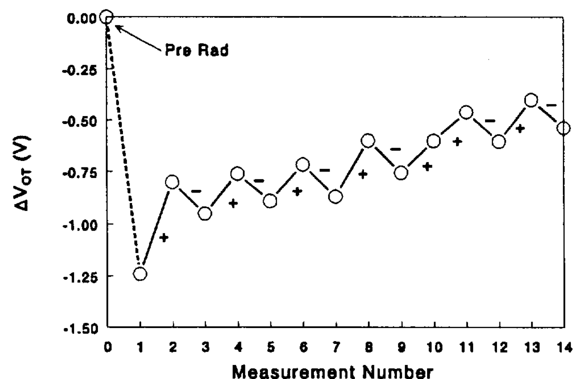

Figure 3. Example of annealing behavior of transistor with alternating biases. Horizontal scale is variable (see text and table).

panel 4, this transistor was negatively biased for more time than it was positively biased. Nevertheless, the net positive charge in the oxide has decreased. This decrease suggests that a component of the initial charge distribution has been permanently removed. Finally, in panel 4 it can be seen that the reverse annealing appears to be saturating in approximately 1-2x10^5 seconds. The total shift in panel 4 is about -0.5 volts. This result shown in panel 4 is consistent with the result shown in panel 2, although the negative bias anneal in panel 2 was terminated too soon to observe the saturation. This saturation behavior will be shown more clearly in Figure 5.

The annealing behavior following irradiation of a second CMOS/SOS device is shown in Figure 5. The strategy for this example was to anneal as much of the radiation-induced trapped charge as possible in a reasonably short time. A large reduction of trapped charge was obtained by a combination of radiation-induced annealing [10-12] and an overnight positive bias anneal. The first data point in the figure shows ΔV_{OT} following a 700 krad irradiation with a +1 MV/cm applied field. The second point shows the remaining voltage shift following the radiation-induced anneal. This consisted of a 300 krad irradiation with all leads shorted (0 V applied bias). In the remainder of the figure, ΔV_{OT} vs. time for applied fields of first positive then negative

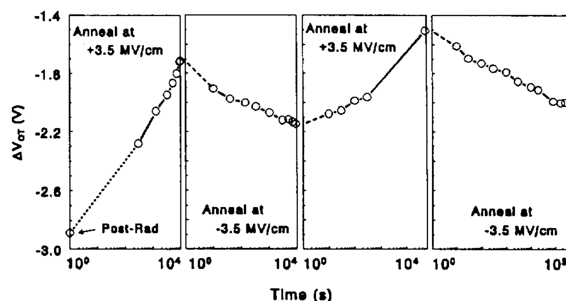

Figure 4. Four room temperature anneals illustrating the reproducibility of APC charging and discharging.

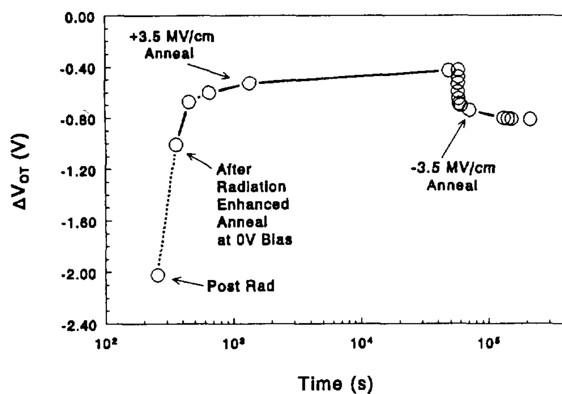

Figure 5. Illustrating that an 80% anneal of the radiation induced trapped charge does not affect the magnitude or time of the reverse shift due to APC discharging.

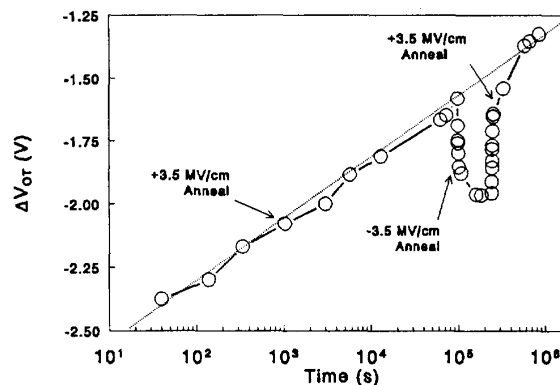

Figure 6. Illustration that trapped hole annealing is independent of APC charging and discharging.

3.5 MV/cm is plotted. The combination of radiation-induced annealing and a 15 hour positive bias anneal appears to have removed about 80% of the observed radiation-induced trapped charge. However, when the field was changed to -3.5 MV/cm, reverse annealing takes place and some charge appears to return. This data clearly shows the saturation of the reverse annealing, with ΔV_{OT} changing by about -0.38 V. That is, the last four data points are all within 10 mV of each other, which is within experimental error. As was the case for the data of Figure 4, this saturation is complete in about 1-2x10^5 seconds. It should be noted that a similar saturation behavior can be seen during the elevated temperature anneals in the work of Lelis et al. [5].

Figure 6 shows the results of a third CMOS/SOS device irradiated to 1 Mrad with a +1 MV/cm field. Here the applied bias during the anneal was first +3.5 MV/cm, then -3.5 MV/cm, and then returned to +3.5 MV/cm. During the first positive bias anneal ΔV_{OT} shifted toward zero linearly in log time as is expected. After about 10^5 seconds the bias was switched to negative and again reverse annealing occurred. Here also, saturation of this reverse annealing occurs in about 1-2x10^5 seconds with a total shift of -0.4 volts. After about 2x10^5 seconds under negative bias, the bias was changed back to +3.5 MV/cm, and again it appears that the positive charge is annealing. The interesting feature in this figure is the annealing curve returns to the same linear behavior as was shown by the first positive bias anneal. This observation suggests the following interpretation. During the first positive bias anneal, the APC's were neutralized by electrons tunneling from the substrate. Upon reversing the bias, these electrons tunnel out of the oxide into the silicon. During the second positive bias anneal, electrons tunnel into the oxide and again neutralize the APC's. Finally, the ΔV_{OT} versus time curve returns to the extension of the first positive bias anneal, implying that the APC's are charging and discharging independently of the trapped holes.

One common feature of Figures 4-6 is the negative bias reverse annealing always seems to saturate in approximately 2x10^5 seconds or less. The fact that the negative bias annealing saturates in approximately the same time for all of the CMOS/SOS devices studied suggests a way to quantify the relative number of APC's with respect to the number of trapped holes. That is, the difference in the midgap voltage of the device before and after a 2x10^5 second negative bias anneal is approximately equal to the midgap voltage shift due to the APC's.

In order to explore this idea further two additional transistors of CMOS/SOS type from the same wafer were irradiated with a +1 MV/cm applied oxide field. The first was irradiated to a total dose of 250 krad, and the second to 500 krad. Following irradiation both were maintained with a +3.5 MV/cm applied oxide field. After 10^5 seconds the field was reversed and maintained for 2x10^5 seconds. If we assume the difference in ΔV_{OT} between the beginning and the end of the negative bias anneal to be equal to ΔV_{OT} due to the APC's, then the difference between this value and the midgap voltage shift measured shortly following the irradiations is approximately equal to the midgap voltage shift due to the trapped holes generated during the irradiation. Let us define

$$\Delta V_{APC} = \Delta V(\text{post}) - \Delta V(\text{pre})$$

$$\Delta V_{HOLES} = \Delta V_{TOTAL} - \Delta V_{APC},$$

where post and pre refer to pre- and post-negative bias anneal, and ΔV_{TOTAL} is the measured midgap voltage shift following irradiation. These definitions permit us to quantify the relative proportion of APC to trapped holes following irradiation. The results of such a calculation are shown in Figure 7. Note that the generation of trapped holes is linear with dose. On the other hand, the generation of APC's is strongly nonlinear. The solid line in Figure 7 is of the form a[1-exp(-bD)], a commonly used functional form to describe saturation phenomena, where a and b are constants, and D is the dose.

Our results are corroborated by the results of a recent study where the anneal times were much longer. Fleetwood et al. [16] presented data where two transistors were irradiated to total doses differing by a factor of three. Following a positive bias anneal for 2.75 years to essentially anneal/compensate all the positive oxide charge, the bias was reversed. The midgap voltage shifts following these negative bias anneals both saturated and had the same magnitude, although there was a factor of three difference in total dose. A reasonable interpretation of their results could be the following. During the 2.75 year positive bias anneal essentially all of the trapped holes were annealed while the APC's were compensated. During the subsequent negative bias anneal, the APC's became uncompensated. The number of APC's for the two doses was the same because of a saturation of the number of APC's as suggested by Figure 7.

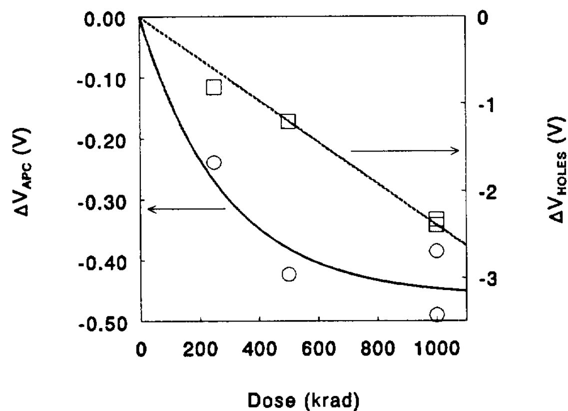

Figure 7. Dose dependence of radiation-induced trapped hole and APC generation. Note saturation of APC generation.

DISCUSSION

There have been several previous studies done on the annealing properties of radiation induced trapped positive charge [6-9]. It is generally accepted that with a positive gate bias during irradiation, electron hole pairs are created throughout the oxide. The photoelectrons are rapidly swept out through the gate, while the holes migrate toward the Si-SiO_2 interface where some fraction is trapped at sites close to the interface. It is usually observed that during a positive bias anneal following irradiation the trapped positive charges anneal out at a rate that is approximately linear in logarithmic time. Log linear annealing has been interpreted to imply a tunneling process, where electrons tunnel from the substrate to traps sites that are uniformly distributed out to some distance from the interface [13]. It has also been observed that following a subsequent negative bias anneal, some positive charge returns. Reverse annealing has been explained by a process where electrons tunnel out of the traps back into the silicon [7,8]. However, it is typically observed that not all of the trapped positive charge can be retrieved. That is, some trapped charge truly anneals, and some can only be compensated or neutralized, but the defect is not removed.

In a model proposed by Lelis et al. [7,8], the radiation generated hole breaks a strained Si-Si bond at the site of an oxygen vacancy to form a complex commonly called the E' center [14]. The annealing/compensation of a trapped hole is explained by an electron tunneling to a site near the trapped hole, thereby establishing electrical neutrality without removing the trapped hole. If a negative bias is applied before the electron and hole recombine, the electron can tunnel back to the silicon leaving a net positive charge. Alternatively, the electron can recombine with the trapped hole, i.e., truly anneal. The work of Lenahan [14] et al. is used to support this model. In this work the number of radiation-induced trapped positive charges deduced from C-V measurements correlates very well with the number of E' centers determined by Electron Spin Resonance (ESR). It should be noted that there is a relatively large uncertainty in the absolute density of spins determined by ESR (perhaps as much as a factor of 2). There is also some uncertainty in the number of trapped charges determined from C-V measurements. Therefore it is possible that some fraction of the radiation-induced defects could be APC,s and yet find a good correlation between the E' centers and positive charge.

Several researchers [3-5] studying the annealing behavior of oxide trapped charge following electron injection have shown the existence of more than one form of trapped positive charge. In particular the work by Trombetta et al. [3], and Buchanan et al. [4] show that significant positive charge can be generated with little or no ESR signal being detected. Warren et al. [5] have shown a very poor correlation between the number of E' centers and the amount of trapped positive charge following electron injection. From these experiments, it is clear that the E' center is not the only positively charged defect that can be generated in SiO_2 insulating layers. The remaining question is whether ionizing radiation can generate more than one defect type. The work of Stahlbush et al. [15]. showed that the number of radiation-induced defects that can reversibly exchange charge with the substrate is a function of the amount of hydrogen in the oxide. Since hydrogen is not a constituent of the E' complex, this hydrogen related effect argues strongly for the existence of a second radiation-induced defect.

An alternative model that includes two distinct forms of trapped positive charge, presented in the paper by Trombetta et al., is more reasonable than a single defect model [1]. This model is consistent with all of the data shown in this paper. Furthermore, the data in the papers by Lelis et al. [4,5] is also entirely consistent with this model. This model assumes two distinct positively charged defects (APC centers and trapped holes). The distinguishing electrical characteristic is the annealing behavior as described earlier. Secondly this model assumes these two defects are located at different energy levels. The energy level of the first (trapped hole) is below the silicon valance band edge. Trombetta et al.

ascribe the removal of this defect to tunneling from the oxide into the substrate. This tunneling process is shown in Ref. 1 to occur under any applied bias, although the annealing rate is bias dependent. The second defect (APC) on the other hand, readily exchanges charge with the silicon via a tunneling process, and these authors suggest that this likely puts them within the silicon bandgap.

It is difficult to explain the data of Figures 4-6 using a single defect model. Consider, as an example, the data of Figure 5. Assume that during the initial 700 krad positive bias irradiation, positive charge is trapped with a distribution that is approximately uniform and near the Si-SiO_2 interface. This assumption is supported by the linearity of the positive bias anneals shown in Figures 4 and 6 for similar devices. The following 300 krad zero bias irradiation anneals or compensates about half of this charge. Following this zero bias radiation-induced anneal was a 15 hour positive bias anneal which further neutralized the positive charge. This procedure resulted in about 80% of the radiation-induced positive charge being neutralized. Since the photoelectrons are generated uniformly throughout the entire oxide layer as well as in the silicon, it follows then, that the radiation-induced annealing (compensating) of the trapped charge should also be uniform throughout the entire trap distribution. This is very different from the case where a sample is only exposed to a positive bias anneal. Figure 6 shows that following the positive bias anneal about 33% of the charge has been neutralized in that transistor. If one assumes a single defect model with charge neutralization proceeding via a tunneling mechanism, then those defects closest to the interface will be neutralized at a much greater rate than those farther away. That is, trapped charges closest to the interface have a greater probability of being neutralized, whereas those farther away will probably still be positively charged. It follows then, that number and distribution of compensated charge in the device exposed to only a positive bias anneal is most likely to be very different than in the device that was exposed to radiation-induced annealing.

Given the difference in treatment these two devices received it seems unlikely, assuming a single defect model, that the negative bias annealing curves in Figures 5 and 6 should be so similar. First, the time to saturation should not be the same. If a single defect were responsible, it would be expected that the time to saturation would be longer for the sample subjected to a zero bias irradiation. This increased duration would be due to the charge neutralization extending throughout the entire charge distribution. Secondly, the transistor of Figure 5 had 80% of its charge neutralized before the negative bias anneal, and the transistor of Figure 6 had only about 33% of its charge neutralized. A single defect model would predict a larger midgap voltage shift following a negative bias anneal for the sample with more charge previously neutralized. That was not observed during the anneals in this work.

A third argument can be made from the data shown in Figure 3. From point 1 to point 13, 60 percent of the radiation-induced charge was neutralized. Yet the magnitude (after approximately the same time) of the change in ΔV_{OT} during each of the room temperature negative bias anneals remained fairly constant. The constant shift implies that the number of reversible defects within some distance from the interface remained constant. If the total number of E' centers decreased during the positive bias anneals, it seems unlikely that the number and density that could be repeatedly charged and discharged would remain constant.

The data shown in Figure 7 is also inconsistent with a model that assumes electrons are tunneling from the substrate and get trapped at sites near the E' centers. The fact that the number of radiation-induced defects that can reversibly charge and discharge with alternating bias seems to saturate with dose argues against a single defect model. That is, it seems very unlikely that as more E' centers are generated with increasing dose that the electron trapping sites would not increase accordingly.

The model of Trombetta et al. is supported by the data presented above. Figure 3 shows five room temperature negative bias anneals following variable time intervals under positive bias. The net amount of positive charge before each of these anneals is variable. Yet the response during each negative bias anneal is very similar despite the previous annealing history. This is consistent with the existence of a defect that does not truly anneal. Under positive bias, electrons tunnel into the oxide and anneal some of the trapped holes and compensate the APC's out to some distance into the oxide depending upon the time under positive bias. During the negative bias anneals, only the electrons compensating the APC's return to the substrate. That the rate and the amount of this reverse anneal is the same for all room temperature anneals independent of the total amount of trapped charge prior to the negative bias anneals is consistent with the two defect model. The similarity between the negative bias annealing behavior that is shown in Figures 5 and 6 also supports a two defect model. In both cases about 0.4 V of the initial midgap voltage shift can be attributed to APC's. That they both anneal the same amount in the same time (even though the initial neutralized charge distribution was very different for these two examples) argues strongly for a separate defect being responsible for the reversible component. The remaining (non-reversible) fraction then is due to trapped holes. Figure 7 implies that the total number of APC centers that can be generated is limited. About 500 krad is sufficient to saturate these devices. This saturation phenomena is more consistent with a two defect model. The total number of APC centers that can be generated is likely to be highly process dependent. This would be true if, as Stahlbush et al. [15] have shown, that the number of APC centers that can be generated is in some way related to the hydrogen content in the device.

SUMMARY AND CONCLUSIONS

We have presented data that supports a model that assumes the existence of two distinct species of trapped positive charge following irradiation. The major distinguishing characteristic is the difference in their annealing behavior. The first type (trapped holes) anneal irreversibly. The second type (Anomalous Positive Charge) can be charged and discharged repeatedly by applying alternating bias anneals. The time to charge or discharge these defects in the devices used in this work is about 1-2 x 10^5 seconds for the bias conditions studied. The trapped holes will irreversibly anneal at room temperature, whereas the APC's appear to show little annealing at room temperature. The density of APC's that can be generated appears to saturate with increasing dose independent of the number of trapped holes present. For the devices used in this study, the number of APC's saturate at approximately 500 krad. The density of trapped holes on the other hand, was shown to increase linearly with dose up to 1 Mrad. A second model has been considered. This model assumes a single defect, the E' center. It has been shown that the two defect model is more consistent with the annealing properties of the devices used in this work. The two defect model is also consistent with recent work presented by Fleetwood et al. [16] as well as Stahlbush et al. [15]. Both of these efforts also show data that is hard to explain with a single defect.

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