ON-CHIP p-MOSFET DOSIMETRY

M. G. Buehler, B. R. Blaes, G. A. Soli, and G. R. Tardio
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, CA 91109

ABSTRACT

On-chip p-FETs were developed to monitor the radiation dose of n-well CMOS ICs by monitoring threshold voltage shifts due to radiation induced oxide and interface charge. The design employs closed geometry FETs and a zero-biased n-well to eliminate leakage currents. The FETs are operated using a constant current chosen to greatly reduce the FET's temperature sensitivity. The dose sensitivity of these p-FETs is about -2.6 mV/krad(Si) and the off-chip instrumentation resolves about 400 rad(Si)/bit. When operated with a current at the temperature-independent point, it was discovered that the pre-irradiation output voltage is about -1.5 V which depends only on design-independent silicon material parameters. The temperature sensitivity is less than 63 μV/°C over a 70°C temperature range centered about the temperature insensitive point.

1. INTRODUCTION

The use of FETs (Field-Effect Transistors) as dosimeters was pioneered by Holmes-Siedle [1]. A number of these devices have flown on earth bound satellites [2 - 4].

In recent years, p-FET dosimeters have been developed with specially-grown thick-gate oxides which have a large number of oxide traps. Sensitivities of >10 mV/rad(Si) [5] have been achieved. The sensitivity to radiation can be enhanced by applying a large positive bias during radiation which forces more of the positive oxide charge to the interface. The sensitivity to temperature can be minimized by operating the p-FET with a current at the temperature-independent point [6, 7].

In this work, a p-FET dosimeter is developed under the constraint that the dosimeter be useful in predicting the radiation dose of an IC fabricated with a non-radiation hardened 1.2-μm CMOS process. As shown in Fig. 1, two p-FETs were fabricated on the RADMON (Radiation Monitor), which also includes an SEU-SRAM for monitoring particle upsets. This appears to be the first time a p-FET dosimeter was fabricated in a fine-line, thin-oxide semiconductor technology.

The p-FET is biased to about -1.5 V during measurement and is unbiased when not being measured. This approach to biasing is intended to provide a known bias environment at all times. In certain applications, the availability of spacecraft power is unpredictable. Thus, being unbiased during irradiation provides a known bias scenario.

On-chip dosimetry provides the advantage that the dose is measured directly next to the IC. This reduces the uncertainty inherent in dosimetry calculations which are complicated especially for highly shielded electronics.

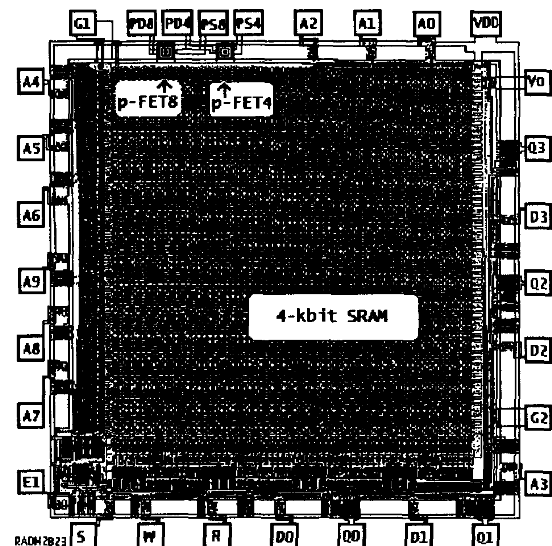

Figure 1. STRV-RADMON chip 2.6 mm x 2.7 mm.

2. p-FET DESIGN

The RADMON, shown in Fig. 1, contains two p-FETs. The geometry of p-FET4 is W/L = 182/4 μm/μm and p-FET8 is W/L = 182/8 μm/μm where W and L are the channel width and length, respectively. The layout of the p-FET, shown

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in Fig. 2, features a closed geometry design where the drain completely surrounds the source. The closed geometry eliminates the bird's beak or channel-edge leakage encountered in a linear FET.

The schematic cross section of the device, shown in Fig. 3, indicates that the n-well and source are separated so they can operate at slightly different biases required by the operational amplifier, U1. This allows all the forced current to flow through the p-FET channel. Drain-to-well leakage is shunted to ground. Grounding the n-well is a departure from normal CMOS circuit operation where the n-well is normally connected to VDD.

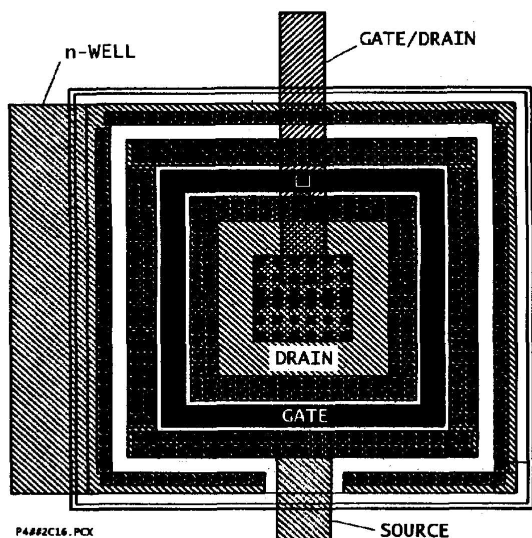

Figure 2. p-FET, MP4, layout where the gate length is L = 4 μm and width is W = 182 μm.

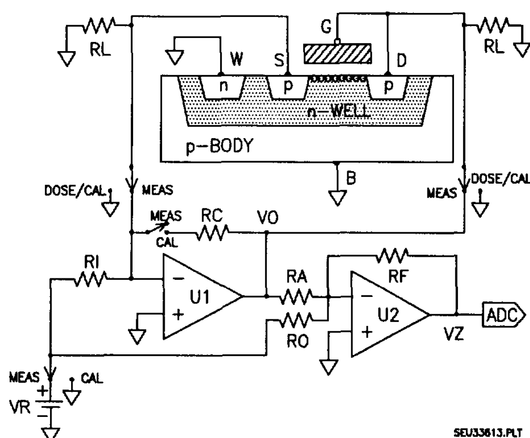

Figure 3. p-FET total dose circuitry.

In operation, all terminals of the p-FET are operated near ground except the drain which operates near VO = -1.5 V. During irradiation, the device is biased in the off state. The two RL resistors are used to bleed off any charge remaining on the p-FET. The instrumentation is calibrated by positioning the switch to CAL shown in Fig. 3. This replaces the p-FET with calibration resistor RC.

The p-FET constant drain current, ID, is established by VR and RI or ID = VR/RI. The output of amplifier U1 is scaled by U2 so that it makes maximum use of the range of the 8-bit ADC (Analog-to-Digital Converter). As seen in Fig. 3, the gate is connected to the drain. This insures that the p-FET is operated in saturation.

3. p-FET MODEL EQUATIONS

In saturation the p-FET drain current [7] is:

$$(1)\quad ID = \frac{\beta}{2}\cdot\frac{(-VO + VT)^2}{1 + \theta(-VO + VT)}$$

where VO is the p-FET output voltage, $\beta = KP\cdot W_e/L_e$, $KP = \mu\cdot C_0$ and VT is the p-FET threshold voltage. $W_e = W - \Delta W$ and $L_e = L - \Delta L$ are the effective channel width and length, respectively, μ is the zero-field channel mobility, C_0 is the gate oxide capacitance per unit area, and θ is the mobility electric-field degradation parameter.

The above equation was simplified by taking its square root. Then the θ term was linearized using Taylor Series expansion:

$$(2)\quad \sqrt{ID} = \sqrt{\beta/2}(-VO + VT)[1 - \frac{\theta}{2}(-VO + VT)]$$

Expressions for the temperature and dose dependence of VT, β, and θ are given below. The equations are expanded about the reference temperature T_0. In these equations, the temperature and dose effects are assumed to be independent. That is, the equations do not include a dose·temperature product term.

The threshold voltage is described by:

$$(3)\quad VT = VT_0 + VT_T(T - T_0) + VT_D\cdot D$$

where D is the dose, VT_0 is the threshold voltage at T_0 and D = 0, $VT_T = \partial VT/\partial T|_{T\to T_0}$ and $VT_D = \partial VT/\partial D|_{D\to 0}$. The temperature [7] and dose dependence [8] of β is given by:

$$(4) \quad \beta = \beta_0 (T/T_0)^{-n} + \beta_D \cdot D$$

where β_0 is β evaluated at T_0 and $D = 0$, $\beta_D = \partial\beta/\partial D|_{D\to 0}$, n characterizes the mobility temperature dependence, and T is the absolute temperature. For $D_T = \partial D/\partial T = 0$:

$$(5) \quad \beta_T = \partial\beta/\partial T = -n \cdot \beta/T$$

The temperature and dose dependence of θ is given by:

$$(6) \quad \theta = \theta_0 + \theta_T \cdot (T - T_0) + \theta_D \cdot D$$

where θ_0 is θ evaluated at T_0 and $D = 0$, $\theta_T = \partial\theta/\partial T|_{T\to T_0}$ and $\theta_D = \partial\theta/\partial D|_{D\to 0}$.

4. p-FET TEMPERATURE EQUATIONS (INCLUDING θ)

In this section the p-FET equations are derived including the θ parameter. This allows an accurate analysis at the operating or measurement temperature, T_m. This temperature is usually different from the reference temperature, T_0. The measurement temperature, T_m, might be the mean spacecraft operating temperature.

The p-FET output voltage follows from Eq. 2. The solution requires solving the equation which is quadratic in VO:

$$(7) \quad VO = VT - \frac{1}{\theta} \cdot (1 - \sqrt{1 - \theta \cdot \sqrt{[8 \cdot ID/\beta]}})$$

The sign of the square root is negative which can be verified by evaluating this equation in the limit $\theta \to 0$. The value of VO at T_m is calculated from:

$$(7a) \quad VO_m = VT_m - \frac{1}{\theta_m} \cdot (1 - \sqrt{1 - \theta_m \cdot \sqrt{[8 \cdot ID_m/\beta_m]}})$$

The current, ID_m, at the measurement temperature is found from the above equation by setting $\partial VO/\partial T|_{T\to T_m} = 0$ and solving the resulting quadratic equation for ID_m:

$$(8) \quad \sqrt{ID_m} = + \frac{A}{2} - C \pm E \cdot \sqrt{[1 + B \cdot (-C + A/4)]}$$

where

$$(9) \quad A = a^2 b/d^2$$
$$(10) \quad B = b$$
$$(11) \quad C = c/d$$
$$(12) \quad E = a/d$$
$$(13) \quad a = VT_T + \theta_T/\theta_m^2$$
$$(14) \quad b = -\theta_m \cdot \sqrt{(8/\beta_m)}$$
$$(15) \quad c = \theta_T/\theta_m^2$$
$$(16) \quad d = -[(2\theta_T/\theta_m) - (n/T_m)]/\sqrt{(2\beta_m)}$$

The sign of the square root in Eq. 8 is positive for $\theta > 0$ and negative for $\theta < 0$.

5. p-FET TEMPERATURE EQUATIONS (θ = 0)

The equations derived in Section 4, include the θ parameter. Since θ is small, it is neglected in this section to gain physical insight into the meaning of the equations.

The p-FET IV characteristics are plotted in Fig. 4 using Eqs. 1, 3, and 4 for D = 0 and the parameters [7] listed in the Fig. 4. This figure shows that the so called "temperature independent" point is in fact ill-defined when viewed in detail.

In this analysis, the most important p-FET parameter is VO. Its temperature dependence is analyzed by expressing Eq. 2 as follows:

$$(17) \quad VO = VT - \sqrt{2ID/\beta}$$

The VO is calculated for D = 0 using Eqs. 3 and 4 and plotted in Fig. 5. These curves show that there is a point at which VO is independent of temperature. This point is determined by differentiating Eq. 17 with respect to temperature and setting the result to zero. This leads to the simple expression for the measurement current:

$$(18) \quad ID_m = 2\beta_m^3(-VT_T/\beta_{Tm})^2$$

The value for ID_m = 19.2 µA was calculated using the parameters shown in Fig. 5. The five curves were plotted with ID values that vary by one percent. This shows the effect of missing the target current of ID_m. As seen in the figure, the peak in the curve moves to higher temperatures as ID increases. The value of VO changes by 0.25 percent for a one percent change in ID.

The temperature sensitivity of VO can be expressed simply by combining Eqs. 4, 5, 17, and 18 which leads to:

$$(19) \quad VO_T = \partial VO/\partial T = VT_T[1 - (T_m/T)^{1-n/2}]$$

This shows that $VO_T = 0$ at $T = T_m$ for any n or $VO_T = 0$ for n = 2 for all T.

The effect of temperature variations on VO_T is analyzed with the help of the horizontal line shown in Fig. 5. This line is 1 mV below the target value of VO_m = -1.5 V. The value of 1 mV was chosen because it is the same magnitude as the dose effects to be measured. The VO_T = -63 µV/°C at point "a" and 63 µV/°C at point "c" seen in Fig. 5. The temperature range between "a" and "c" is more than 70°C. This means that VO_T is less than ±63 µV/°C over the 70°C temperature range centered at the measurement temperature, T_m. This is a significant

improvement in the uncompensated temperature sensitivity of VT_T = 2 mV/°C used in calculating Figs. 4 - 6.

The solution for n = 2 means that the curves shown in Fig. 5 have zero slope. For this case, the p-FET IV characteristics display a true temperature insensitive point as shown in Fig. 6.

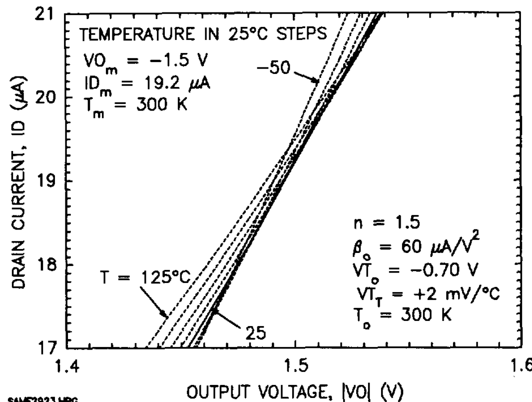

Figure 4. Expanded p-FET IV characteristics showing that the "temperature independent" point is not a point. Note n ≠ 2.

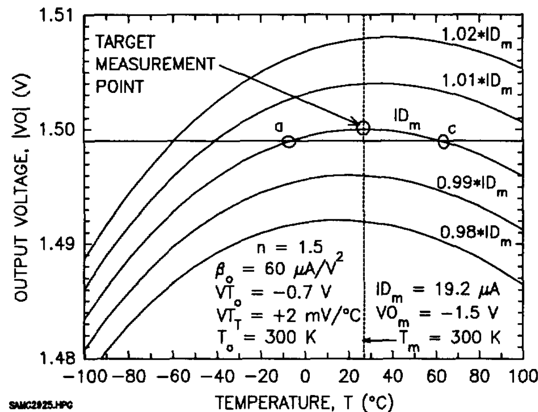

Figure 5. The temperature and current dependence of the p-FET output voltage using Eq. 17.

Next, ID_m is analyzed for design purposes by substituting $\beta_m = KP_m W_e/L_e$ into Eq. 18; this leads to:

$$(20)\quad ID_m = 2KP_m(VT_T \cdot T_m/n)^2 W_e/L_e$$

This equation shows that ID_m depends on the silicon parameters, KP_m, VT_T, and n, the measurement temperature, T_m, and the FET geometry. Thus, once the silicon parameters and T_m are known, the designer is free to choose ID_m by adjusting W and/or L.

Finally, VO is analyzed for design purposes by substituting Eqs. 5 and 18 into Eq. 17:

$$(21)\quad VO_m = VT_m - 2VT_T \cdot T_m/n$$

This equation shows that VO_m depends on the silicon parameters, VT_0, VT_T, and n and the measurement temperature, T_m. Note that VO_m is independent of FET W/L geometry. Thus the designer has no control over this value. In this study, the value for VO_m is about -1.5 V. With irradiation, VO_m becomes more negative. The initial VO_m value is important from an instrumentation stand point. Since the ADC shown in Fig. 3 has an input voltage range between 0 to 5 V, the pre-radiation value for VZ in Fig. 3 is set to zero volts by compensating VO_m by setting $RO = -RA \cdot VR/VO_m$.

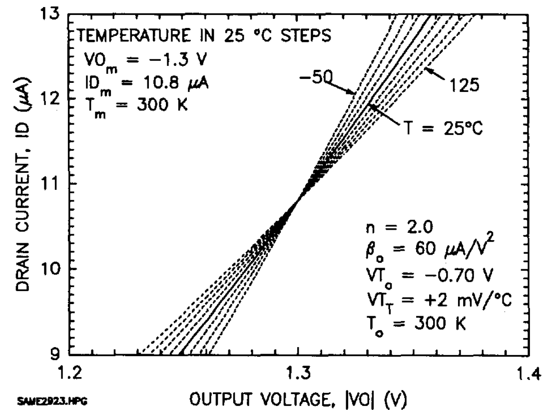

Figure 6. Expanded p-FET IV characteristics showing a true temperature independent point for n = 2.

6. p-FET TEMPERATURE DATA ANALYSIS

The p-FETs were measured in packages in an oven using an hp4062 parametric test system. The temperatures are estimated to be accurate to within ±1°C. The measurements were obtained by forcing VO = 2 V and measuring ID_5. Then four additional currents were forced at $\sqrt{ID_1} = 0.2 \cdot \sqrt{ID_5}$, $\sqrt{ID_2} = 0.4 \cdot \sqrt{ID_5}$, $\sqrt{ID_3} = 0.6 \cdot \sqrt{ID_5}$, and $\sqrt{ID_4} = 0.8 \cdot \sqrt{ID_5}$. Once these values are determined, they are used throughout the rest of the measurements.

The experimental data, shown in Fig. 7, was fitted using the method of least squares. In

the analysis, the following parabolic equation was used. The coefficients of the equation were related to the parameters in Eq. 2:

(22) $\sqrt{ID} = a_0 + a_1 \cdot VO + a_2 \cdot VO^2$

where

(23) $a_0 = \sqrt{(\beta/2)} \cdot VT \cdot (1 - \theta \cdot VT/2)$

(24) $a_1 = -\sqrt{(\beta/2)} \cdot (1 - \theta \cdot VT)$

(25) $a_2 = -\sqrt{(\beta/2)} \cdot \theta/2$.

The "a" parameters are used to obtain VT, ß, and θ for each IV curve. The VT solution was obtained by setting VO = VT at ID = 0. This leads to a quadratic equation whose solution is:

(26) $VT = a_1/(2a_2) \cdot (-1+\sqrt{1-4a_0a_2/a_1\text{^}2})$

The sign of the square root is positive. This can be verified by setting θ = 0 or a_2 = 0. The solution for ß is:

(27) $\beta = 2(a_1 + 2a_2 \cdot VT)^2$

The solution for θ is:

(28) $\theta = 2a_2/(a_1 + 2a_2 \cdot VT)$

The IV points, shown in Fig. 7, were fitted using the above procedure. The ß, VT, and θ values are listed in Table 1 for three temperatures.

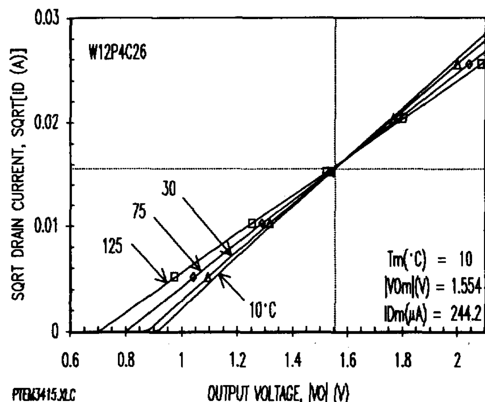

Figure 7. 1.2-µm CMOS p-FET IV temperature response for flight chip number W12P4C26.

The temperature parameters for VT and θ were extracted by least squares fitting the data listed in Table 1 by using Eqs. 3 and 6. The temperature parameter for ß was extracted using Eq. 4 after it was linearized by taking the logarithm. The temperature parameters are listed in Table 2.

Values for ID_m and VO_m were calculated using Eqs. 7a and 8 and the parameters listed in Table 2. The results are listed in Table 2 and plotted as the vertical and horizontal lines in Fig. 7.

Table 1. Flight p-FET4 Parameters (W12P4C26)

T °C	VT V	ß mA/V^2	θ 1/V
30	-0.874	1.100	0.056
75	-0.800	0.891	0.041
125	-0.703	0.708	0.027

Table 2. Flight p-FET4 Parameters (T_o = 300 K, T_m = 10°C, W12P4C26)

PARAM	UNITS	MEAN STDEV
X_o	nm	21.8*
W	um	182
L	um	4
ΔL	um	0.3459*
VT_o	V	-0.8821±0.0051
VT_T	mV/°C	1.8002±0.0800
β_o	mA/V^2	1.1240±0.0110
KP_o	$\mu A/V^2$	24.7041±0.2423
n	--	1.6140±0.0528
β_{To}	$(\mu A/V^2)/°C$	-6.0471
θ_o	1/V	0.0571±0.0013
θ_T	(1/kV)/°C	-0.3153±0.0210
VT_m	V	-0.9125
β_m	mA/V^2	1.2339
θ_m	1/V	0.0624
β_{Tm}	$(\mu A/V^2)/°C$	-6.6384
ID_m	µA	244.2
VO_m	V	-1.554

* MOSIS supplied parameter.

7. p-FET DOSE DATA ANALYSIS

The p-FET dose dependence was determined using Cobalt-60 irradiation. The devices were irradiated with their lids on, at room temperature, at 1 rad/sec, and at zero bias. The p-FETs were measured at room temperature within 15 minutes after the Cobalt-60 irradiation. The p-FET were also annealed at room temperature for times measured after the final irradiation.

The p-FET irradiation results, shown in Fig. 8, were fitted using Eq. 22. This produced a

set of VT, ß, and θ values for each dose value. These values are plotted in Figs. 9 to 11 for four p-FETs. The radiation results are listed in Table 3 for one of the p-FETs.

The VT values, plotted in Fig. 9, show a high degree of linearity during irradiation and a slight recovery with anneal. The group average slope of the VT vs dose curve during irradiation is VT_D = -1.698±0.038 mV/krad(Si). The shift in VT with radiation is consistent with the build up of positive oxide charge and interface states. The slight recovery of VT during room temperature anneal is consistent with the slight loss of oxide charge. The interface state density is stable as seen by the flat response of the mobility during anneal.

The ß values were converted to zero-field hole channel mobility using:

$$(29)\quad \mu = (L - \Delta L)\cdot \beta/(W\cdot C_0)$$

In this analysis, the value for C_0 was calculated using the MOSIS supplied value for the gate-oxide thickness, X_0 = 21.8 nm.

Table 3. Ground Test p-FET Cobalt-60 Radiation Parameters for Chip Number W12P4C05

PAR.	UNITS	MEAN STDEV
VT_D	mV/krad(Si)	-1.674±0.004
β_D	$\mu A/V^2$/krad(Si)	-3.585±0.164
KP_D	$\mu A/V^2$/krad(Si)	-0.079±0.004
θ_D	1/kV/krad(Si)	-1.184±0.018
VO_{Dm}	mV/krad(Si)	-2.591±0.018

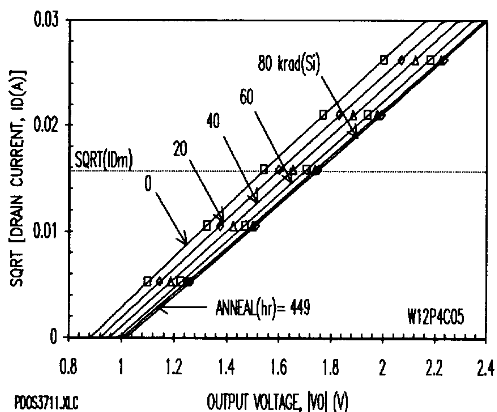

Figure 8. 1.2-μm CMOS p-FET IV dose/anneal response for chip number W12P4C05.

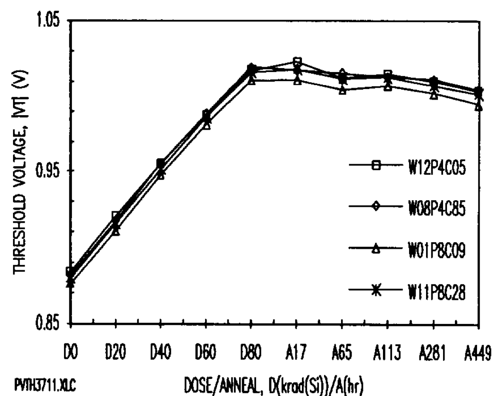

Figure 9. Four 1.2-μm CMOS p-FET threshold voltage dose/anneal responses.

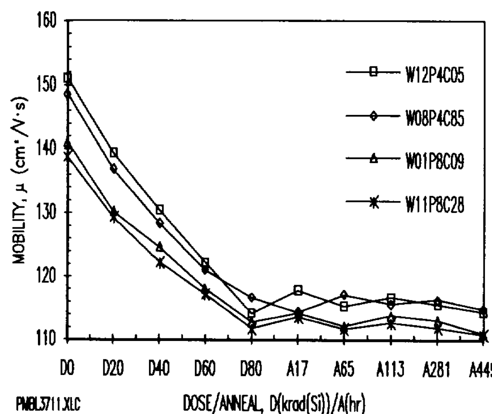

Figure 10. Four 1.2-μm CMOS p-FET hole mobility dose/anneal responses.

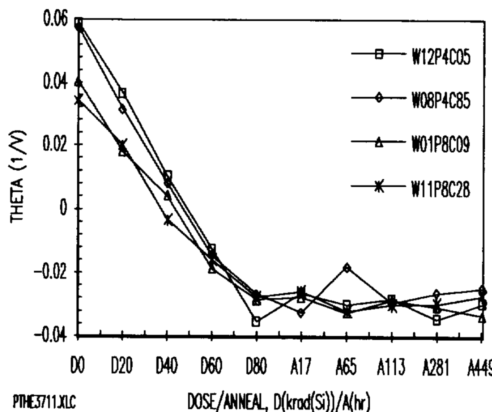

Figure 11. Four 1.2-μm CMOS p-FET theta dose/anneal responses.

The data, shown in Figure 10, are clustered according to the p-FET's W/L ratios. This ratio is designated by the "P" number given in the wafer number listed in the figure. That is, for P4 the ratio is W/L = 182/4 μm/μm and for P8 the ratio is W/L = 182/8 μm/μm. This dependence on the W/L ratio does not affect the output voltage, for VO is geometry independent as seen in Eq. 21.

As seen in the Fig. 10, μ is stable after annealing. The build up of positively charged interface states during irradiation degrades the mobility due to the increase in channel scattering centers [9]. Since the mobility does not anneal at room temperature, the interface state density is stable.

The θ values, shown in Fig. 11, are clustered according to the p-FET W/L ratios. The characteristics show no annealing, which indicates that the interface state density is stable during annealing.

The θ parameter represents the curvature term for the parabolic equation given in Eq. 2. The curvature is difficult to see in Fig. 8 because θ is very small. As seen in Fig. 11, the maximum value for θ is 0.06 1/V. The influence of θ in Eq. 2 is less than 3 percent because it enters as $\theta/2$. This small value for θ justifies the use of the Taylor Series expansion in simplifying Eq. 2.

As shown in Fig. 11, θ is positive at low dose and negative after high dose and anneal. The sign of θ indicates the direction of the $\sqrt{ID}$ vs VO parabola given by Eq. 2. This point is illustrated in Fig. 12. For $\theta > 0$ the parabola points down and for $\theta < 0$ the parabola points up. For $\theta = 0$, the $\sqrt{ID}$ vs VO relationship is a straight line.

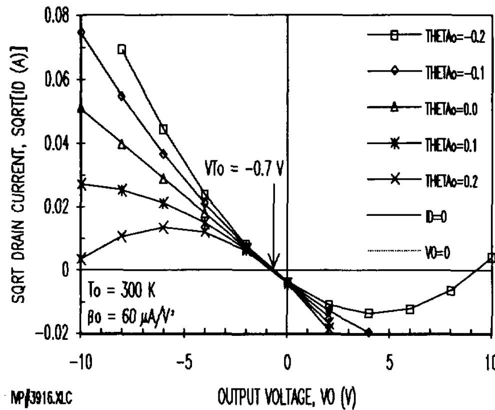

Figure 12. Plot of Eq. 2 for different θ values.

8. DOSIMETRY

The device dose sensitivity is derived in this section. Since the dose is measured at the constant current, ID_m, the radiation dose sensitivity of VO is greater than VT_D. This is evident in Fig. 8 where the spread in the curves is wider at ID = ID_m than at ID = 0 due to the dose dependence of the mobility.

In this section the output-voltage dose sensitivity, VO_D, for $\theta = 0$ is calculated by differentiating Eq. 17 with respect to dose at ID = ID_m. Then ID_m, given in Eq. 18, is substituted into the result. The output-voltage dose sensitivity is:

$$(30) \quad VO_{Dm} = \partial VO/\partial D|_{Tm} = VT_D - VT_T \cdot \beta_D/\beta_{Tm}$$

A value for VO_{Dm} = -2.59 mV/krad(Si) was calculated using the values listed in Tables 2 and 3. This result is considerably larger than VT_D = -1.67 mV/krad(Si).

The output voltage for the four p-FET samples is shown in Fig. 13. This plot was obtained from data sets like those shown in Fig. 8 where the VO values were obtained at ID_m. The data shows a nearly linear rise in VO with dose and a slight annealing effect.

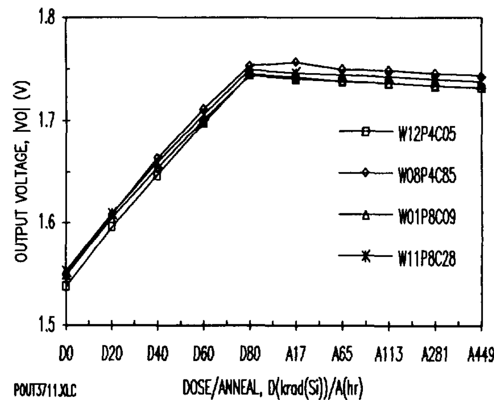

Figure 13. Four 1.2-μm CMOS p-FET output voltage dose/anneal responses determined at the current, ID_m.

The similarity of the data is remarkable considering the p-FET samples came from different wafers from the same run. This means that the sample set can be assumed to be uniform and that the results can be used to calibrate the flight parts which, of course, can not be irradiated on the ground.

For the circuitry shown in Fig. 3, which uses an 8-bit ADC to span 100 krad(Si), the resolution is 100k/256 = 390 rad(Si)/bit. This means that the p-FET dosimeter can easily resolve a dose of 1 krad(Si).

9. CONCLUSION

The use of on-chip p-FET dosimeters has been established and provides a radiation sensitivity of -2.6 mV/krad(Si) for the 1.2-μm CMOS used in this study. The temperature dependence is less than ±63 μV/°C over a temperature range of 70°C centered about the p-FET temperature independent point. At this point, the pre-irradiation output voltage was determined to be about -1.5 V and this value is design independent. The use of on-chip p-FETs provides a direct measure of the radiation dose experienced by the associated CMOS IC.

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