Programmable 1 V DC Voltage Standard

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***Abstract*— We have developed a Josephson voltage standard that produces intrinsically stable voltages that are programmable from −1.1 to +1.1 V. The standard uses a binary array sequence of 32 768 SNS (superconductor-normal-superconductor) Josephson junctions. The output can source or sink up to 2 mA and thus has high noise immunity.**

***Index Terms*— Josephson junctions, Josephson voltage standard, voltage measurement.**

I. Introduction

THIS paper describes a new Josephson voltage standard (JVS) in which the output voltage $V = Nf/K_{J-90}$ is defined by digitally programming the step number N. In this programmable JVS, an array of nonhysteretic junctions is divided into a binary sequence as shown in Fig. 1. The microwave excitation for each junction is set to equalize the amplitude of the $n = 0$ and $n = 1$ steps as shown in the inset. Each segment of the array can be set to the $n = -1$, 0, or $+1$ steps by applying bias current ($-I_s$, 0, $+I_s$) at the appropriate nodes. The combined step number N for the whole array can thus be set to integer values between $-M$ and $+M$, where M is the total number of junctions in the array [1], [2].

The rapid settling time, inherent step stability, and large operating current margins of the JVS in Fig. 1 make it superior to a conventional JVS for many dc measurements. (We define a dc measurement to be one in which the transient associated with changing N can be excluded from the measurement.) This improved performance is made possible by a new integrated circuit technology using intrinsically shunted SNS (superconductor-normal-superconductor) Josephson junctions. These junctions operate at lower excitation frequencies (10–20 GHz) than a conventional JVS and have 100 times larger step amplitudes (2–4 mA) [3].

The new JVS chip contains 32 768 Josephson junctions that are distributed such that the device functions as a 9-bit (including sign) digital-to-analog converter (DAC) [4]. The microwave drive is split eight ways and delivered to eight array segments of 4096 junctions each. The first segment is further divided into arrays of 128, 128, 256, 512, 1024, and 2048 junctions. Limiting the largest segment to 4096 junctions allows the bias currents to compensate for critical current variations between individual 4096 junction segments. Chips with one or more defective segments can be operated at reduced voltages. The microwave drive frequency is near 16 GHz, which makes the voltage generated by each junction

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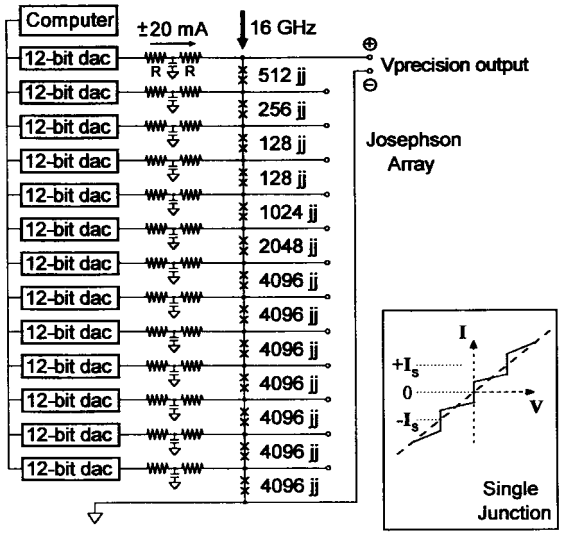

Fig. 1. Bias schematic of the 1 V programmable JVS.

$V = f/K_{J-90} \approx 33\,\mu$V. The smallest cell in the device consists of 128 junctions, which makes the least-significant-bit (LSB) resolution about 4 mV. Better output resolution is obtained by adjusting the frequency f to cover the voltage range between LSB's. This allows the JVS to provide gap-free coverage of the voltage range from 50 mV to 1.1 V (and −50 mV to −1.1 V), where the voltage resolution is limited only by the resolution of the frequency source.

II. Bias Circuit Design

As shown in Fig. 1, each node of the Josephson array is connected to a 12-bit DAC voltage source. These voltages are converted to currents by the two series resistors in each RCR filter ($R = 100\ \Omega$, $C = 0.02\ \mu$F). The bias current to a typical array segment is about 15–20 mA. To set the Josephson array to any of its 511 quantized output levels, the computer calculates the voltage for each DAC output based on the bias current required by each array segment. The algorithm automatically accounts for the fact that each DAC output is a function of the voltage at the node of the series array to which it is connected. After the 13 DAC input buffers have been loaded by the computer, the DAC outputs are simultaneously updated with a common trigger signal. The Josephson chip settles to the new voltage within a few microseconds.

The computer controls the bias electronics through an ordinary PC parallel port. Programming the array to a new output level takes about 500 μs. To reduce the potential for ground loops and unwanted RFI coupling, the 12-bit DAC's are powered from rechargeable batteries and optically isolated from

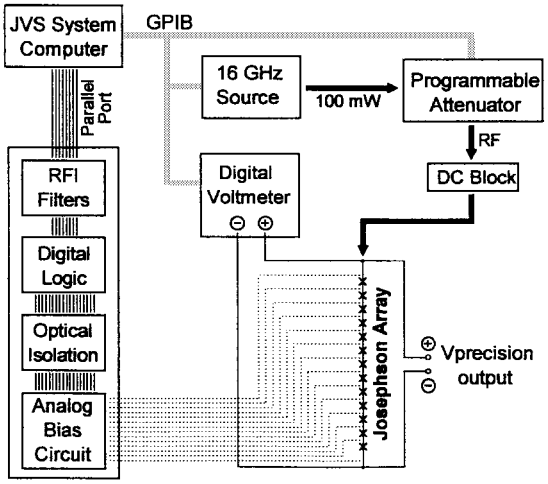

Fig. 2. Block diagram of the 1 V programmable JVS.

the digital logic. This allows the Josephson array to float with respect to ground, providing greater flexibility when the JVS is connected to other measurement systems. To prevent noise from the computer (10–50 MHz) and the environment from entering the bias electronics box and coupling to the Josephson array biases through the air, each signal wire from the parallel port passes through a 1 MHz low pass filter. The battery powered components typically require about 200 mA which allows the system to operate up to 24 h before recharging.

III. System Overview

Fig. 2 shows the overall configuration of the 1 V programmable JVS. The system computer controls the microwave frequency and power through GPIB connections to the 16 GHz source and the programmable attenuator. The output from the array is connected independently to both the precision output leads and the system digital voltmeter (DVM). This allows the system computer to continually monitor the array output with a resolution of a few microvolts (a few parts in 10^6 at 1 V).

Under control of the system computer, chip testing and diagnostic procedures are performed automatically. The individual I–V (current–voltage) curves of each array segment are measured to confirm functionality and to select the optimum bias points for the -1 and $+1$ steps. The chip operating margins for both dc bias currents and microwave power are measured, and the output voltage step flatness is verified over the full step height with submicro-ohm resolution. The term "step flatness" is used to describe the regions in the I–V curve where the output voltage is independent of changes in bias current (over a ± 1 to ± 2 mA range typically).

In order for the SNS programmable chips to be used in a voltage standard system, it is very important that the operating margins and step flatness be verified frequently (many times each day). Unlike conventional SIS voltage standards, it is possible for an SNS array to produce stable output voltages even when it is not on a constant voltage step. This can occur if the dc bias currents are incorrect, if the chip traps magnetic flux, or if the microwave frequency or power is changed without double-checking the bias operating range. The computer monitors the performance of the SNS array repeatedly between changes from one precision output level to another. A complete reoptimization of the chip's operating parameters at a given frequency and power takes about 10–15 min.

The programmable JVS uses several different methods to measure the step flatness of the output voltage from the Josephson chip. The fastest technique is to place all of the cells on the +1 step which results in an output voltage of 1.1 V. This voltage is measured by the system DVM while a dither current is applied (typically ± 1 mA) through the entire array. With 50 data points at the maximum resolution on the 1 V range, the DVM will resolve a voltage difference of 100 nV between the top and bottom of the Josephson step. This allows the system to resolve a resistance on the step as small as $R = 100$ nV/2 mA = 50 $\mu\Omega$ using this method. The JVS can verify the output step flatness at this level of precision in about 2 min, limited by the integration time required by the DVM.

The more precise method of measuring the output step flatness is to place half the cells on the $+1$ step, and half the cells on the -1 step. This makes the chip output voltage ideally 0 V, which allows the DVM to be used on its most sensitive range. Then we apply a dither current (± 1 mA) to one individual cell while measuring the output voltage of the entire array. In this configuration the DVM will resolve a voltage difference of 1 nV between the top and bottom of the Josephson step, which allows the system to resolve a resistance on the step as small as $R = 1$ nV/2 mA $= 0.5$ $\mu\Omega$. Since this procedure measures each cell individually, it takes about 20 min to complete. For metrology applications, the output voltage needs to be known at the level of parts in 10^9. The second method of measuring the step resistance is accurate enough to yield such an uncertainty. For example, if the programmable array will be operating over a range of output current $\Delta I = 2$ mA (i.e., ± 1 mA) and the step resistance has been measured to be $R = 0\,\Omega \pm 0.5\,\mu\Omega$, then the error in the output voltage will be $V_{error} = \Delta I \bullet R = 0$ V $\pm$ 1 nV which is ± 1 part in 10^9 at 1 V.

IV. Applications

The 1 V programmable JVS makes possible a number of dc measurements that take advantage of its rapid programmability, intrinsic output stability, and large operating margins (noise immunity). Some of these measurements have already been reported, including fast characterization of D/A and A/D converters, comparison against conventional SIS voltage standards, Zener reference calibrations using null voltages of 1 μV or less, etc., [2], [4].

The latest application of the 1 V programmable JVS is the watt balance experiment [5] which requires a stable, reversible voltage reference with high noise immunity. In the first mode of this experiment, a servo system controls the velocity of an induction coil moving in a magnetic field such that the voltage across the coil is equal to the 1 V reference from the JVS. In the second mode, the current in the induction coil is controlled in order to balance the gravitational force of a 1 kg mass. This current is precisely measured by passing it through a resistance standard and comparing the resulting voltage to the JVS with a null-meter. The new JVS operated successfully

as a direct reference in both modes of the experiment, thereby eliminating two voltage transfers and the associated noise and uncertainty contributions. These experiments show that the large step height and floating output of the Josephson array makes it ideal for use in an experiment of this complexity. A system dedicated to the NIST watt balance experiment is in the final stages of construction. A similar system is being developed for a comparable experiment at the Swiss Federal Office of Metrology [6].

Another experiment that combines the advantages of fast switching and stable output voltage of the programmable JVS is the precise characterization of capacitors used in electron counting experiments. When a nearly perfect step function generated by a Josephson array is applied to the capacitor, measurement of the charging current yields information on the low-frequency dependence of the capacitance.

The programmable JVS can also provide both the dc and ac inputs for the fast reversed dc (FRDC) method of measuring the thermoelectric transfer difference of thermal voltage converters (TVC). The first use in this application yielded a type A uncertainty of 0.13×10^{-6} in the measurement of the thermoelectric transfer difference of a single-junction TVC and a multijunction TVC [7].

The programmable JVS has also been proposed for use as the voltage leg in a metrology triangle experiment. This application would utilize a special, low voltage, high-resolution version of the device.

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Charles J. Burroughs, Jr., for a photograph and biography, see this issue, p. 269.

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