A High-Current Very Wide-Band Transconductance Amplifier

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Abstract—A new design approach for a high-current, very wide-band transconductance amplifier is described. The approach is based on paralleling the input and output of complementary unipolar current-mirror cells. Each cell has a fixed current gain determined by the ratio of two resistors. A differential input voltage-to-current circuit drives the cell array. The design has the advantage of avoiding the need for a single low-resistance current-sensing resistor and the attendant problems inherent in such resistors. Although the concept is still under development, a prototype of the cell-based transconductance amplifier was implemented with ten positive and ten negative current cells to gain some experimental familiarity with the approach in addition to providing verification of computer simulation results. The prototype transconductance amplifier is dc coupled, has a 3-dB bandwidth of about 750 kHz, and can deliver up to 35-A rms at 100 kHz with an output compliance voltage of 5-V rms. Other important characteristics such as output-load regulation and dc offsets are discussed.

I. INTRODUCTION

A TRANSCONDUCTANCE amplifier is an important component that is used in a variety of calibration activities requiring a known stable source of current. Such an amplifier ideally produces a current in a load proportional to an input voltage and maintains that current independent of the load impedance. The increasing requests of the National Institute of Standards and Technology (NIST) to provide calibrations of current transformers, meters, and shunts at current levels up to and even exceeding 20-A rms at 100 kHz have provided the impetus to develop a high-current, very wide-band transconductance amplifier. Although commercial transconductance amplifiers exist, which can deliver currents well in excess of 20 A, they fail to provide such levels of current above just a few kilohertz. The transconductance amplifier design being developed at NIST and described in this paper overcomes the present current/frequency limitation and will allow current calibrations to be made over a much broader range.

A number of authors have described a variety of fixed and controlled current sources implemented by combinations of monolithic and discrete components [1]-[5]. Almost all current sources or transconductance amplifier designs rely on a single current shunt to provide a voltage proportional to current which is used as feedback to com-

pare it with an input voltage. The shunt must be properly designed to provide a voltage drop across it that is a true measure of the current through it over a wide-frequency range with minimum phase shift. At low currents, rather ordinary commercial metal film resistors serve well. However, practical considerations dictate a low-value resistance shunt for high currents. Typically, a resistance of about 5–10 mΩ is used for current levels in the 20-A range. Low-value shunt resistors of this order must be of special design to minimize resistance, deviation of resistance with frequency, and temperature coefficient of resistance. Although good low-value shunt resistors are achievable, they are often proprietary items and expensive because of the special design necessary. The cell-based amplifier described below essentially overcomes the problem of requiring a single low-valued, high-quality shunt by utilizing the inherent tendency for paralleled current sources to add currents so that the sum is independent of frequency.

II. APPROACH

The approach described here is a modification of the basic idea of using complementary current-sources or current-mirrors with an operational amplifier to obtain a bipolar voltage-controlled current source [6], [7]. A simplified diagram of the cell-based approach of the transconductance amplifier is shown in Fig. 1. A total of ten positive and ten negative current-mirror cells each contribute to provide the total bipolar current at the output. This configuration has several advantages. The controlling device within each cell operates at one tenth the maximum peak output current rather than having a single stage power circuit to control the full output current. The total power is, therefore, dissipated evenly among the cells, allowing easier thermal management. Also, sharing the current by a number of cells has the main advantage of not requiring a single low-resistance shunt in the output circuit to sense the current. Finally, the bandwidth of the system is independent of the number of paralleled cells.

A differential voltage-to-current circuit converts an input voltage to a current which is polarity separated and steered to each cell array. The converter also provides an appropriate low-level of equal input currents to each polarity array at zero input voltage in order to maintain a quiescent operating current in each cell. Biasing each cell with a small quiescent current is usually done for Class *B*
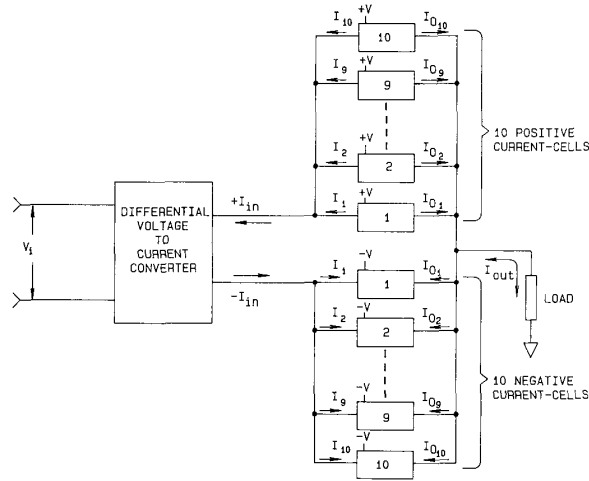
Fig. 1. Block diagram of the transconductance amplifier utilizing paralleled current-mirror cells.
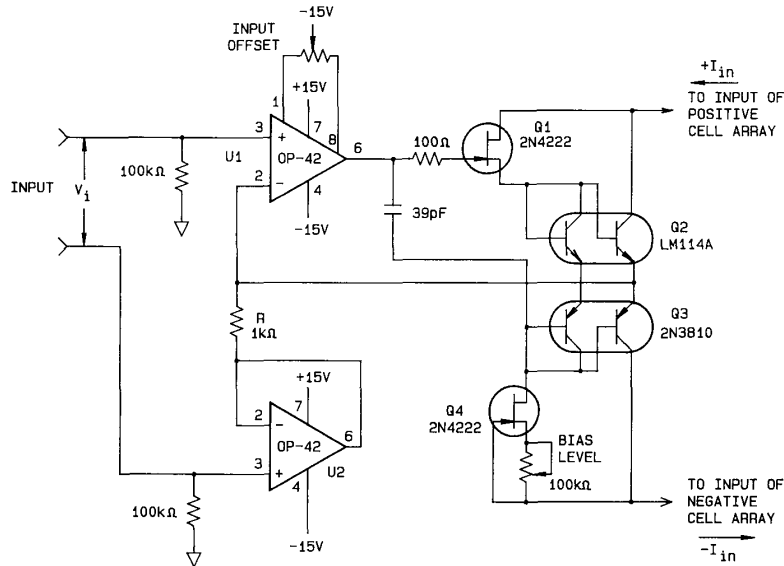

Fig. 2. Schematic detail of the differential voltage-to-current converter.

stages as a means to avoid the nonlinearities and attendant crossover distortion when the input signal passes through zero.

A general expression for the total output current of either polarity array where I_n is the input current to the nth cell and K_n is the current gain of the nth cell is

$$I_{out} = \sum_{n=1}^{10} I_n K_n. \qquad (1)$$

If all cells have an equal current gain of K, regardless of whether the input current divides equally into each cell, then the overall current gain reduces to

$$I_{out}/I_{in} = K. \qquad (2)$$

Thus the overall current gain is independent of the number of cells but the maximum output current is n times the maximum current capability of a single cell.

Fig. 2 shows the circuit detail of the differential voltage-to-current converter. Operation of the circuit is as follows: the two operational amplifiers, $U1$ and $U2$ are each connected as unity-gain amplifiers. Thus a voltage V_i, applied at the input terminals is forced across resistor R, resulting in a current equal to V_i/R. Depending on the polarity of the input voltage, the current through R is steered by $Q2$ and $Q3$ either to the negative cell or out of the positive-cell array input. $Q4$ serves as a dc current source to provide a fixed level of equal quiescent current for each cell array. An important feature of this design is

the differential input circuit which effectively separates the voltage input terminal from the common side of the output load-current terminal. This feature is essential for interrupting possible ground loops when dealing with high output currents at high frequencies.

The gain of the entire transconductance amplifier is the transconductance gain of the Fig. 2 circuit ($1/R$) times the fixed current gain of the cell array (K) or

$$I_{\text{out}}/V_i = (1/R)K. \tag{3}$$

Note that the gain of the transconductance amplifier can be conveniently changed by varying R. Also, the overall frequency response will not be affected by changing R, provided the voltage swing across R is not limited by the slew rate of the circuit.

The performance of the transconductance amplifier is, of course, very dependent on the design of the current-mirror cell. Current gain, frequency response, offset currents, and equivalent output impedance are the important characteristics that must be considered and traded off in a cell design. Fig. 3 shows the basic version of a positive current-mirror cell used in the prototype amplifier. The negative cell has the same topography but uses complementary devices and reversed power supply voltage polarities. Operation of the current-mirror cell is as follows: an input current I_{in} causes a voltage drop across $R2$, which in turn causes the operational amplifier to turn on the power MOSFET, $Q1$. Output current I_{out} through $R1$ is regulated when the voltage drop across $R1$ equals the drop across $R2$. $Q1$ was selected for a 7-A maximum continuous drain current rating. Transistor $Q2$ serves as a buffer for $U1$ in order to supply the current necessary to drive the large interelectrode capacitances associated with $Q1$. The transformer in the source circuit provides stability and is designed to set the upper cutoff frequency of the cell's current gain. Output compliance voltage is determined primarily by the supply voltage at the $R1$–$R2$ node minus the voltage drop across $Q1$.

An expression for the current gain of the current-mirror cell, assuming the forward transconductance of $Q1$ is constant and neglecting device capacitances, is shown in the equation as

$$I_0/I_i = \frac{R2}{(R1 + j\omega M) + (R1 + 1/G_{fs} + j\omega L1)/A_\omega} \tag{4}$$

where

$M = k(L1 \times L2)^{1/2}$,
A_ω open loop gain of $U1$,
G_{fs} forward transconductance of $Q1$,
k transformer coupling coefficient.

At low frequencies, the current gain reduces simply to $R2/R1 = K$. Thus for the values given in Fig. 3 the current gain is 10^4. At high frequencies, the first break in the
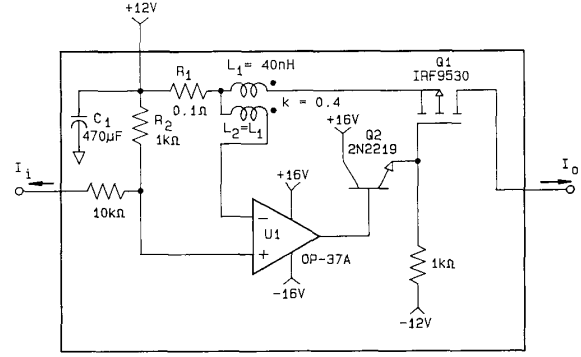

Fig. 3. Schematic diagram of a positive current-mirror cell.

frequency response occurs at $\omega = R1/M$, provided the second term in the denominator is small with respect to the first term by virtue of sufficient open-loop gain, A_ω. The values of the transformer parameters and $R1$ in Fig. 3 were designed to produce a -3-dB cutoff frequency of 1 MHz.

The equivalent output impedance, Z_0, of the current cell is approximated by [1]

$$Z_0 \simeq Z_{\text{ds}} G_{fs} R1 A_\omega \tag{5}$$

where Z_{ds} is the drain-to-source impedance of $Q1$. Equation (5) shows that the output impedance is boosted by the open-loop gain of the operational amplifier. This results in a very high output impedance. At low frequencies, the equivalent output impedance is in the range of several hundred megohms. Unfortunately, however, the output impedance decreases rapidly with increasing frequency due to the fall in amplifier open-loop gain and the decrease in Z_{ds}. The problem of trying to maintain a high output impedance is exacerbated by the voltage dependence of Z_{ds}. The drain-to-source capacitance increases rapidly with decreased drain-to-source voltage. Also, the output impedance of the transconductance amplifier will be proportionally reduced by the number of paralleled cells.

The output offset currents of the current cell are primarily determined by the offset voltage and input bias currents of the operational amplifier, $U1$. Gate current leakage of $Q1$ is also a factor but can be neglected. The OP-37A operational amplifier is one of the keys to this design approach because of its wide bandwidth and precision dc characteristics. Typically, the input bias current of the OP-37A amplifier will contribute about ± 200 μA to the cell's output offset-current and an additional ± 300 μA due to input voltage offsets. More important, though, is the total offset drift with time and temperature, since any initial offset can be balanced out. Input bias current drift of the OP-37A with temperature is negligible and input-voltage offset drift will result in a maximum output-current drift of about ± 10 μA/°C per cell.

A few words are in order to point out some of the practicalities involved with the components and layout of the current-mirror cell circuit shown in Fig. 3. Resistor $R1$ is made up by paralleling ten 1-Ω, 1/3-W, metal film resistors. Resistor $R2$ is also of the same type as $R1$ so that, ideally, if their temperature coefficient of resistance of each are equal, then the current gain of the cell becomes independent of temperature. The parameters of the transformer are easily implemented as an air-core transformer on a printed circuit board by setting the length, trace width, and spacing of two parallel conductors to obtain the desired mutual inductance. The bypass capacitor $C1$ for the positive supply voltage is essential to hold the node potential at $R1$ and $R2$ constant. In practice, the ground return end of the capacitor should be magnetically coupled to the output current lead. Twisting the output and return leads tightly together and terminating them at the output terminal, effectively reduces the size of the loop area formed by the interconnection of the cell outputs. The result is a lower inductance between each cell's output and the output terminal of the transconductance amplifier. It is important that the inductance of the cables which parallel the cell outputs be equal in order to avoid circulating currents between the cells. Triaxial cable can also be used effectively to reduce wiring inductance from each cell to the output terminal by employing the inner and outer shields for the output and return conductors of each cell.

III. SIMULATION RESULTS

Analog simulation was used at various times during the development process as a tool to gain a better understanding of circuit operation and to rapidly sort out the causes of anomalies observed in circuit breadboards. The simulations were performed on a commercial analog simulation system that uses "SPICE PLUS" as the general-purpose circuit simulation program, together with a large library of models which emulate commercially available devices.

Fig. 4 shows the output current time-domain simulation for the single cell of Fig. 3 (lower trace) and ten identical cells connected in parallel (upper trace). The single-cell waveform has a peak-to-peak output of 3 A and the ten-cell waveform has 30-A peak-to-peak output. Note that the transition times, about 350 ns, are virtually identical, indicating that cell paralleling does not affect bandwidth. Because the current gain of the cell is 10^4, only 3 mA is required at the input of the ten-cell array to obtain a 30-A output.

Fig. 5 shows a plot of the equivalent output impedance as a function of frequency of a single current-source cell. The plot was generated from simulation in the frequency domain by applying a test voltage source at the output terminal and measuring the ratio of the applied test voltage to the resulting current. The vertical scale is presented in decibels in order to show the decrease in impedance over a wide range of frequency. At 1 Hz, the impedance
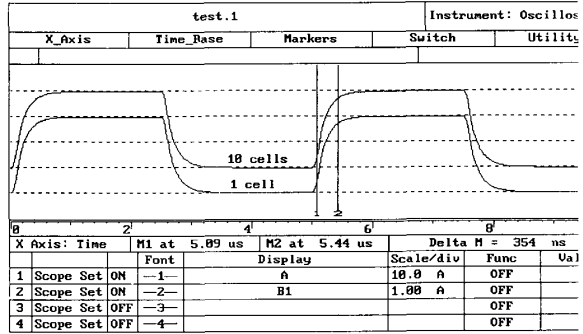

Fig. 4. Simulated time-domain current waveforms of a single cell and ten cells connected in parallel.
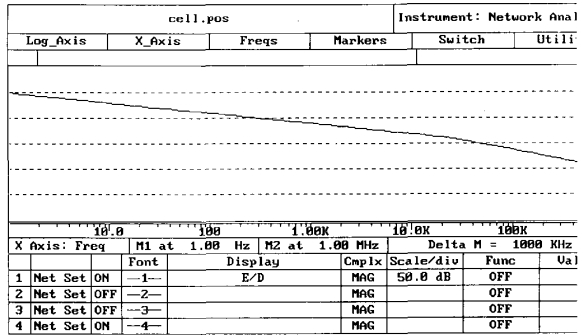

Fig. 5. Simulated equivalent output impedance of a cell as a function of frequency.

is about 10^8 Ω. At 50 kHz, the impedance drops about 100 dB, resulting in a value of about 1 kΩ.

IV. PERFORMANCE

A prototype transconductance amplifier was fabricated with ten positive and ten negative current cells of the design given in Fig. 3 and the differential voltage-to-current converter shown in Fig. 2. Some of the measured performance characteristics of the transconductance amplifier are listed below:

1) gain: 0.5–10 s, 5 ranges;
2) gain temperature coefficient: -25 ppm/$^\circ$C;
3) frequency response: dc to 100 kHz (-0.5 percent), 750 kHz (-3 dB), at 20-A rms;
4) maximum output: 35-A rms at 100 kHz;
5) compliance voltage: 5-V rms at 20 A;
6) output impedance: 10 kΩ at 2 kHz;
7) output offset current: ±100 μA;
8) total harmonic distortion: -40 dB.

The measured performance results deviate somewhat from the simulation results previously presented for two reasons. First, the mutual inductance of the transformer in each cell turned out to be about 25 percent higher than planned for, resulting in a slightly lower 3-dB cutoff fre-

quency than indicated by simulation. Second, it was found that for large inductive loads a small amount of negative feedback across each cell array (< 10 pF) was required to stabilize the system. The effect of this feedback causes a substantial lowering of the equivalent output impedance, especially at high frequencies. This effect has been substantiated later by simulation which shows that without feedback the real part of the output impedance has a negative component within part of the operating frequency band.

The maximum output current of 35 A at 100 kHz indicated in the list of performance characteristics is only due to a compliance voltage limitation in the differential voltage-to-current circuit and the current capability of the power supplies. The amplifier is capable of at least 50-A rms output before reaching the thermal limitations of the cells.

Total harmonic distortion is an especially important measure of performance for this design. Since each complimentary set of current cells is not within a common feedback loop, small differences in response between the two halves, will contribute to harmonic distortion. Table I shows the total harmonic distortion at the 5- and 20-A rms output-current levels over a frequency range from 50 Hz to 100 kHz. Distortion drops to about −40 dB at 100 kHz at 20-A rms.

Fig. 6 shows the pulse response of the transconductance amplifier output-current superimposed on the output terminal voltage waveform. Measurements were made with a wide-band current transformer that has a sensitivity of 0.1 V/A. The peak output current is 30 A with rise and fall times of about 500 ns. The narrow 3-V peak voltage-pulses at the current transitions reflects the voltage required to overcome the parasitic inductance (about 50 nH) in the output load measuring circuit. Note that even a small amount of inductance in the output circuit requires 3 V of compliance from the amplifier.

The equivalent output impedance of the transconductance amplifier determines the load current regulation. The equivalent output impedance can be determined by measuring the change in output current for a known change in load impedance. Table II shows the change in the magnitude of current and phase caused by a load change of 0.2 Ω at 5-A rms. The last column in the table shows the calculated equivalent output impedance. Measurements were made with a two-channel programmable source, a two-phase vector/lock-in amplifier, and a wide-band current transformer. Resolution limits prevented measurement of current changes below 1 kHz and data were limited to 20 kHz by the programmable source. Note that the output impedance falls off rapidly with frequency to about 250 Ω at 20 kHz. The low output impedance at higher frequencies is a result of the negative feedback that had to be added to make the amplifier unconditionally stable for all loads. Further work on improving the design of the basic cell suggests that the problem of conditional stabil-
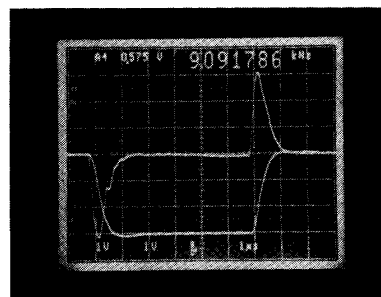

Fig. 6. Pulse response of the transconductance amplifier.

TABLE I
TOTAL HARMONIC DISTORTION

Frequency Hz	Distortion @5A rms dB	Distortion @20 A rms dB
50	-55	-59
100	-59	-64
1 k	-59	-71
2 k	-59	-69
5 k	-59	-66
10 k	-58	-61
20 k	-56	-53
50 k	-47	-44
100 k	-42	-40

TABLE II
LOAD REGULATION VERSUS FREQUENCY

Frequency Hz	Current change ppm	Phase change μRad	Output imped. Ω
50	0	31	--
400	0	237	--
1 k	-5	602	40000
2 k	-22	1192	9090
8 k	-97	4847	2061
10 k	-156	6355	1282
14 k	-324	8290	617
16 k	-610	9577	327
20 k	-793	11800	252

ity due to a negative real output impedance can be overcome without reducing the output impedance as much at higher frequencies.

V. CONCLUSIONS

A high-current, very wide-band transconductance amplifier has been described. The approach is based on paralleling the input and output of complementary unipolar current-mirror cells. The cell approach has the advantage of avoiding the need for a single low-resistance current shunt and the attendant problems inherent in such resistors. It was shown that the bandwidth of the system is independent of the number of current cells. Test results of a prototype transconductance amplifier indicate that a bandwidth of 750 kHz and output currents up to 35-A rms at 100 kHz can be achieved in practice. Although the

equivalent output impedance of the amplifier at higher frequencies is lower than desired, further work suggests that improvements can be made in this area.

ACKNOWLEDGMENT

REFERENCES

[1] J. G. Graeme, *Applications of Operational Amplifiers—Third Generation Techniques.* New York: McGraw-Hill, 1973, pp. 78–94.

[2] J. Williams, "Current-source alternatives increase design flexibility," *Electrical Design News,* pp. 169–174, Sept. 1, 1982.

[3] R. A. Pease, "Improve circuit performance with a 1-op-amp current pump," *Electrical Design News,* pp. 85–90, Jan. 20, 1983.

[4] O. B. Laug, "A wide-band transconductance amplifier for current calibrations," *IEEE Trans. Instrum. Meas.,* vol. IM-34, pp. 639–643, Dec. 1985.

[5] D. Patranabis, S. Ghosh, S. Bandyopadhyay, and S. Sarkar, "New improved bipolar and bilateral voltage to current converters," *IEEE Trans. Instrum. Meas.,* vol. 37, pp. 58–61, Mar. 1988.

[6] J. W. Haslett and M. K. N. Rao, "A precision controlled current source," *IEEE Trans. Instrum. Meas.,* vol. IM-29, pp. 212–213, Sept. 1980.

[7] D. Baert, H. Simoens, and H. Kuyken, "Precision voltage to single-ended current source sidesteps CMRR problems," *Electron. Design,* p. 320, June 14, 1984.