Lateral Distribution of Hot-Carrier-Induced Interface Traps in MOSFET's

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***Abstract*—The spatial profiles of hot-carrier-induced interface traps in MOSFET's with abrupt arsenic junctions and oxide thicknesses of 10–38 nm are determined using change pumping both in the conventional manner and with a modified "constant field" approach. For the thinnest oxides we find the damage to be highly localized in a very sharp peak that is located inside the drain at the point of maximum lateral electric field. In thicker oxides, the damage peak is broader and is shifted toward the edge of the drain junction. Two-dimensional device simulations using the measured profiles are in qualitative agreement with measured *I–V* characteristics after degradation. However, the magnitude of the predicted degradation is underestimated, suggesting that significant electron trapping occurs also.**

I. Introduction

It is well known that in small-geometry MOSFET's, carriers from the channel can be injected into the gate oxide. This "hot-carrier" injection phenomenon constitutes a threat to the long-term reliability of such devices in that the injected carriers may lead to both electron trapping in the oxide and formation of interface traps (D_{it}) at the Si–SiO_2 interface [1]–[4]. In this work, as part of a broader investigation into the causes and effects of hot-carrier injection, we report on the location of the generated D_{it} and its electrical effects with greater precision than done heretofore.

A primary difficulty in understanding hot-carrier injection is its highly localized character. The injection is brought about by high electric fields in the channel giving carriers sufficient energy to surmount the conduction and/or valence band discontinuities at the Si–SiO_2 interface. These large electric fields are strongly localized near or in the drain, and hence the carrier injection and D_{it} creation are similarly concentrated. This strongly inhomogeneous character of the hot-carrier injection and resultant damage presents a considerable challenge to both experimental and modeling efforts.

One well-known experimental approach for assessing the D_{it} created by hot-carrier stressing is the charge-pumping technique [5]. Using this technique, it has been possible to measure the spatial variation of hot-carrier-induced N_{it} (interface traps per square centimeter) near the drain in small-geometry transistors [6]–[8]. In this work, we perform similar spatial profiling experiments, either in the conventional manner or with a special modification to eliminate certain undesirable electric field effects (discussed more fully below). We find that, in devices with very thin gate oxides (10 mm), the peak is very narrow being concentrated over 10–15 nm. This peak is considerably narrower than those observed previously [6]–[8] and is found to be well correlated with the location of peak lateral electric field. Interestingly, in thicker oxide devices the damage peak broadens and its correlation with the field maximum is lost.

A number of papers have appeared recently [9]–[11] in which efforts were made to numerically simulate the effects of hot-carrier damage on MOSFET *I–V* characteristics. Here, we perform simulations also. Our calculations differ from the previous work in that *we do not assume the D_{it} profile*. Rather, we employ the results of spatial profiling measurements on particular stressed devices. We can then make *predictions* of the post-degradation *I–V* characteristics of these devices, which may in turn be compared with actual measurements. In general, the results of these comparisons indicate that the measured D_{it} profiles are insufficient to explain the observed degradation. From this we tentatively conclude that hot-carrier stress must also induce trapped oxide charge (which charge-pumping is not sensitive to) and that this too is important in explaining the observed *I–V* degradation. Unfortunately, we know of no technique for verifying this conclusion by experimentally measuring the profile of the trapped oxide charge.

II. Experimental Methods

The devices used were NMOS transistors fabricated at the NRL. The devices had shallow arsenic junctions (0.2 μm, no LDD), phosphorus-doped polysilicon gates, threshold adjust and anti-punchthrough implants, and oxide thicknesses in the range of 10–38 nm. Some devices having deep phosphorus junctions were also processed for comparison. Effective channel lengths (determined electrically) were in the range of 1–1.3 μm with gate widths of 15 μm. The doping concentration at the surface of the channel was estimated to be $N_A = 2.4 \times 10^{16}/cm^3$ from SUPREM simulations. A device cross section appears in Fig. 1.

Charge-pumping experiments to determine the spatial

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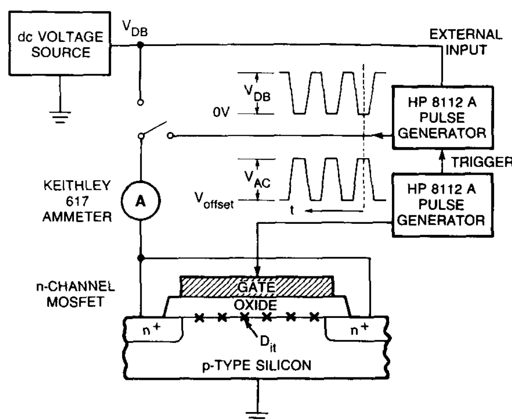

Fig. 1. Device cross section and schematic of the charge-profiling measurement setup. The switch located above the ammeter selects between the "standard" (switch vertical) and "constant field" (switch horizontal) profiling techniques.

profile of N_{it} in these devices were performed in two ways. These are shown schematically in Fig. 1 with the profiling method being selected by the position of the switch located just above the ammeter. The first method (with the switch vertical), which we will refer to as the "standard" profiling technique, is essentially method II of [8]. The second method (with the switch horizontal) represents a modification of the standard technique and will be termed the "constant field" profiling technique. The basic principle of both techniques is to use charge-pumping (explained below) to detect the integrated amount of interface traps while varying the size of the region from which interface traps can contribute by modulating the source–drain depletion widths. From such information (plus the assertion that all the hot-carrier damage occurs near the drain), the spatial profile of D_{it} can be inferred.

In brief, the charge-pumping technique works as follows ([5] should be consulted for a detailed discussion). The gate of the NMOS device under test is biased with a dc offset voltage (V_{offset}) plus an ac signal (V_{ac}) that in our experiments was a 1-MHz square wave, typically 6–12 V in amplitude with a rise/fall time of 0.2 μs. This biasing causes the surface to alternately accumulate (with holes) or invert (with electrons) in synchrony with the ac signal. The dc current collected at the source and drain as a function of V_{offset} is the raw output and is called the charge-pumping current I_{cp} (e.g., see Fig. 3). The primary source of I_{cp} is recombination of electrons, trapped by interface traps when the surface is inverted (filling step), with holes, which enter when the surface switches to accumulation (emptying step). Given this interpretation, values for N_{it} can readily be deduced from the measured I_{cp}. These values of N_{it} are averages of D_{it} over energy and over the area of the channel (length × width).

In order to find the spatial variation of N_{it} in the vicinity of the drain, in the standard technique dc biases V_{db} are applied to both the source and drain. The range of V_{db} values used by us was typically from −0.1 to 5 V. As the junctions become more strongly reverse biased, more interface traps (assumed to be produced by hot-carrier stressing near the drain only) are prevented from contributing to I_{cp} by the growing depletion layers. Thus, from the dependence of I_{cp} on V_{db} (e.g., see Fig. 4), the variation of N_{it} with position near the drain can be deduced. For these positions to be accurate, it is essential that the locations of the source–drain depletion layer edges be determined by 2-D numerical simulation as was pointed out in [8]. Ideally, these edges are defined as the locations at which the surface free-carrier density (holes) is just sufficient to allow all the interface trapped electrons to recombine. For our work, we have usually assumed this density to be 1×10^{12} holes/cm^2; variations of this choice do not affect our conclusions significantly.

The constant field profiling method is identical to the standard method except that the bias applied to the source and drain is an ac signal. The reason for this modification can be understood as follows. In the standard profiling technique, when the gate is biased into inversion, the source and drain are electrically connected and the channel potential becomes equal to V_{db}. This implies that the electric field at the Si–SiO_2 interface during the part of the cycle when the interface traps fill (inversion) varies with V_{db}. Because this electric field can affect the occupancy of the interface traps [12], [13], its variation with V_{db} can (and does) lead to spurious results. However, this problem can be circumvented because V_{db} serves a role in profiling only during the accumulation part of the cycle when it defines the source–drain depletion widths. When the surface is inverted, V_{db} can take any value; in particular, it can be held constant thereby keeping the surface electric field constant during filling. Thus, for the constant field (during filling) method, an ac signal of amplitude V_{db} (on a baseline of 0 V) and 180° out of phase with the gate ac signal is applied to source and drain (Fig. 1, switch horizontal).

In a typical experiment, pre-stress characteristics were first established for each device. This consisted of measurements of the current–voltage characteristics of the device plus a determination of the (uniform) spatial profile of N_{it} using either or both of the above-described profiling techniques. The device was then repeatedly stressed and, following each stress, recharacterized. As is often done, the stresses were performed under biases well above normal operating voltages (typically V_d = 6–8 V) in order to accelerate the rate of degradation. Numerous such experiments (many not discussed here) were performed on over 40 devices under a variety of conditions both as self-consistency checks on the results, e.g., varying the amplitude and frequency of V_{ac}, and for exploring how various parameters, e.g., oxide thickness, stress conditions, and temperature, affect the damage.

III. Experimental Results

Typical I_{ds}–V_g characteristics with V_d = 50 mV for a hot-carrier degraded MOSFET are shown in Fig. 2 with the duration of the stress as a parameter. The device had

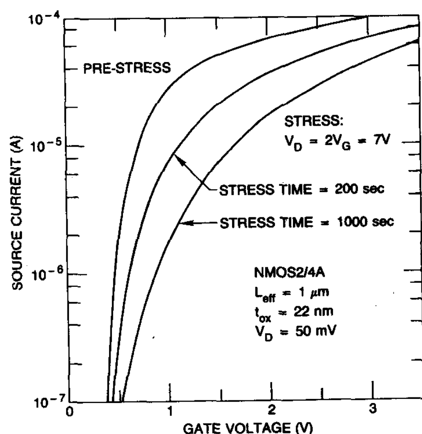

Fig. 2. Source current as a function of gate voltage with V_d = 50 mV for a MOSFET with t_{ox} = 22 nm and L_{eff} = 1 μm and with stress time as a parameter. The degradation in the *I–V* characteristics as a result of hot-carrier stressing is evident.

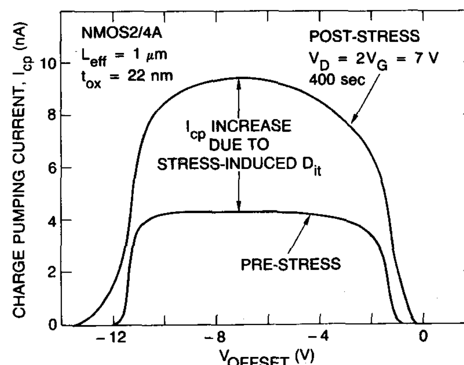

Fig. 3. Charge-pumping current I_{cp} (measured with V_{ac} = 12 V) as a function of V_{offset} for a MOSFET with L_{eff} = 1 μm and t_{ox} = 22 nm. The increase in I_{cp} following the stress results from interface traps generated by hot-carrier injection.

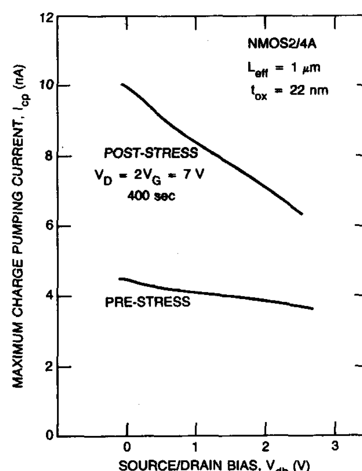

Fig. 4. Maximum charge-pumping current versus the reverse bias V_{db} applied to source and drain (with respect to substrate) for the same sample as in Fig. 3. By converting V_{db} into the corresponding depetion layer edge location and differentiating the data, the N_{it} spatial profile is obtained.

an L_{eff} of 1 μm and t_{ox} = 22 nm and the stresses were done at 295 K with V_{ds} = 7 V and V_g = 3.5 V for times of 200 and 1000 s.

The raw charge-pumping data for a similar sample both before and after a 400-s stress are shown in Fig. 3. The curves are "rectangular" in shape because charge pumping current can flow through the interface traps only when V_{offset} is such that *both* holes (accumulation) and electrons (inversion) reach the surface in response to V_{ac}. The magnitude of the I_{cp} signal is a measure of N_{it}, and the large increase in I_{cp} seen post-stress is entirely due to hot-carrier-induced D_{it}. (The increased rounding of the post-stress curve is due to the spatial inhomogeneity of the damage). In Fig. 4 we show the maxima of a sequence of such I_{cp} curves for a single MOSFET (both pre- and post-stress) plotted as a function of the dc source–drain reverse bias V_{db}. I_{cp} (max) drops with increasing V_{db} since this causes the size of the source–drain depletion widths to increase thereby excluding more interface traps from contributing. That the slope of I_{cp} versus V_{db} is much larger after stress shows that much of the damage does indeed lie in the depletion region and can be profiled. However, at large V_{db}, the post-stress I_{cp} does not match the pre-stress value indicating that there is damage that lies beyond (or outside) the profiling region as well. As noted previously, V_{db} is converted to position information by computing the depletion layer edge locations and the N_{it} profile is then obtained by taking the spatial derivative of I_{cp} (max).

A typical spatial profile of the hot-carrier-induced interface trap density deduced from data like that of Fig. 4 is shown in Fig. 5. These data are for a sample with L_{eff} = 1 μm and t_{ox} = 10 nm and is the damage resulting from 40 s of stress. The profile was determined using the standard profiling technique. Also depicted in Fig. 5 are the variation with position of the lateral electric field at the surface and an indication of the drain doping profile. The latter is derived from a SIMS profile of the junction and an assumed lateral diffusion ratio of 0.7. The N_{it} profile shows a sharp peak with a full width at half-maximum (FWHM) of roughly 10 nm, located 25 nm inside the metallurgical junction. The position of this peak is well-correlated with the location of the peak lateral field (within 5 nm).

In Fig. 6 we illustrate how the N_{it} profile (standard technique) of the device used for Fig. 5 varies with stress time. The magnitude of the damage increases with stress time, but the profiles remain qualitatively the same. The small peak in the pre-stress characteristic is an artifact of the standard technique as discussed below.

The dependence of the width and location of the damage peak on oxide thickness is examined in Fig. 7. We compare a normalized N_{it} profile for a thin gate oxide device (10 nm) with that found for a device with t_{ox} = 37.6 nm. Two aspects are noteworthy. First, the peak location shifts by roughly 20 nm from near the peak field point

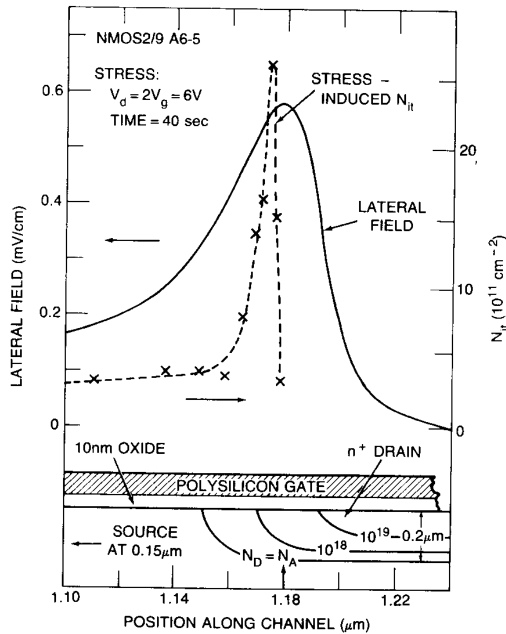

Fig. 5. Stress-induced N_{it} that results following 40 s of stress with $V_d = 2V_g = 6$ V plotted as a function of position along the channel. The very narrow damage profile is well correlated with the lateral (surface) electric field peak also shown.

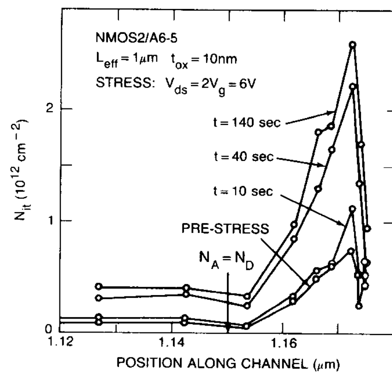

Fig. 6. Stress-induced N_{it} for the same sample as in Fig. 5 plotted as a function of channel location with stress time as a parameter. The pre-stress peak is spurious (see text).

(10-nm oxide device) to a point close to the metallurgical junction (37.6-nm oxide device). And second, the peak broadens in the thicker oxide sample to a FWHM of approximately 30 nm. Devices with 22-nm oxides were studied also (data not shown) and the results are consistent with these trends.

To investigate possible effects of the abruptness of the drain junction on the damage profile, we examined the extreme case of devices with nonabrupt phosphorus junctions. In Fig. 8, we show an N_{it} profile taken using the standard technique on a device similar to our other devices ($L_{\text{eff}} = 1.2$ μm, $t_{\text{ox}} = 22$ nm) but with deep phosphorus junctions ($x_j \approx 0.8$ μm from SUPREM simulations). The location and width of this peak are roughly

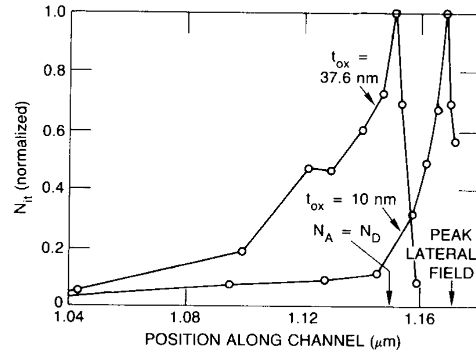

Fig. 7. Normalized N_{it} as a function of channel position for MOSFET's with oxides 10 and 37.6 nm thick. The peak N_{it} values were 3.28×10^{12}/cm^2 (10 nm) and 2.76×10^{12}/cm^2 (37.6 nm) and both devices were stressed with $V_d = 2V_g$. A dependence of both the location and spread of the stress-induced damage on oxide thickness is apparent.

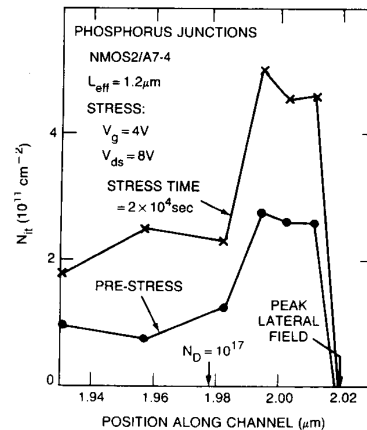

Fig. 8. Stress-induced N_{it} as a function of position along the channel for a device with phosphorus junctions. The metallurgical junction is located at 1.90 μm.

the same (somewhat larger in width) as those seen in the comparable arsenic-junction samples. (Note that, as with Fig. 6, the pre-stress peak in Fig. 8 is an artifact). From this we conclude that the junction width is relatively unimportant in determining the width and location of the damage peak.

Lastly, Poorter *et al.* [8] reported a considerable dependence of peak location on stress bias, i.e., as V_g was varied at constant V_{ds}. We did not investigate this question extensively; however, in the limited amount of data obtained, no consistent trends were observed. Qualitatively, results similar to those of Figs. 5–7 were obtained independent of stress bias; the only significant differences were in the well-known effects of biasing on the rate at which damage accumulates [2]–[4].

IV. Discussion of Experiments

A. N_{it} Profile

The most important results of this paper are those depicted in Figs. 5–7. As noted above, when the gate oxide of the MOSFET is very thin (10 nm) we find the damage

to be highly localized with an FWHM of about 10 nm (Figs. 5 and 6). This damage appears well correlated with the position of peak lateral electric field; its location is well inside the metallurgical junction (25 nm) and also far from the gate edge (125 nm). These results are direct evidence that, at least in very thin oxides, the injection of hot carriers and the resulting damage are strongly localized at the point where carrier heating is maximal. Apparently, little lateral motion of the hot carriers occurs inside the thin oxide.

As shown in Fig. 7, as oxide thickness increases from 10 to 37.6 nm, the width of the N_{it} peak increases (FWHM goes from 10 to 30 nm), and the peak location shifts toward the source by about 20 nm. These effects could arise from two possible mechanisms. First, the position of maximum injection may not be the point of peak electric field in samples with thicker oxides. And second, in a thicker oxide there is an increased possibility that lateral transport of hot carriers may occur within the oxide following injection causing the damage to shift and spread out. Finally, error and/or other limitations in the experimental data cannot be discounted as an explanation. These possibilities are discussed in the following three paragraphs.

The effect of oxide thickness on the lateral electric field at the surface during stress is examined in Fig. 9 using 2-D numerical simulation. Two curves are shown corresponding to the two devices of Fig. 7 that are identical except for their oxide thickness (10 and 37.6 nm) and stress conditions. The lateral field curves are nearly identical with the location of the peak lateral field having shifted by only about 7 nm. Therefore, *if* in thicker oxide devices the injection remains localized at the peak lateral field point, then the shift in injection point with oxide thickness is insufficient to account for the observed 20-nm shift in the damage peak.

The mechanism of in-oxide transport of injected hot carriers has been discussed previously by various authors (e.g., [3]). The main piece of evidence from our studies consistent with this mechanism is that the widths of the damge peaks are of the same order as the oxide thicknesses (Fig. 7). In addition, the shift in peak location is of roughly the same size as the change in oxide thickness. These are expected features of any in-oxide transport model since carriers transported longer distances would likely be lost to the gate or substrate rather than remaining in the oxide. Of course, for an in-oxide transport mechanism to be correct, it needs to involve a positively charged specie—either a hot hole or some other intermediate—because of the sign of the lateral field in the oxide.

The final possibility of error and/or other limitations of the data must be considered. The data of this paper are representative of experiments we have performed on over 40 devices and over a considerable range of experimental parameters. Generally, the results are repeatable and consistent. Moreover, our conclusions are largely independent of quantities that are not accurately known such as the location of the metallurgical junction. This is because

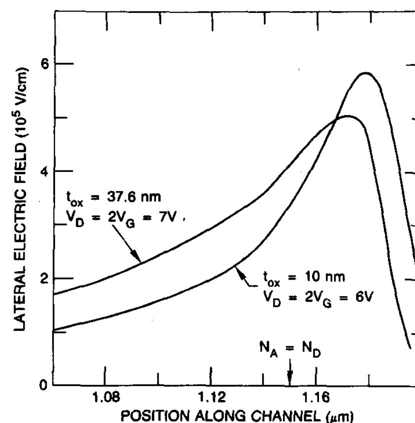

Fig. 9. Comparison of the lateral electric field at the surface as function of channel position for two devices with differing oxide thicknesses and bias conditions.

the locations of the damage peaks and lateral field maxima are determined *relative* to the junction edge. However, there are some significant error sources. For example, the assumption made in the profiling about the location of the depletion layer edge can lead to errors of as much as 5 nm in the locations of damage peaks. As a second example, the profile information furthest inside the drain is least reliable because these points require the junctions to be slightly forward biased and the small forward current adds to the charge-pumping current I_{cp}, obscuring the interface trap signal and leading to increased error (even though we attempt to correct for this by subtracting the pre-stress baseline). In general, we believe the various experimental and analysis errors alter only the *size* and precise *shape* of the damage profile and that the central fact of our data—the *existence* of a narrow peak in the N_{it} profile—is unaffected.

The damage profiles measured in this work differ somewhat from those reported by Poorter and Zoestbergen [8] for devices with $L_{\text{eff}} = 1.6$ μm and $t_{ox} = 50$ nm. In particular, their damage peaks (when they existed) were broader (FWHM ≈ 75 nm) and appeared to shift as a function of the gate bias used during the stress. The origin of these differences is not entirely clear; however, that their devices had thicker oxides and broader damage peaks is consistent with the trend in our data (Fig. 7). Moreover, it is plausible that thickened oxides could lead to dependences on stress biasing, e.g., by affecting the lateral motion of injected carriers. The locations of their damage peaks—between the maximum lateral field point and the metallurgical junction—were similar to ours; however, any quantitative comparison is unwarranted given the different devices involved and the spatial resolution required ($\leq$20 nm).

B. Pre-stress N_{it} Peak

As seen in Figs. 5–7 the spatial profile of the hot-carrier-induced N_{it} is sharply peaked. Unfortunately, as was noted earlier in relation to Fig. 6, a peak appears at this

same location in the *pre-stress* curve as well. This peak, while possibly real, is likely anomalous, and it therefore suggests the possibility of some unknown flaw in the spatial profiling technique. Such a flaw would obviously draw into question most of the conclusions of this paper.

We therefore conducted a number of experiments aimed at understanding the pre-stress peak, e.g., varying parameters in the charge-pumping measurement. We have concluded that the correct explanation involves an electric field effect on interface traps. The effect of an electric field on interface traps has been investigated in the past, and evidence for its significance has been presented [12], [13]. It is believed that these effects result from the electric field lowering interface trap barriers as in the Poole–Frenkel effect. In this way, an electric field can change the occupancy of the interface traps by modifying either their capture cross section or their location in energy (which could include the pulling of "new" traps out of the conduction and valence bands). Now, as pointed out earlier, when the standard profiling technique is used, the electric field at the Si–SiO_2 interface during filling (inversion) changes as the source–drain reverse-bias V_{db} and, hence, the channel potential are varied. Consequently, if the occupancy of interface traps is affected by the electric field, spurious variations in I_{cp} as a function of V_{db} and hence in N_{it} as a function of position will be observed. Since the field is largest when V_{db} is small and the electric field tends to enhance "filling" (lowers barriers), the spurious N_{it} will be largest when V_{db} is small. This is just what is observed with the pre-stress peak (although why a peak is observed rather than a monotonically increasing N_{it} is unclear). As a test of this explanation, we developed the constant field (during filling) profiling technique described earlier. A comparison between results obtained using this and the standard technique is shown in Fig. 10. It is seen that essentially the entire pre-stress peak vanishes when the constant field method is used.

How do electric field effects modify post-stress data? In Fig. 11 the same comparison as in Fig. 10 is made for a device following stressing. Although some difference in the magnitude of the post-stress peak is observed, both the location and width are largely unchanged. We can conclude, therefore, that the conclusions drawn from Figs. 5–8 (made using the standard profiling technique) are not significantly altered by electric field effects.

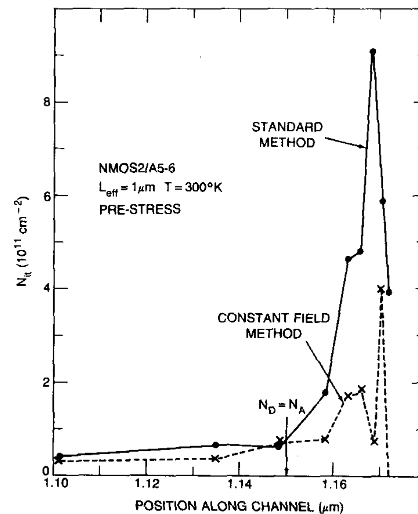

Fig. 10. Comparison of the pre-stress N_{it} profiles measured using the standard and constant field profiling techniques. The lack of a peak when the latter technique is used reveals the electric field origin of the pre-stress peak (see text).

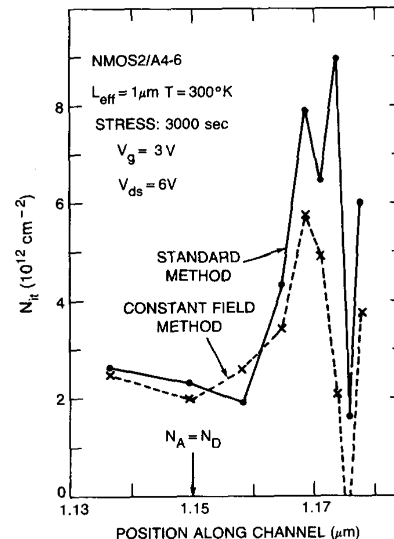

Fig. 11. Comparison of post-stress N_{it} profiles measured using the standard and constant field profiling techniques.

V. Simulation Results

As noted in the Introduction, the simulations done for this paper differ from earlier modeling efforts [9]–[11] in that we use experimentally determined D_{it} profiles as inputs to the simulations. In this way, we can make *predictions* of *I–V* characteristics that can then be compared with measured values from the same samples. To determine the doping profiles for the simulations we used SUPREM runs, correcting the profiles somewhat to be consistent with SIMS measurements and assuming a lateral diffusion ratio of 0.7. For the 2-D device simulations we employed MINIMOS 2.2 modified in order to include possibly inhomogeneous surface charge and/or interface traps. For the latter, we permit a nonuniform energy dependence as well. In most respects, these capabilities are identical with those reported in [9] and [11], including the restriction that the position and energy dependences of the D_{it} be separable. One important difference is that we have taken great care in parameterizing our mobility model to account for scattering by interface charge. The basic approach used was to determine the requisite mobility parameters by curve-fitting data from an independent experiment: *I–V* measurements on MOSFET's that were irradiated (Co^{60}) to introduce a uniform density of D_{it}.[1]

[1] We note that this approach does not account for differences in the effectiveness of scattering of uniform versus inhomogeneous interface charge.

This is an essential step if any quantitative comparisons between experimental I–V characteristics of degraded devices and predictions from simulation are to be made.

For the simulations discussed here, we assumed the spatial dependence of the hot-carrier-induced D_{it} to be a smoothed fit to profiling data obtained using the standard technique on a device with an oxide 22 nm thick that had received 200 s of stress (at $V_d = 2V_g = 7$ V). The energy dependence of the D_{it} was determined using charge pumping [5], and this was reasonably well fit by assuming a constant density below midgap and a linearly increasing density above midgap (much like that assumed in [11]). We assumed also that the interface traps are neutral when the bands are bent to midgap [14], which, as discussed below, is a key assumption.

The experimental I–V data for this sample are plotted in Figs. 12 and 13 (solid lines). Fig. 12 shows the drain current as a function of gate voltage with $V_d = 50$ mV both before stressing and following a 200-s stress while Fig. 13 compares pre- and post-stress I_{ds}–V_d characteristics with $V_g = 2$ V. In Fig. 13 both the forward and reverse (i.e., with source and drain interchanged) characteristics following the stress are shown. Finally, the simulation results for the pre-stress data are denoted by circles; good agreement is achieved by curve-fitting (i.e., by selecting an appropriate flat-band voltage and mobility parameters).

The squares in Fig. 12 represent the predictions of simulation for the I–V characteristics following stress assuming the only damage is the measured D_{it} described earlier. Qualitatively, the behavior of data and simulation are similar; however, the model does not predict nearly as large a degradation as is in fact observed. This lack of agreement is apparent also when predictions of the post-stress forward and reverse characteristics (not shown) are compared with the data of Fig. 13; the predicted asymmetry ratio (reverse current divided by forward current) is 0.9 whereas the measured value is 0.5. These disagreements represent the main finding from our simulations: The measured D_{it} damage profile appears insufficient to explain the observed degradation in transistor characteristics. Of course, this conclusion rests on the validity of both our experiments and the modeling, and, while much effort has been expended in verifying these ingredients, our conclusion must necessarily be tentative.

If in fact the measured damage profile is insufficient to account for the observed degradation, then the two simplest (and nearly equivalent) explanations for the disagreement are that either the interface traps are not neutral when the Fermi level is at midgap or that spatially inhomogeneous trapped oxide charge is present. Neither of these possibilities can be detected by the charge-pumping measurements we have performed. In order to show that these explanations are *plausible*, we have incorporated such charge (with the same spatial variation as that measured for D_{it}) into our simulations and varied the magnitude to best fit the data. The results are shown in Figs. 12 (+'s) and 13 (+'s and ×'s). Reasonably good agreement between experiment and calculation was obtained by taking the maximum value of N_{it} to be $1.2 \times 10^{12}/\text{cm}^2$. Thus, these simulations suggest that both interface traps and fixed charge (or interface traps that are non-neutral at midgap) are required in order to fully explain the observed degradation in I–V characteristics.

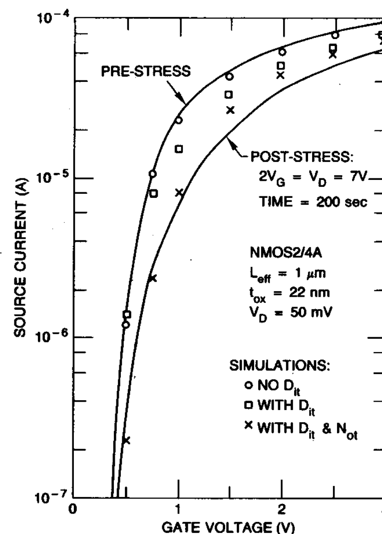

Fig. 12. Pre- and post-stress source current as a function of gate voltage for a MOSFET with $L_{\text{eff}} = 1$ μm, $t_{\text{ox}} = 22$ nm, and $V_d = 50$ mV (solid lines). The points are from 2-D numerical simulations with results when no damage is present (pre-stress) denoted by circles. Also shown are the results of simulations in which the measured post-stress D_{it} profile was included (□'s) and when the D_{it} plus an additional trapped-oxide charge profile were considered (+'s). The lack of fit when just D_{it} is included suggests that the stress induces trapped-oxide charge as well.

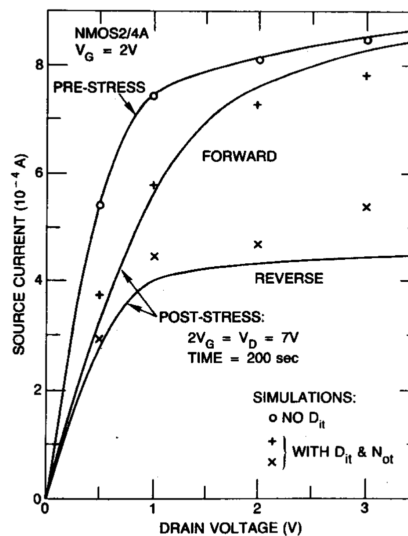

Fig. 13. Experimental (solid lines) and simulation (points) results for I_{ds} versus V_d with $V_g = 2$ V both pre- and post-stress. For the latter, both forward and reverse characteristics are shown. The results of the simulation for the pre-stress characteristic are denoted by circles. For the post-stress simulations of the forward (+'s) and reverse (×'s) characteristics, the damage was taken to consist of the measured D_{it} profile plus the same trapped-oxide charge profile used for Fig. 12 (+'s).

VI. Summary and Conclusions

The data and calculations of this paper represent the most detailed information on hot-carrier-induced damage and its electrical effects to date. Nonetheless, our findings and, particularly, various precise details are subject to errors from numerous sources (as discussed above) and should not be regarded as definitive. With this caveat, the main points made by this work are:

1) We have carried out spatial profiling experiments with greater precision than done heretofore. Through these experiments and by using MOSFET's with very thin oxides we have provided direct evidence that the point of maximal carrier heating (peak lateral electric field) is also the point of maximum hot-carrier-induced damage (D_{it}). Devices with thicker oxides do not show this sharp correlation, a fact we interpret as arising either because of significant lateral travel of hot holes inside the thicker oxide or because the point of maximum injection has shifted.

2) The importance of electric field effects in spatial profiling measurements using charge pumping has been demonstrated. A "constant field" profiling technique has been developed that minimizes spurious results arising from these effects. These findings also represent an independent confirmation of the results of [12] and [13].

3) By incorporating the spatial profiling results into 2-D device simulations, *predictions* of I–V characteristics for degraded devices were made. These are qualitatively, but not quantitatively, in agreement with measured data. We take this to be an indication that significant charge (electron) trapping accompanies the D_{it} creation.

Note Added in Proof

The recent article by C. Plossu, C. Choquet, V. Lubowiecki, and B. Ballard (*Solid State Commun.*, vol. 65, p. 1231, 1988) has reported charge-pumping data that they interpret as arising from real inhomogeneity in pre-stress N_{it}. Their results are quite similar to that shown in Fig. 6 (pre-stress) and, as discussed in this work (see Section IV-B), are likely spurious.

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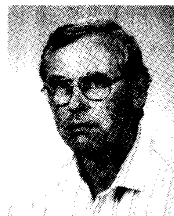

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