Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs

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***Abstract*— This paper demonstrates and investigates the time-dependent vertical breakdown of GaN-on-Si power transistors. The study is based on electrical characterization, dc stress tests and electroluminescence measurements. We demonstrate the following original results: 1) when submitted to two-terminal (drain-to-substrate) stress, the AlGaN/GaN transistors show a time-dependent degradation process, which leads to the catastrophic failure of the devices; 2) time-to-failure follows a Weibull distribution and is exponentially dependent on stress voltage; 3) the degradation mechanism is strongly field dependent and weakly thermally activated, with an activation energy of 0.25 eV; and 4) emission microscopy suggests that vertical current flows under the whole drain area, possibly through extended defects. The catastrophic failure occurs at random positions under the drain contact. The time-dependent failure is ascribed to a percolation process activated by the high-electric field that leads to the generation of localized shunt paths between drain and substrate.**

***Index Terms*— GaN, high-electron-mobility transistors (HEMTs), vertical breakdown (VB), Weibull distribution.**

I. Introduction

GaN-BASED high-electron-mobility transistors (HEMTs) grown on silicon substrate have demonstrated excellent performance, thanks to the unique properties of gallium nitride [1]: 1) the high-electron mobility (up to 2000 $cm^2 \cdot V^{-1} \cdot s^{-1}$), which minimizes the ON-state resistance (R_{ON}) of the devices; 2) the high breakdown field (3.3 MV/cm), which allows to fabricate small devices (tens of micrometer) with breakdown voltage in the order of hundreds or thousands of volts; and 3) the high thermal conductivity (>2 W cm^{-1} K^{-1}), which allows to reach high levels of power dissipation with a low increase of the channel temperature. Moreover, the use of a silicon substrate reduces production costs and guarantees a good scalability. For these reasons, GaN-on-Si HEMTs are considered excellent switches for application in power conversion systems.

Nevertheless, several mechanisms may lead to the early breakdown of the devices [2]: 1) lateral breakdown at the drain edge of the gate (where the electric field peaks), due to the converse piezoelectric effect [3] or to the time-dependent formation of traps and percolative paths [4]; this aspect is especially relevant for Schottky-gated devices; 2) lateral drain–source breakdown of the (Al)GaN buffer caused by subthreshold leakage and punch-trough effects [5]; 3) lateral breakdown of the silicon nitride (passivation) layer due to the excessive electric field at the edge of the field plate [6], [7]; and 4) vertical (buffer related) breakdown ascribed to the increase of the drain-to-substrate leakage [8]–[13].

Most of the papers in the literature focus on lateral breakdown [i.e., mechanisms 1)–3)], while only a few number of papers have been published so far on vertical leakage and breakdown: Zhou *et al.* [8] investigated the vertical leakage conduction, and showed that the drain-to-substrate leakage is a trap-assisted mechanism. The donor/acceptor defects in the buffer and in the transition layer play a key role in the conduction process. The resulting current can be explained using the Space-Charge-Limited model. The same model was also used by Moens *et al.* [9] for the investigation of temperature-dependent drain-to-substrate I–V measurements.

Umeda *et al.* [10] investigated the factors responsible for vertical conduction, and proposed to insert a p-type region in the silicon substrate (at the peripheral area of the devices) to reduce the vertical leakage through the formation of a depletion region. A different solution to improve vertical robustness consists in localized substrate removal between the drain and the gate [11], [12]. Finally, Fleury *et al.* [13] investigated the statistics and localization of vertical breakdown (VB), and preliminarily suggested that VB of GaN-HEMTs is a time-dependent process.

Despite the importance of this topic, no systematic analysis of the time-dependent VB has been published to date in the literature: several issues remain open, including the dependence of time-to-failure (TTF) on stress voltage, the thermal activation of VB, the statistics of VB, and the spatial localization of the breakdown spots.

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The aim of this paper is to contribute to the understanding of the VB process in GaN-based transistors. We perform a systematic analysis on the VB process, demonstrating that: 1) GaN-HEMTs submitted to two-terminal (drain-to-substrate) stress show a time-dependent degradation process, whose TTF is Weibull-distributed; 2) has an exponential dependence on the applied voltage; and 3) temperature-dependent measurements indicate that the VB process is weakly accelerated by temperature, with an activation energy $E_a = 0.25$ eV. Finally, emission microscopy and optical analysis suggest that failures can occur in a random position under the drain metallization. The VB process is ascribed to the generation/percolation of defects in the highly depleted GaN or in the AlN nucleation layer, induced by the high vertical field.

II. Experimental Details

The results presented in this paper were obtained on AlGaN/GaN normally-OFF HEMTs grown on a silicon substrate designed for 200-V operation. The normally-OFF condition has been obtained through the use of a p-GaN gate. With regard to VB, the most important aspect is the vertical structure of the devices, between drain and substrate contacts. Over the boron-doped silicon substrate with a resistivity comprised between 1 and 10 Ωcm, a 200-nm-AlN nucleation layer is grown. Graded backbarrier is composed by two 500-nm AlGaN layers with Al concentration, respectively, of 0.77 and 0.44. The carbon-doped buffer layer is an AlGaN alloy with 8% of Al concentration. Finally, on top of the C-doped buffer there are 300 nm of undoped GaN (channel layer), in which the 2-D electron-gas is formed. The drain-contact width is 100 μm while its length is 47 μm. Gate–drain distance is 0.85 μm. The electrical characterization and stress tests were performed by a source-meter and parameter-analyzer. All the measurements were performed keeping the gate and the source floating, while the substrate was connected to ground, and the drain was biased at constant voltage. These stress conditions are referred to as "two-terminal stress" in the following. The measurements were carried out at different ambient temperatures. Emission microscopy measurements and optical analysis were done using a cooled charge-coupled device (CCD) camera.

III. Results and Discussion

A. Vertical Leakage Conduction: Preliminary Tests

Before the execution of the stress experiments, we investigated the physical origin of vertical leakage current. Fig. 1(b) shows the two-terminal (between drain and source) leakage measurements performed on five devices belonging to the same wafer. The leakage curves in Fig. 1 were measured by sweeping from $V_D = 0$ V to $V_D = 850$ V [Fig. 1(b)] and from 850 to 0 V (not shown): the vertical I–V curves do not demonstrate any hysteresis, indicating the absence of the slow trapping processes in the buffer. Two conduction mechanisms can be noticed (see the change in slope above $V_D = 300$ V). This result is consistent with previous studies [8], [9], and has been explained by considering the following: for $V_D < 200$ V, conduction is nearly ohmic (possibly involving dislocations), since the slope of the log–log I–V curves is nearly 1.

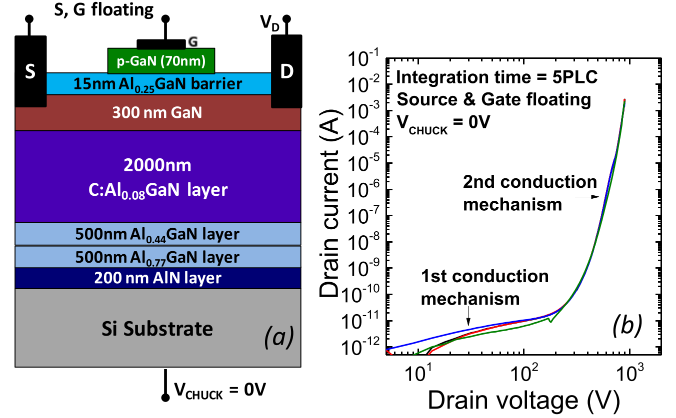

Fig. 1. (a) Schematic representation of the device under test. (b) Drain-controlled vertical leakage current measurement. The measurements were stopped at breakdown.

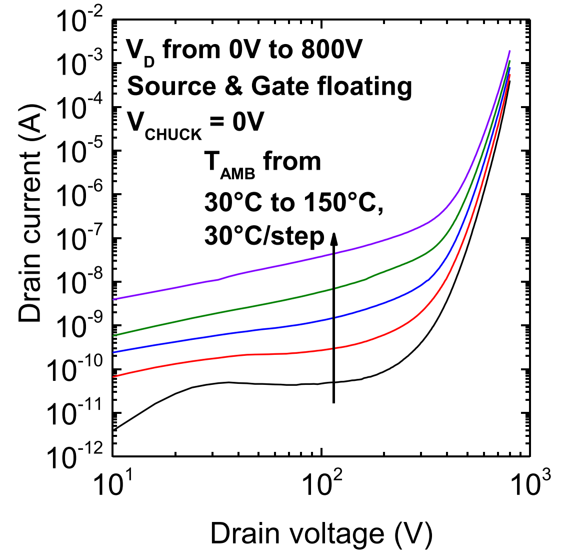

Fig. 2. Leakage current measurements performed at different ambient temperatures ranging from 30 °C to 150 °C.

For $V_D > 300$ V, the buffer is significantly depleted, and the defects (possibly C atoms at the nitrogen site, C_N) are ionized. As described in [9], the high-electric field for $V_D > 300$ V may favor Poole–Frenkel emission process (Fig. 3), and allows the charge stored in the ionized C_N acceptors to leak out of the traps. This leads to a strong increase in vertical leakage for $V_D > 200$ V (where $I–V^k$, $k = 18$). By fitting the Poole–Frenkel current equation ($\propto I E e^{-\Phi_B/\mathrm{kT}} e^{\beta\sqrt{E}/\mathrm{kT}}$) with the leakage measurements at different ambient temperatures (Fig. 2), we extrapolated—in a first approximation—the depth of the trap level involved in the conduction process to be equal to 1.1 eV; this value—considering the degree of approximation of this analysis—is consistent with the carbon related defects (C_N, 0.85–0.95 eV). The reported conduction mechanism can be explained with the space-charge-limited model: until all the traps are not ionized, the conduction is nearly ohmic; as soon as the applied voltage reaches a specific value (i.e., trap filled limit voltage) and all the buffer traps are ionized, the current starts to increase rapidly, according to the trap filled limited model.

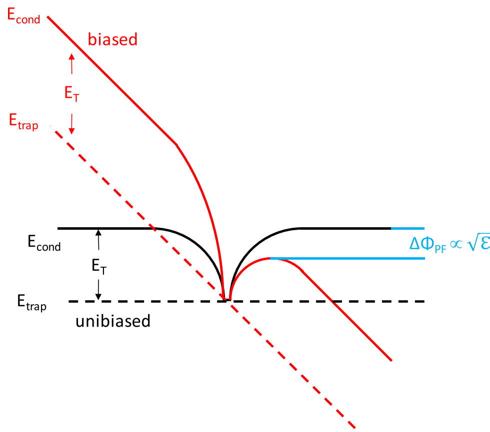

Fig. 3. Schematic representation of the Poole–Frenkel emission at high drain bias.

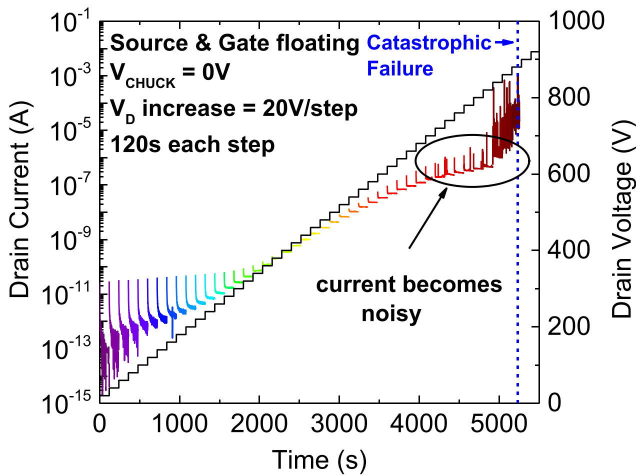

Fig. 4. Drain current monitored during the step stress (V_{CHUCK} = 0 V, V_D increases in 20-V steps).

By varying the ambient temperature, the leakage current increases (Fig. 2, consistently with Moens *et al.* [9]) due both to the increased availability of free carriers and to a stronger ionization of buffer traps.

B. Results of Step-Stress Experiments

The analysis reported in Fig. 1 reveals that—during a two-terminal breakdown sweep—the devices under test fail when the voltage applied between drain and substrate reaches 900 V. In order to obtain a better understanding on the failure mechanisms and on the vertical robustness, step-stress experiments were performed. The voltage between drain and substrate was increased by 20 V every 120 s, from $V_D = 0$ V up to the failure. All the measurements presented within this paper were obtained by biasing the drain, with only the substrate grounded. The gate and the source were left disconnected; the notation $I_G = I_S = 0$ A means that no current can flowthrough the gate and source contacts due to the absence of an electrical connection. Representative results are reported in Fig. 4: the device showed a stable behavior up to a drain voltage of 700 V. For higher stress voltages, the noise superimposed to the drain leakage current showed a significant increase, indicating

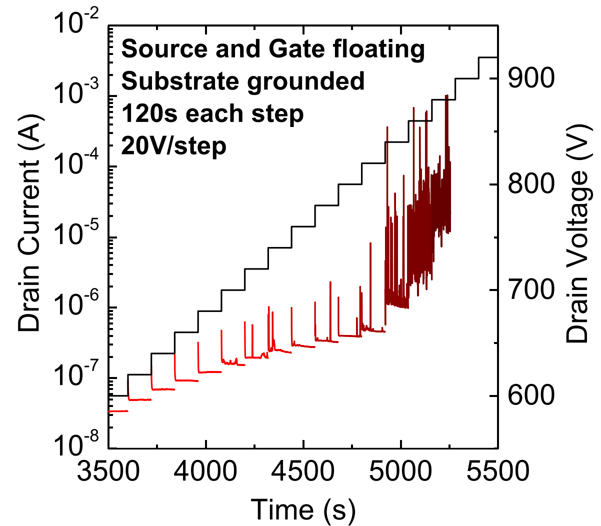

Fig. 5. Drain current monitored during the last 15 steps before failure occurs.

the generation of random conductive paths between adjacent defects [14], [15] (see also the enlargement of the last steps in Fig. 5). Breakdown was found to occur at $V_D = 870$ V, which is lower than the breakdown voltage estimated by dc sweeps (Fig. 1). The results in Figs. 4 and 5 suggest that the vertical (drain–source) breakdown is a time-dependent process, that is accelerated by the high-electric field. Details on this time-dependent degradation process are described in detail in the following.

C. Constant Voltage Stress Experiment: Dependence of TTF on Voltage and Temperature

In order to investigate the dependence of the degradation kinetics on voltage and temperature, we carried out a set of constant voltage stress tests. Based on the results of breakdown measurements and step-stress tests, three voltages were imposed during the constant voltage stresses, namely, 770, 800, and 820 V. Fig. 6(a) reports the variation of the leakage current measured during the stress of 18 identical samples at $V_D = 800$ V. Vertical leakage current is initially stable, and slightly decreases due to the occurrence of the charge trapping effects. For sufficiently long stress times, the current becomes noisy, suggesting the occurrence of a defect generation process. The failure consists in a sudden increase in the leakage current that leads to the catastrophic failure of the devices. This behavior is similar to the time-dependent breakdown of dielectrics that is commonly explained by the defect percolation theory [16].

Fig. 6(b) reports the TTF and leakage current of several devices stressed at the three different voltage levels. With increasing stress voltage, an increase in leakage current and a decrease in TTF is observed.

Fig. 7(a) shows that the TTF follows a Weibull distribution. The scale parameter α is the time at which 63.2% of the devices under test fail, while the shape parameter β specifies the failure rate behavior. The cumulative Weibull distribution is expressed as $F_t = 1 - \exp(t/\alpha)^{\beta}$. The scale parameters, with 50% of confidence level, are 10511.5, 2868.5, and 863.2 s,

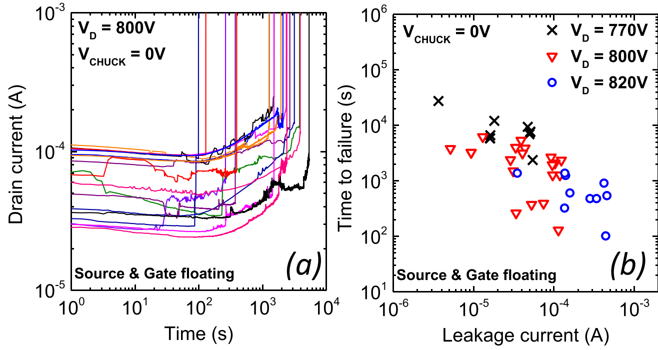

Fig. 6. (a) Drain current monitored during a constant voltage stress ($V_D = 800$ V). (b) TTF dependence on the initial leakage for three drain bias levels applied during the constant voltage stress.

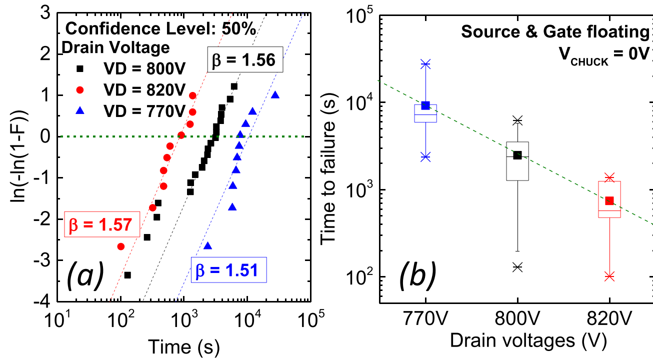

Fig. 7. (a) Weibull plot of the constant voltage stress. (b) TTF dependence on the applied drain voltage (box chart).

respectively, at drain bias of 770, 800, and 820 V. In agreement with the percolation theory [16], the drain voltage accelerates the failure mechanisms, resulting in a lower TTF at higher voltages. Shape parameters are larger than 1 and range between 1.51 and 1.93, thus suggesting that the breakdown is related to the intrinsic properties of the material rather than to extrinsic factors [17].

Fig. 7(b) shows the box chart of the dependence of the TTF on the applied voltage; the TTF exponentially decreases with increasing stress bias, indicating that the degradation process is strongly field dependent.

To evaluate the impact of temperature on TTF, we performed constant voltage stress tests (stress voltage = 770 V) at different ambient temperatures, namely, 30 °C, 90 °C, and 150 °C [Fig. 8(a)]. Increasing stress temperature shortens the TTF: the activation energy of the failure mechanism results $E_a = 0.25$ eV [Fig. 8(b)]. Results indicate that TTF is strongly (exponentially) dependent on the electric field, indicating that the degradation process is field dependent. On the other hand, a low thermal activation ($E_a = 0.25$ eV) was found. This result supports the hypothesis that degradation is primarily activated by voltage, while temperature acts only as a weak acceleration factor.

The results allowed us to evaluate the dependence of TTF on the applied voltage. Fig. 9 shows that the maximum applicable voltage for a lifetime of 20 years with 1% failure rate is about 560 V at room temperature, considerably higher than the operating voltage of the devices under test (200 V).

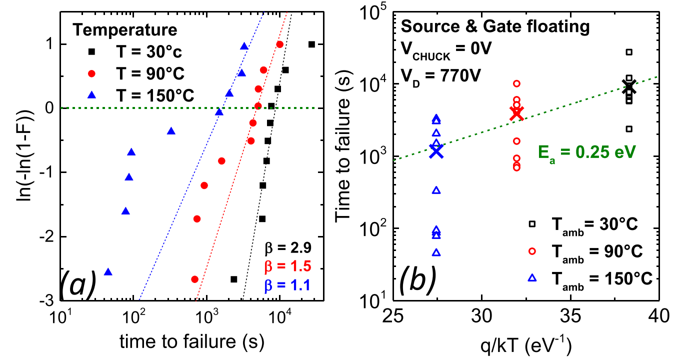

Fig. 8. (a) Weibull plot of constant voltage stress ($V_D = 770$ V, T_{AMB} ranging from 30 °C to 150 °C). At high temperature a secondary failure mechanism shortens the lifetime of some devices. (b) Corresponding Arrhenius plot.

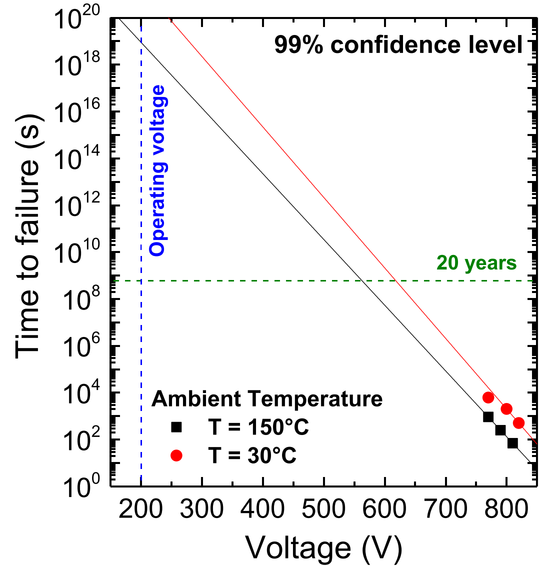

Fig. 9. TTF dependence on the drain voltage applied at ambient temperature of 30 °C and 150 °C. Each point represents the Weibull scale factor with a confidence level of 99%.

Consistently with the low activation energy of the failure mechanism, analogous results were estimated at higher temperature (150 °C).

D. EL Measurements and Failure Analysis

In order to collect more information on the physical origin of VB, we investigated the EL pattern emitted by the devices during stress. This allows to investigate on the presence of electroluminescence, and to identify the presence/position of the leakage paths responsible for breakdown. Fig. 10 reports the false color pattern of the electroluminescence measured during a stress experiment at three different voltages, namely, 650, 850, and 860 V. The stress/acquisition was changed accordingly, in order to avoid the saturation of the CCD camera. The leakage current monitored during the emission reveals results consistent to the step-stress analysis: for low drain voltage ($V_D = 650$ V) the current remains stable with a slight noise superimposed to the curve; at higher bias levels ($V_D = 850$ V, 860 V) the leakage current increases until the catastrophic failure occurs. The stress is applied in a two-terminal configuration, i.e., between drain and substrate,

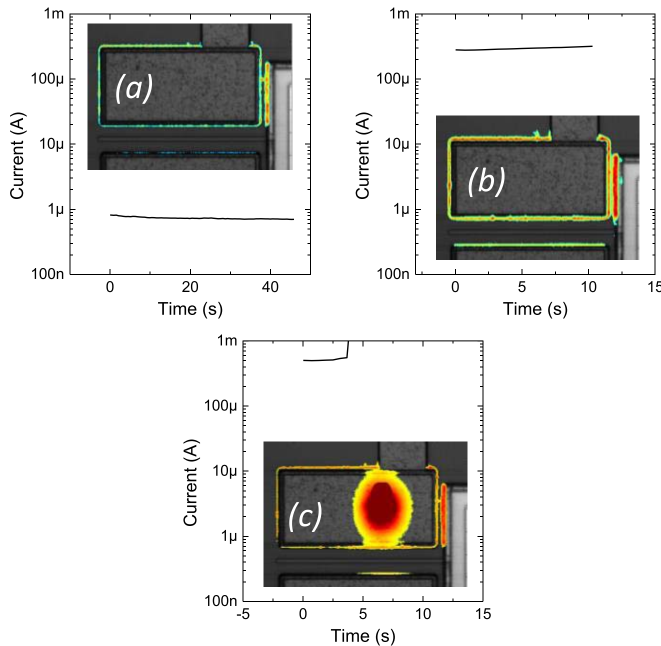

Fig. 10. Emission microscopy acquired at different drain bias levels, namely, (a) $V_D = 650$ V, (b) $V_D = 850$ V, and (c) failure voltage ($V_D = 860$ V). The EL patterns were taken under constant voltage conditions. The reason is that a long integration time is needed, due to the fact that the luminescence emitted by the devices is weak. The EL pattern is reported along with the current measured during the execution of the EL test (lasting few tens of seconds). As can be noticed, the current flowing through the devices is stable during the EL measurements, apart from the last step when the device fails.

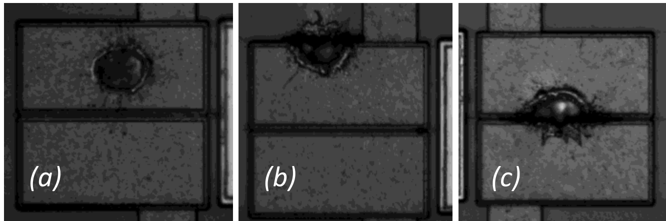

Fig. 11. Photograph taken after the catastrophic failure. Damage can be located (a) in the middle of the drain pad, (b) at the edge of the gate pad, and (c) in the edge of the drain pad next to the gate finger.

by keeping the source and the gate terminal floating. As it can be noticed, a significant EL signal is detected all around the drain pad. Since the drain contact is ohmic, and the field is applied vertically, we infer that the EL signal is emitted on the overall drain area, but visible only outside the thick drain metallization.

Failure occurs at random positions under the drain contact, either at the center of the pad, or at the edges (see three representative examples in Fig. 11). We suggest that failure is a random process: in the following, we discuss the physical origin of time-dependent breakdown.

During a two-terminal vertical stress, a high bias is applied between drain and substrate. Vertical leakage current flows mainly through dislocation-related paths [18], [19]; several works ascribe the conduction to the pure-screw dislocation [20], [21] but also a moderate bulk conduction is possible due to the nonideal compensation of the buffer and the corresponding residual conductivity.

The deeply depleted buffer behaves as a leaky dielectric, and shows a time-dependent breakdown, similar to what happens when dielectrics are subject to high-electric field. The main difference between the TDDB of dielectrics and the process described within this paper is that in the present case the failure is detected in a semiconductor (a wide bandgap semiconductor, depleted) and not in an insulator. We suggest that the breakdown could be facilitated in proximity of dislocations, where a higher (vertical) leakage might accelerate the defect generation process.

When the drain bias reaches 850 V, this voltage drops on the 3500-nm-thick buffer, resulting in an average electric field of 2.4 MV/cm (the breakdown field of GaN is 3.3 MV/cm). Under these conditions, two regions may be subject to a higher vertical field: 1) the AlN nucleation layer, that is located between the conductive silicon substrate and the AlGaN buffer, as was proposed in [13] and 2) the undoped GaN channel layer that, due to the significantly low free charge density, is highly depleted at high drain voltages. We suggest that failure originates in one of these two regions: once a short circuit path is created through the GaN channel or the AlN layer, it propagates vertically thus leading to the creation of a shunt between the drain and the substrate. This process is promoted by the high-electric field [consistently with the results in Fig. 7(b)], while temperature has only a minor role in the degradation process [Fig. 8(b)].

IV. Conclusion

In this paper, we have presented a systematic analysis of the time-dependent breakdown of GaN-based HEMTs submitted to two-terminal vertical stress.

We demonstrated that the drain-substrate stack shows a time-dependent degradation, similar to the time-dependent breakdown of a dielectric material: TTF is Weibull distributed, with a shape factor greater than 1, indicating the existence of an intrinsic failure process. The failure mechanism is strongly field dependent, and weakly thermally activated ($E_a < 0.25$ eV).

The failure of the devices occurs due to the creation of a defect path (percolation path) between drain and substrate; the presence of defective leakage paths is confirmed by the electroluminescence analysis. The time-dependent failure is supposed to originate in the undoped GaN channel layer or in the AlN nucleation layer, due to a defect generation and percolation process enhanced by the electric field. In order to improve the vertical robustness of the devices two aspects have to be taken into account: 1) the density of defects within the vertical stack has to be minimized and 2) the electric field profile must be optimized, with the aim of spreading the voltage drop among all the interfaces/layers.

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