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Capacitance study of inversion at the amorphous-crystalline interface of n-type silicon heterojunction solar cells

Jian V. Li,[a] Richard S. Crandall, David L. Young, Matthew R. Page, Eugene Iwaniczko, and Qi Wang
National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, Colorado 80401, USA

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We use capacitance techniques to directly measure the Fermi level at the crystalline/amorphous interface in n-type silicon heterojunction solar cells. The hole density calculated from the Fermi level position and the inferred band-bending picture show strong inversion of (n)crystalline silicon at the interface at equilibrium. Bias dependent experiments show that the Fermi level is not pinned at the interface. Instead, it moves farther from and closer to the crystalline silicon valence band under a reverse and forward bias, respectively. Under a forward bias or illumination, the Fermi level at the interface moves closer to the crystalline silicon valence band thus increases the excess hole density and band bending at the interface. This band bending further removes majority electrons away from the interface leading to lower interface recombination and higher open-circuit voltage. © *2011 American Institute of Physics*. [doi:10.1063/1.3663433]

I. INTRODUCTION

Silicon heterojunction (SHJ) solar cells have attracted extensive research due to their remarkable performance.[1] One particular merit is their high open-circuit voltage, which has been in part attributed to low recombination rate[2] at the interface between hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si). Recent studies[3] suggest that the repulsion of majority carriers from the interface by an inversion layer is an important mechanism for the reduction of interface recombination. The study of inversion phenomenon gains additional motivation by the fact that the photogenerated minority carriers are of the same type as the free carriers in the inverted absorber and thus share the same transport mechanisms. Experimental evidence for this inversion layer, however, has been found only in specially prepared coplanar structures or cleaved samples.[4,5] Moreover, crucial details such as Fermi-level position, E_F, at the interface and its evolution with external bias or illumination are still lacking.

A prominent charge distribution such as free carriers in the inverted semiconductors should be observable by capacitance techniques, which has been the tool of choice for probing minute irregular charge distributions and response such as deep levels. This work is launched to gain greater understanding of the charge distribution and transport around the a-Si:H/c-Si junction using a host of capacitance measurements: admittance spectroscopy, deep-level transient spectroscopy (DLTS), capacitance-voltage, and drive-level capacitance profiling (DLCP). Note that all experiments are conducted on regular SHJ solar cells instead of specially prepared test structures. We measure the Fermi-level position at the a-Si:H/c-Si interface using the admittance spectroscopy[6] technique. This measurement enables one to construct the complete band-bending picture in c-Si and calculate the free-carrier density at the interface. We further study how the Fermi-level position changes with bias voltage and light illumination. The evolution of band bending at forward bias and under illumination reveals key mechanisms for suppressing interfacial recombination in SHJ solar cells.

II. EXPERIMENTAL DETAILS

The SHJ solar cells used in this study were fabricated on high quality n-type Czochralski silicon substrates with uniform doping ($\sim 3.5 \times 10^{15}\,\mathrm{cm}^{-3}$). A schematic of device structure is shown in Fig. 1. Three layers were deposited on top of the substrate to form the heterojunction and top contact: a thin intrinsic a-Si:H layer (3 to 12 nm), a 20-nm-thick boron-doped p-type a-Si:H layer (conductivity $\sim 1 \times 10^{-3}\ \Omega^{-1}\,\mathrm{cm}^{-1}$), and a 76-nm-thick indium tin oxide layer, in that order. More layers were deposited at the bottom of the substrate to form a back-surface-field structure (an intrinsic a-Si:H layer and phosphorus-doped n-type a-Si:H layer, $\sim$20 nm) and an Ti/Pd/Ag/Pd back contact. Unless otherwise mentioned, all data shown here are taken from a device with 8 nm intrinsic a-Si:H layer and an active area of 0.16 cm^2. Other details of device fabrication and performance are published in Ref. 7.

We use an Agilent 4294A impedance analyzer to measure the capacitance of the devices in a cryostat as a function of DC bias voltage, AC modulation voltage, frequency, and temperature. The error in the frequency measurement is +/−40 ppm. The resolution of capacitance measurement, which is a more applicable specification than the absolute error in the context of differential data processing, is better than 1 pF or 0.03%. The temperature reading is taken from a calibrated silicon diode temperature sensor attached directly to the top of the device to be measured. The error of temperature measurement is +/−0.1 K. The DLTS data are taken using a SULA system with various rate windows (20 μs to

[a]Electronic mail: jian.li@nrel.gov.

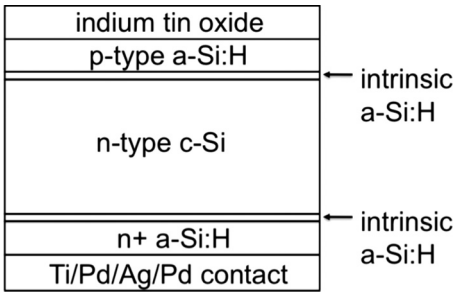

FIG. 1. Schematic device structure of an n-type SHJ solar cell used in this study. The drawing is not to scale.

100 ms). The DLCP data are taken with an AC modulation voltage ranging from 15 to 215 mVrms in 40 mV steps.

III. RESULTS

We first inspect the admittance spectroscopy results taken at zero bias. As seen in Fig. 2, the capacitance measured at a fixed temperature exhibits a transition in its frequency dependence: the capacitance drops to a lower value above certain frequency. The transition frequency f_{pk} at any measurement temperature, T, can be identified by the frequency derivative of the capacitance (Fig. 2). The temperature dependence of f_{pk} taken at 0 V bias is viewed in Figure 3 as an Arrhenius plot—the logarithm of $2\pi\ f_{pk}/T^2$ plotted against the inverse measurement temperature. The linear dependence of the data indicates the thermally activated nature of this charge exchange process. The slope of this line yields an activation energy $E_a = 161 \pm 5$ meV. Also, shown in Fig. 3 is the Arrhenius plot of admittance spectroscopy data taken at −4 V reverse bias, which yields an activation energy (203 ± 12 meV) higher than the zero bias case.

The DLTS experiments provide additional information to that obtained by admittance measurements. Figure 4 shows the DLTS spectra taken at various rate windows. The polarity of the DLTS signal clearly points to thermal emission of *minority* carriers. Note that the DLTS experiment was conducted at a quiescent voltage of −4 V and pulse voltage height of 4 V, i.e., the device was not put under positive bias. The Arrhenius plot extracted from DLTS data is also shown in Fig. 3. Within experimental error, the two Arrhenius plots from admittance spectroscopy and the DLTS

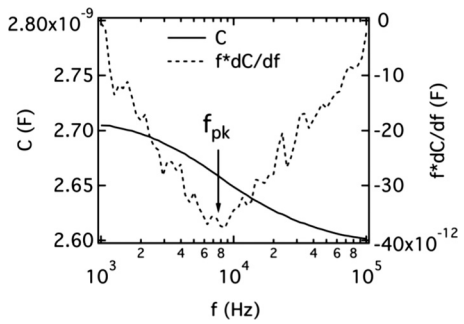

FIG. 2. The frequency dependence of capacitance (solid) and differential capacitance (dashed) measured at 176 K and 0 V bias. The arrow indicates the transition frequency f_{pk} at which the capacitance exhibits a downward transition and differential capacitance exhibits a negative peak.

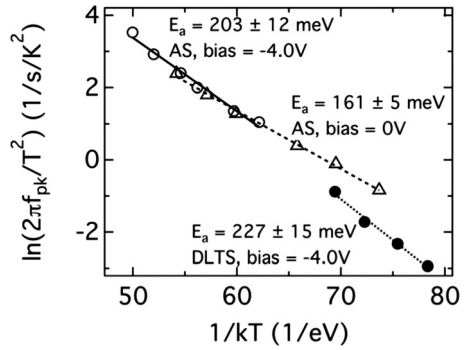

FIG. 3. The Arrhenius plots of $\ln(2\pi\ f_{pk}/T^2)$ versus 1/kT based on admittance spectroscopy measurement conducted at 0 V (open triangles) and −4.0 V (open circles) bias. Also, shown is the Arrhenius plot based on the DLTS measurement (raw data shown in Fig. 4). The device is in dark.

experiments (same bias condition) achieve an exact match, i.e., same activation energy and pre-exponential factor. This establishes that the signatures observed in admittance spectroscopy and the DLTS experiments are of the same physical origin.

We then examine the effect of external bias by extracting the activation energy from admittance spectroscopy measurement at various biases. The results are shown in Fig. 5. As the bias changes from reverse bias towards forward bias, the activation energy decreases. Similar bias dependence of activation energy is also observed in the DLTS experiments (data not shown). We further examine the effect of illumination by subjecting the device to white light illumination (~0.2 AM1.5 sun judging from the short-circuit current density). Under the same bias of 0 V, admittance spectroscopy data taken under white light yields an activation energy 20–30 meV smaller than that in dark (Fig. 6).

Lastly, we observe a peculiar discrepancy between the carrier density profile obtained by the conventional capacitance-voltage method and that by the drive-level capacitance profiling method. The carrier concentration profile measured by the conventional capacitance-voltage technique[11] N_{cv} (Fig. 7) is flat under large reverse bias and then decreases with increasing forward bias. This is rather

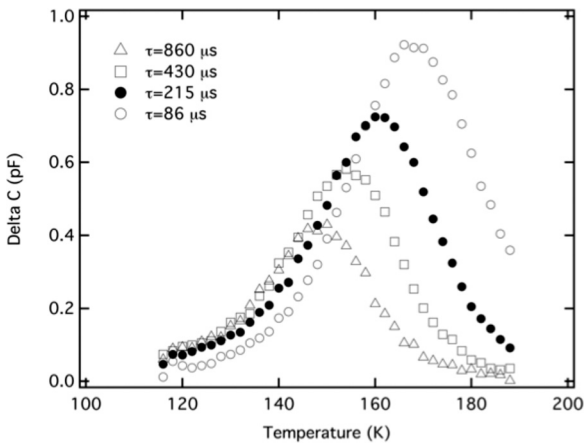

FIG. 4. DLTS spectra taken at a rate window of 86, 215, 430, and 860 μs. The experiment is conducted with a quiescent voltage of −4.0 V, a filling pulse voltage of 0 V, and filling pulse duration of 300 μs.

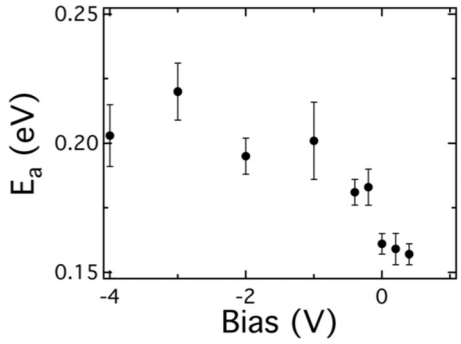

FIG. 5. The activation energies determined by admittance spectroscopy plotted versus external DC bias with the device in dark.

unexpected since the substrate is uniformly doped. The actual uniformity of carrier concentration is more closely represented by the drive-level capacitance profiling measurement[12] (N_{dl}, Fig. 7), which is flat under all biases.

IV. DISCUSSION

Initially, we establish the origin of the activation energy extracted from the admittance spectroscopy and the DLTS experiments. Probable candidates include carrier capture/emission due to deep levels in the bulk of the space charge region, carrier capture/emission at the a-Si/c-Si interface, freeze-out of conductivity in the quasi-neutral (p)a-Si or (n)-c-Si regions, and secondary potential barrier such as band offsets at the a-Si/c-Si interface and back contact.

We first eliminate the possibility of carrier capture and emission by deep levels in the bulk of the space charge region due to several reasons. The most obvious reason is that the activation energy due to a discrete bulk deep level should not exhibit bias dependence. On the contrary, a strong bias dependence (Fig. 5) has been seen by both the admittance spectroscopy and the DLTS experiments. Moreover, *minority* carrier trapping by a deep level typically is not observed by admittance spectroscopy due to the low density of captured/emitted minority carriers where the deep level intercepts the Fermi level in the depletion region. This is contradicted by our experimental finding: the admittance spectroscopy signature, if it was due to a deep level, is

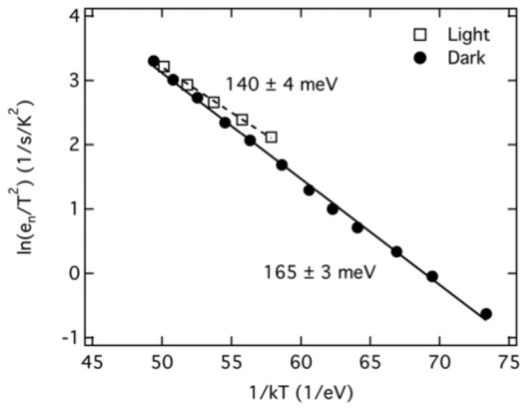

FIG. 6. Arrhenius plots based on admittance spectroscopy measurement taken at 0 V with and without illumination.

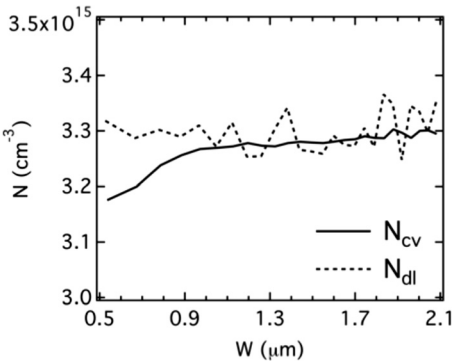

FIG. 7. The carrier concentration N versus depletion width W extracted by conventional capacitance-voltage (solid) and the deep level capacitance profiling technique (dashed). Data were taken at modulation frequency of 10 kHz and T = 295 K with the device in dark.

clearly due to minority carrier trapping/detrapping as shown by the polarity of the DLTS signal (Fig. 4).

We then eliminate the possibility of conductivity freeze-out in the quasi-neutral (p)a-Si or (n)c-Si regions. The conductivity freeze-out phenomenon is characterized by the dielectric relaxation frequency $\omega_{dr} = \sigma/\varepsilon$ where σ is the conductivity and ε the permittivity. In an actual solar cell device environment, the conductivity freeze-out occurs at the modified dielectric relaxation frequency due to the depletion capacitance. A back-of-the-envelope calculation shows that both the (p)a-Si material (conductivity ~0.001 S/cm) and the (n)c-Si material (doping of $3.35 \times 10^{15}\,\mathrm{cm}^{-3}$) used in this work should exhibit conductivity freeze-out above 1×10^{9} Hz at T = 300 K, which is much higher than the inflection frequency of $\sim 1 \times 10^{7}$ Hz that would be seen by our admittance spectroscopy experiment at T = 300 K (this value is not measured but obtained via extrapolation from data shown in Fig. 3).

Lastly, we eliminate the possibility of secondary potential barriers contributing to the admittance spectroscopy and the DLTS data. The back contact potential barrier can be ruled out by the absence of rollover feature in the temperature dependent current-voltage measurement. The valence band offset between a-Si and c-Si is in the range of 0.4–0.5 eV according to most reports.[8–10] This does not agree with the activation energy (~0.16 eV at 0 V) extracted from admittance spectroscopy. The conduction band offset, on the other hand, is in close numerical agreement with the activation energy. However, too few electrons are present at the a-Si/c-Si interface for the conduction band offset to account for the admittance spectroscopy data.

With the most probable competing mechanisms eliminated, we are now ready to establish that the activation energy extracted by admittance spectroscopy is due to the carrier exchange between the holes in the inverted c-Si and the Fermi level at the a-Si/c-Si interface. As seen in the schematic band diagram (Fig. 8(a)), this carrier exchange process is thermally activated with its activation energy being the difference between the Fermi level and the c-Si valence band edge at the interface. Once reaching the Fermi level, the holes transport through the intrinsic amorphous silicon by hopping through defects states.[7] As illustrated in Figs. 8(b) and 8(c),

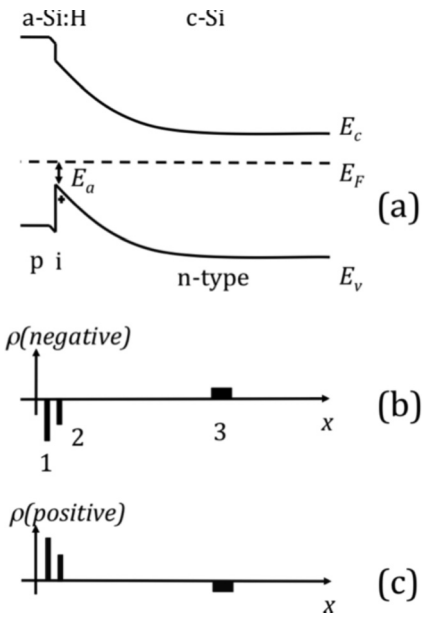

FIG. 8. Schematic band diagram (a) of a SHJ solar cell with n-type c-Si substrate at 0 V bias. The "+" sign indicates free holes at the a-Si:H/c-Si interface due to inversion. Also, shown is the charge response during the negative (b) and positive (c) period of AC modulation.

there are three parts of the charge response: (1) holes at the boundary of depletion region in (p)a-Si; (2) the holes on the c-Si side of the a-Si/c-Si interface, and (3) electrons at the boundary of depletion region in (n)c-Si. During the negative half of the modulation period, holes move from the interface to the p layer (Fig. 8(b)). During the positive half period, holes move from the p layer to the interface (Fig. 8(c)). The charge responses #1 and #3 are majority carrier responses (i.e., dielectric relaxation[11]) and thus exhibit no frequency limit in the observation window of this work. The charge response #2, however, does exhibits frequency dependence as demonstrated by the admittance spectroscopy experiment depicted in Fig. 2. When the modulation frequency is below $f_{pk} = 1/e_n$, where e_n is the exchange rate between the holes at the interface and the Fermi level, the holes can respond at the modulation frequency. Above f_{pk}, the hole response is limited by the rate of carrier exchange and cannot keep up with the AC modulation. The reduced hole response at the interface leads to a smaller capacitance above f_{pk}, because the measured capacitance is inversely proportional to the effective separation (i.e., the first moment) of charge responses.[12]

An external DC bias perturbs the dynamic balance of hole currents flowing in both directions between a-Si:H and c-Si. As a result, the density of holes at the interface changes which in turn moves the Fermi level position. Indeed, the increase of E_a with reverse bias (Fig. 5) indicates that the Fermi level is not pinned at the interface and the number of holes decreases with reverse bias. This is reasonable because the net hole current flows in the direction pointing from the a-Si/c-Si interface to the (p)a-Si under a reverse bias. The decrease of E_a under a forward bias (Fig. 5) indicates stronger inversion due to the holes injected from the a-Si side. The E_a dependence on external bias is consistent with the decrease of E_a under illumination (Fig. 6). Thus, either hole injection from (p)a-Si at forward bias or photogeneration of minority holes increases the hole density on the c-Si side of the a-Si/c-Si interface.

The DLTS provides further insights to the bias dependence of the charge distribution. The DLTS data shown in Fig. 5 record the transient capacitance at a quiescent voltage of −4.0 V following a filling voltage pulse reaching 0 V. According to the above discussion, more holes are present at 0 V (i.e., during the filling voltage pulse) than at −4.0 V. At the beginning of the transient (i.e., time 0, immediately following the termination of the filling voltage pulse), the excess holes are still located at the interface. Electrostatic theory dictates that the depletion region width in c-Si at time 0 is smaller than the steady-state case (at −4.0 V). Therefore, the capacitance at the beginning of the transient (time 0) is larger than the steady-state capacitance at −4.0 V after the transient is over (time infinity). This explains the polarity of the DLTS signal (Fig. 4). The fact that the activation energy extracted by DLTS agrees with that by admittance spectroscopy indicates that the excess holes provided by the filling voltage pulse also transport through the same path to the Fermi level and then through the i-layer via hopping.

The capacitance-voltage measurements (Fig. 7) provide further confirmation to the existence of free holes at the interface and their response to bias perturbation. It has been long realized that the presence of free carriers in the depletion region leads to breakdown of the depletion approximation.[13] As shown in Figs. 8(b) and 8(c), the charge response #2 due to the holes at the interface is inserted between the two depletion-induced charge responses at the depletion boundaries (#1 and #3), leading to a smaller effective separation (or first moment)[12] of charge responses. Because the measured capacitance is inversely proportional to the effective separation of charge responses,[12] this inversion-induced charge response results in a measured capacitance larger than the depletion capacitance. As the bias moves from a large reverse bias toward forward bias, the deletion region width decreases. The relative weight of this inversion-induced capacitance enhancement therefore increases. The overall bias dependence of the measured capacitance in turn leads to an apparent trend of "decreasing" N_{cv} with forward bias. The DLCP technique, on the other hand, is insensitive to charge response near the interface[12] therefore yielding the uniform carrier density as expected.

The value of 161 meV Fermi energy separation at the (p)a-Si:H/(n)c-Si interface supports recent observations[5] of an inversion layer. Borrowing from the common definition of "strong inversion" of metal-oxide-semiconductor (MOS) device,[8] the extent of inversion is categorized as strong inversion. The hole density at the interface is $p_{inv} = N_V{*}exp[(E_V - E_F)/kT] = 5.6 \times 10^{16}\,\mathrm{cm}^{-3}$, where N_V is the valence band effective density of states and k is Boltzmann's constant. Measurement of Fermi energy separation at the a-Si:H/c-Si interface from devices with a thicker intrinsic a-Si:H layer (~12 nm) yields values ~270 meV. This indicates that a thick intrinsic a-Si:H layer may weaken inversion and reduce band bending in c-Si by consuming too much potential. We note that the inversion increases with reverse

bias in an MOS capacitor, contrary to the bias dependence in a SHJ device discussed above. The key difference here in a SHJ device is that the intrinsic a-Si:H layer is permeable to holes and allows extraction/injection of holes from/to the inversion layer via the intrinsic a-Si:H.

We can now quantitatively construct the band-bending picture (Fig. 8(a)) in c-Si at equilibrium. After obtaining the Fermi level position in the bulk c-Si from the bulk carrier concentration (e.g., 234 meV below the conduction band for n-type doping of $3.35 \times 10^{15}\,\mathrm{cm}^{-3}$ in our samples), one can then calculate the band bending in c-Si by subtracting the bulk and interface Fermi energy separations from the bandgap of c-Si (e.g., $\phi_{bi} = 730\,\mathrm{mV}$ in our sample). The total band bending of the entire SHJ device contains an additional term of band bending in a-Si:H which amounts to $\sim$0.2 V according to a numerical solution of the Poisson solution. This is consistent with the high open-circuit voltage observed in SHJ devices (e.g., 671 meV for the device studied in this work).

A stronger inversion under a forward bias or illumination means that the band bending at the a-Si:H/c-Si interface increases (the band bending in the rest of the depletion region still decreases owing to the forward bias) under such operating conditions. The resulting greater band bending (than equilibrium case in dark) adjacent to the a-Si:H/c-Si interface further repels majority electrons away from the interface. Therefore, the interface recombination is effectively suppressed. We believe the evolution of band bending at the a-Si:H/c-Si interface under illumination explains, in part, why the open-circuit voltage of SHJ solar cells is high.

V. SUMMARY

We directly observe the inversion layer at the a-Si:H/c-Si interface in n-type heterojunction solar cells by admittance spectroscopy measurements corroborated by other capacitance techniques. The Fermi level position at the interface is measured by admittance spectroscopy. We calculate the density of holes at the interface and infer the band bending picture in c-Si from the Fermi level. The hole density ($10^{15} \sim 10^{16}\,\mathrm{cm}^{-3}$) indicates that the c-Si at the interface is strongly inverted at equilibrium. The Fermi level is not pinned at the interface. It moves up and down under a reverse and forward (or under illumination) bias, respectively. The band bending (electric field) at the interface thus *increases* under a forward bias (or under illumination). Such an enhancement of band bending in the presence of excess minority carriers is key to the high open-circuit voltage in a-Si:H/c-Si heterojunction solar cells, because it reduces interface recombination by further repelling majority electrons from the interface.

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