BiCMOS Integrated Microfluidic Packaging by Wafer Bonding for Lab-on-Chip Applications

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***Abstract*—In this paper, a fully BiCMOS integrated microfluidic technology platform for Lab-on Chip (LoC) applications is presented. Fusion bonding and adhesive bonding techniques are applied to realize a 3-wafer-stack integration. A glass wafer is used on top of the BiCMOS wafer and the Si channel wafer to enable simultaneous optical and electrical measurements. An alignment accuracy of less than 1 μm between BiCMOS and channel wafer is achieved while having channel heights between 30 and 100 μm. All the microfluidic process integration steps are kept below 300 °C. The microfluidic inlet and the outlet are positioned on the backside of the wafer stack to provide both the optical inspection and the electrical measurements from the wafer's front side. The developed wafer level integration technique provides high throughput solutions for emerging chemical and biological LoC applications.**

***Keywords*-Wafer bonding; Microfluidics; Lab-on-Chip (LoC); packaging; CMOS compatible**

I. Introduction

In the recent years, there is a growing interest on analyzing chemical and biological samples in fast and reliable way [1]. Small amounts of those samples can be flown through microfluidic channels to reaction chambers or electrical sensors [2]. Due to the small amounts and the controlled flow of the samples in microfluidic channels [3], it is possible to have high sensitivity or resolution on the analysis [4]. Integration of microfluidic channels and electrical components together on a single chip is called Lab-on-Chip (LoC) concept, and it receives significant interest from the scientific community. Miniaturized, high throughput and low-cost LoC concepts are extensively in use for the chemical and biological sample analysis [5], [6].

These microchannel structures in LoC systems help to increase the functionality and provide the miniaturization due to their smaller sizes and possibility for bringing electrical and fluidic interfaces together [7]. Different LoC concepts have been demonstrated, which have mostly polymer based microfluidic channels [8]–[10] to combine fluidics and electronics together.

Typically poly-dimethyl-siloxane (PDMS) [11] is etched and bonded with the help of oxygen plasma [12] or directly molded [13] on to Si circuit chips, in order to create microfluidic channels. Although these methods are fast and cost effective, the yield and the chemical stability against solvents which can be used in the microfluidic channels are the main drawbacks limiting the applications. Furthermore, the dimensions of the channels structured in these polymers are larger with respect to the structures which are available in standard CMOS/BiCMOS technologies. The relatively big sizes of microchannels with polymers make it difficult to further miniaturize the LoC systems [14]. Additionally, due to limited mechanical stability of the polymeric microchannels; a full-wafer integration process is very challenging. Therefore, there is a need to improve yield and cost while having stable and reliable microfluidic technologies.

In this study, the integration of a microfluidic technology into a high-performance SiGe BiCMOS process for LoCs is presented. The proposed method is consisting of 200 mm wafer bonding and de-bonding techniques which include high throughput and industrialized semiconductor processes. A transparent glass is used to allow optical observation. The combination of a high-performance BiCMOS technology and microfluidic channels together on a single chip decreases the distances between the sample, the sensor and the read-out integrated circuit (ROIC) thus enabling high sensitivity and high throughput while decreasing the form factor. Hence, integrating microfluidic and BiCMOS technologies together can meet the requirement of fast, reliable and low-cost LoC systems.

II. Microfluidic Packaging

A. Technology Development

The proposed microfluidic packaging technology is based on a 3-wafer-stack which is developed by using 200 mm wafer bonding technologies. The BiCMOS and the microfluidic wafer are integrated together by the wafer bonding of the silicon and the glass wafer as seen in Figure 1. In this method, there are two wafer bonding steps: the first bonding is realized between the BiCMOS and the channel wafer, and the second bonding is done in between the already bonded wafer stack

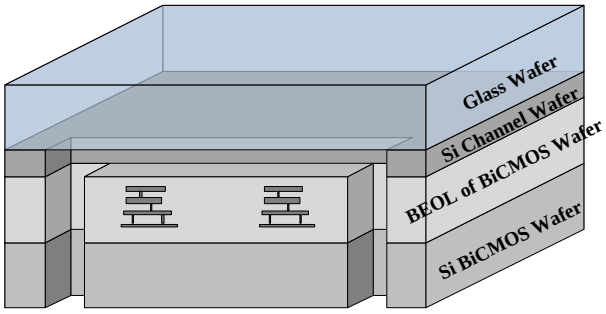

Fig. 1: 3D representation of the microfluidic channel packaging

together with the glass wafer. Therefore the complete stack consists of the BiCMOS wafer, the Si channel wafer and the glass wafer.

The BiCMOS wafer provides the sensors within the back end of line (BEOL), the active circuitry as well as all the electrical connections. It is realized using the available BiCMOS fabrication steps. In order to functionalize the electrical components on the LoC system, the microfluidic structure has to interact with the sensors while having no interruptions to the electrical system. A Si channel wafer is bonded on top of the BEOL oxide of the BiCMOS wafer to realize the microfluidic channels.

The channel wafer etched to have the microfluidic channel structures which will be on the bonding interface. Because of these structures are on the separate wafer rather than BiCMOS wafer, it is easier to construct the channel networks. The length and the width of the microfluidic channel structures are etched into the Si wafer and only minimum restrictions in terms of microfluidic channel dimensions and shapes are presents. The height of the channels is controlled by two different factors: the etching depth and the backside grinding of the wafer. After the wafer bonding, the height of the channels are well-controlled by the grinding process. However the surface roughness after the grinding is required to be low to be able to integrate the glass wafer to this stack therefore a polishing using a polygrind step is applied.

The glass wafer is the top wafer on the 3-wafer-stack. The reason that a glass wafer is being used is the transparency of the glass itself. Consequently, this wafer enables to have simultaneous optical investigations and at the same time electrical sensing and measurements can be realized.

B. Wafer Integration

The integration of the 3-wafer-stack can be seen in Figure 2. The standard 200 mm BiCMOS wafer is fabricated starting with a bare Si substrate as in Figure 2.a and b. Later, the microfluidic inlet and the outlet are opened from the backside of the BiCMOS wafer. Before the first integration, the status of the BiCMOS wafer with the microfluidic inlet and the outlet can be seen in Figure 2.c.

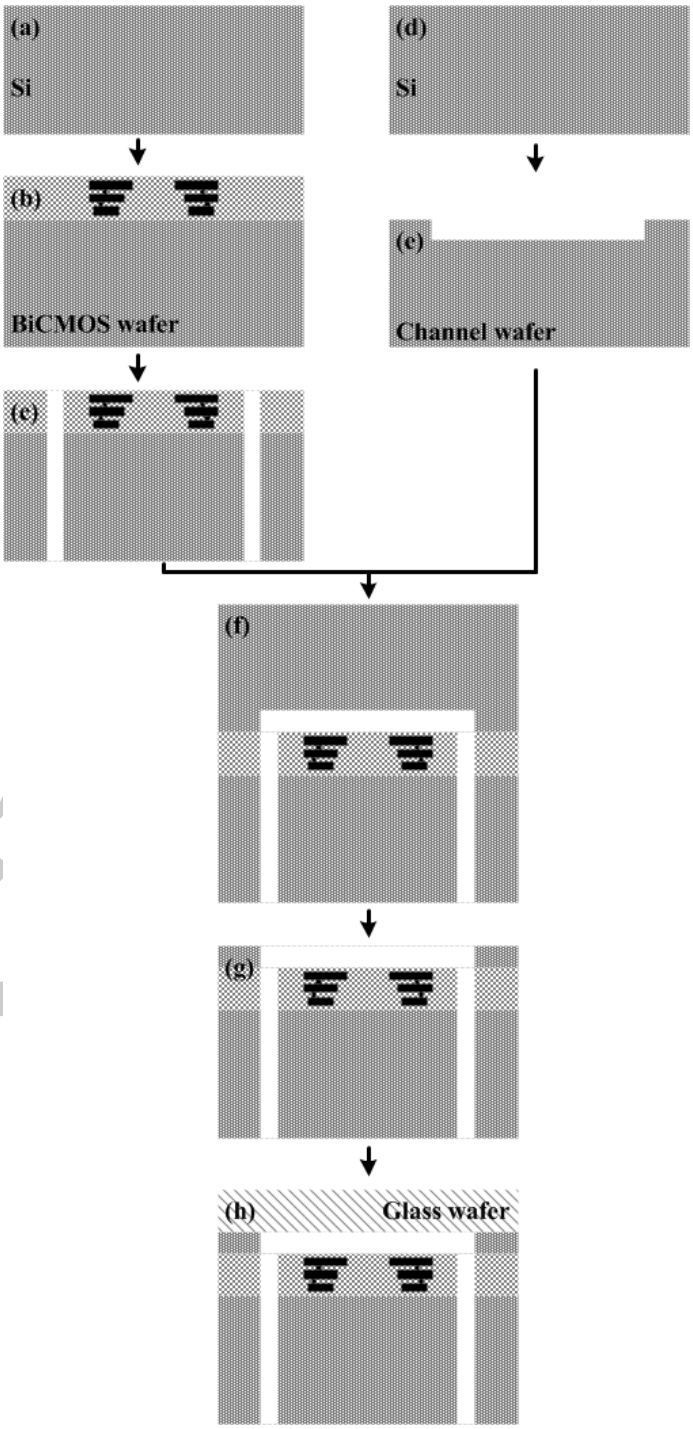

Fig. 2: Schemetical presentation of the microfluidic packaging (a) Bare 200 mm Si wafer for standart BiCMOS fabrication (b) Finished BiCMOS wafer including the sensors within the BEOL oxide (c) Through Si holes for the microfluidic inlet and the outlet (d) Bare Si wafer for the microfluidic channels (e) Etched microfluidic structure on the Si wafer (f) Bonded wafer stack: the BiCMOS and the channel wafer (g) Bonded wafer stack grinded from backside (h) Final 3-wafer stack with the glass wafer on top

Firstly, the silicon based microfluidic channel wafer is structured and etched to realize the channels (Figure 2.d and e). After that, the first bonding is performed between the front side of the BiCMOS wafer with the integrated sensors and the silicon based microfluidic channel wafer. A cross section of the wafer stack after the bonding can be seen in Figure 2.f. Plasma assisted oxide-oxide fusion bonding at 300 °C under a bond force of 1.5 kN is applied in order to achieve high quality and leakage free interfaces. Additionally, plasma assisted bonding enables to achieve high bonding quality at lower temperatures, which allows staying within the thermal budget of the BiCMOS processes. The micro-roughness of the surfaces of both wafers has to be lower than 0.5 nm in order to achieve a good oxide-oxide fusion bonding quality. To achieve this roughness, chemical mechanical polishing (CMP) is used.

After the bonding, the height of the microfluidic channel is adjusted by a grinding process from the backside. Channel heights of 30 μm to 100 μm are realized with minimum distance of 30 μm between the different channels. A cross section of the system after the grinding can be seen in the Figure 2.g. The minimum alignment accuracy of less than 1 μm is achieved between the BiCMOS wafer and the silicon microfluidic channel wafer by using a smart view aligner (*EVG-SmartView NT2®*).

The second wafer bonding is applied on the backside of the engineered channel wafer and the glass wafer. The roughness of the backside grinded wafer is well above the fusion bonding requirement. An adhesive bonding is performed to finalize the structure at the last step. A 30 μm thick adhesive is laid on the glass wafer by spin coating and then the wafer is bonded with the stack. The bonding occurred at 200 °C, which is still below the temperature restrictions. In the end, a 3-wafer stack is completed which consists of the BiCMOS wafer at the bottom, the microfluidic channel wafer in the middle and the glass wafer on top which can be seen in Figure 2.h.

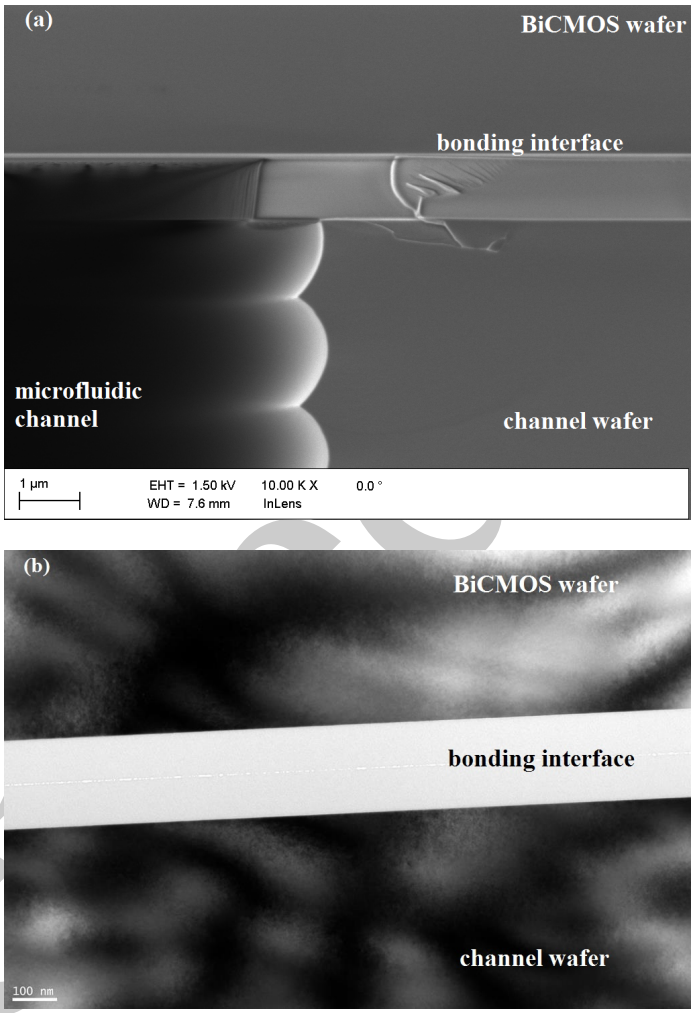

Fig. 3: Oxide-oxide bonding interface between the BiCMOS wafer and the channel wafer (a) SEM image of the interface (b) TEM image of the interface

III. Experimental Results

A. Wafer Bonding

The 3-wafer-stack LoC system requires high quality oxide-oxide fusion bonding. In the first bonding step, the wafers are bonded in a way that there will be no leakage from the microfluidic channels, which are formed at the bonding interface. In Figure 3.a, SEM image on the bonding interface between the BiCMOS wafer and the channel wafer can be seen. In the same figure, it is visible that the bonding is successful and there is no change in the channel structures.

Additionally, in Figure 3.b, TEM image of the bonding interface clearly shows that there are no visible voids in the interface after the fusion bonding. This proofs that while having fluids in the channels, there will be no leakage. In this sense, the bonding quality is suitable for microfluidics in LoC applications.

After achieving the high quality bonding, the next step is achieving the channel integration to the BiCMOS wafer. To do this, the Si wafer with microfluidic structure is bonded to the BiCMOS wafer. In Figure 4.a, the bonded stack of the BiCMOS wafer and the channel wafer can be seen after the backside grinding of the channel wafer. Since the bonding quality is high at the interface, the structures are transferred to the BiCMOS wafer after the grinding.

Mechanical grinding enables to control the height of the microfluidic channels. Due to the process variations, the channel structure sizes can differ. For example in Figure 4.b, it is clearly seen that the depths of the etching of the channel structures are different which is related to the aspect ratio dependent etch rate. The channel wafer is grinded down to adjust the channel heights as well as bringing out the channel structures to outside. However after the grinding, the surface roughness of the channel wafer is too high for next bonding for capping the channels with the glass wafer. In Figure 5, an AFM surface scan of the backside of the channel wafer can be seen. The wafer surface roughness on the scanned area is around 4.7 nm, which is extremely above the required roughness of 0.5 nm.

When the surfaces are ready for the next bonding, the glass

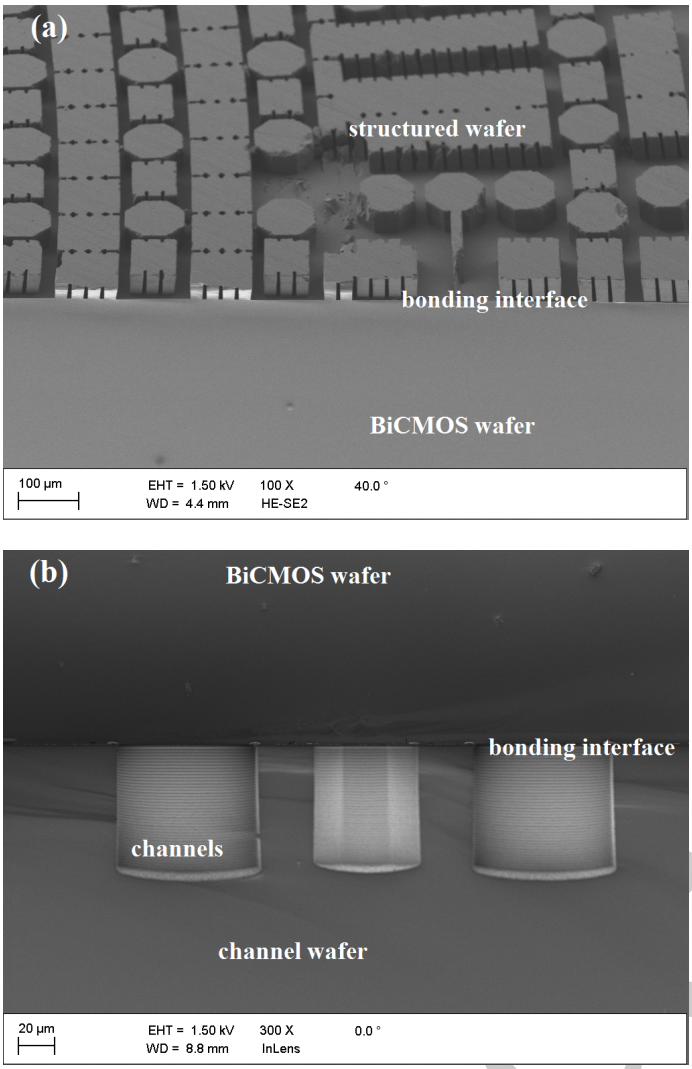

Fig. 4: Channel formation on the bonding interface (a) SEM image of the structured Si wafer bonded on the BiCMOS wafer after the backside grinding. (b) Cross-section SEM image of the channel on the bonding interface.

wafer is bonded to the grinded channel wafer by an adhesive. The channels are visible from the top view due to the grinding of the excess Si on the channel wafer. In Figure 6, the 3-wafer stack can be seen after the glass wafer bonding. In this stack, it is possible to observe inside the channel by looking from the glass wafer side.

B. Microfluidic LoC

After the successful demonstration of the 3-wafer-stack by 200 mm wafer bonding techniques, the integration of different types of passive sensors is required to realize a fully integrated LoC system. In Figure 7, the 200 mm processed BiCMOS and the channel wafer can be seen. The sensors on the BiCMOS wafer have to be aligned with the channel structures on the channel wafer. By the inlet and outlet opening from the backside of the channel wafer, it is possible to have

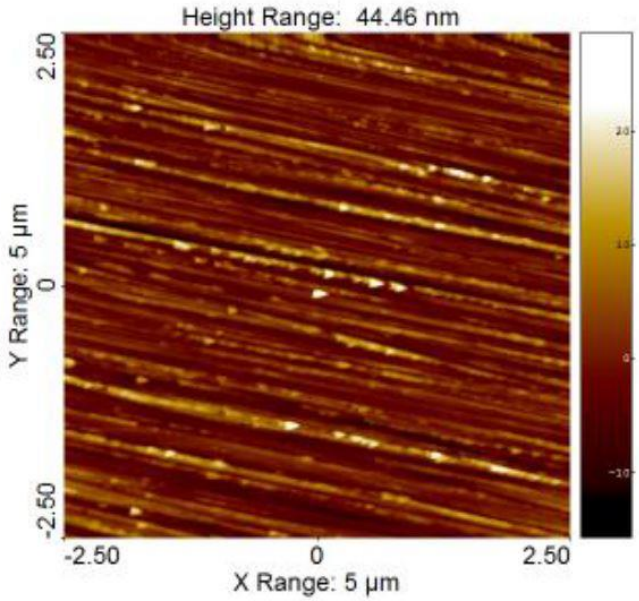

Fig. 5: AFM image of the surface after grinding

Fig. 6: 3-wafer-stack after glass wafer bonding, channel structures are visible on image.

a microfluidic interface from wafer backside thus enabling electrical and optical measurements from the front side of the system. In the Figure 7, the inlet and outlet are highlighted by illumination from backside of the wafer.

Through Si holes from the backside of the BiCMOS wafer enables to have microfluidic interface on the backside of the system. In Figure 8.a, the sensors located inside the microfluidic channel can be seen. It is possible to make electrical measurements while the chemical and biological samples are

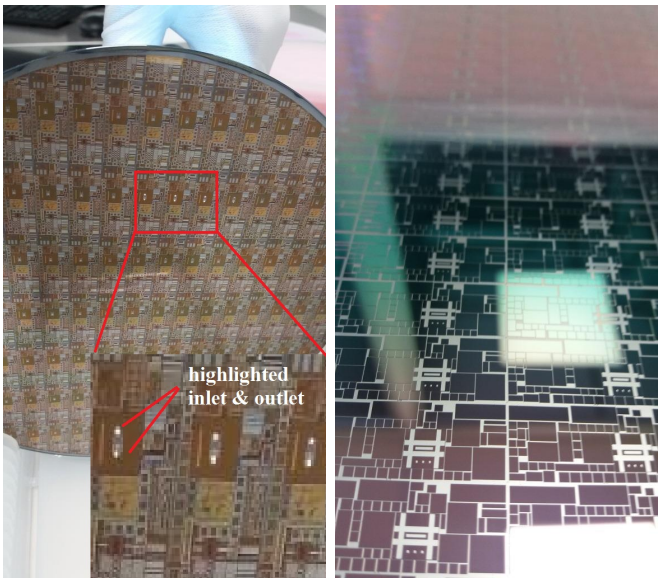

Fig. 7: Microfluidic packaging for LoC aplications (the BiCMOS wafer including highlighted inlets and outlets (*left*) and the channel wafer (*right*) before integration)

placed on top of these sensors. The inlet of the microfluidics into the LoC system is visible in the microscope image in Figure 8.b. After capping these channels with the glass wafer and dicing of the required chip sizes, the LoC fabrication is finished. In Figure 8.c, the cross section of the LoC system can be seen. The sensors are located in the microfluidic channel.

IV. Conclusion

A wafer level integration of a flexible microfluidic technology into a BiCMOS process is demonstrated. The integration includes fusion and adhesive wafer bonding steps to combine a BiCMOS wafer, a silicon microfluidic channel wafer and a transparent glass capping wafer. Flexible dimensions of microchannels are achieved with an alignment accuracy of less than 1 μm. The developed wafer level integration technique allows not only simultaneous, optical and electrical measurements which are highly desired by the bio and medical community but also provides an emerging platform for medium and high volume bio applications.

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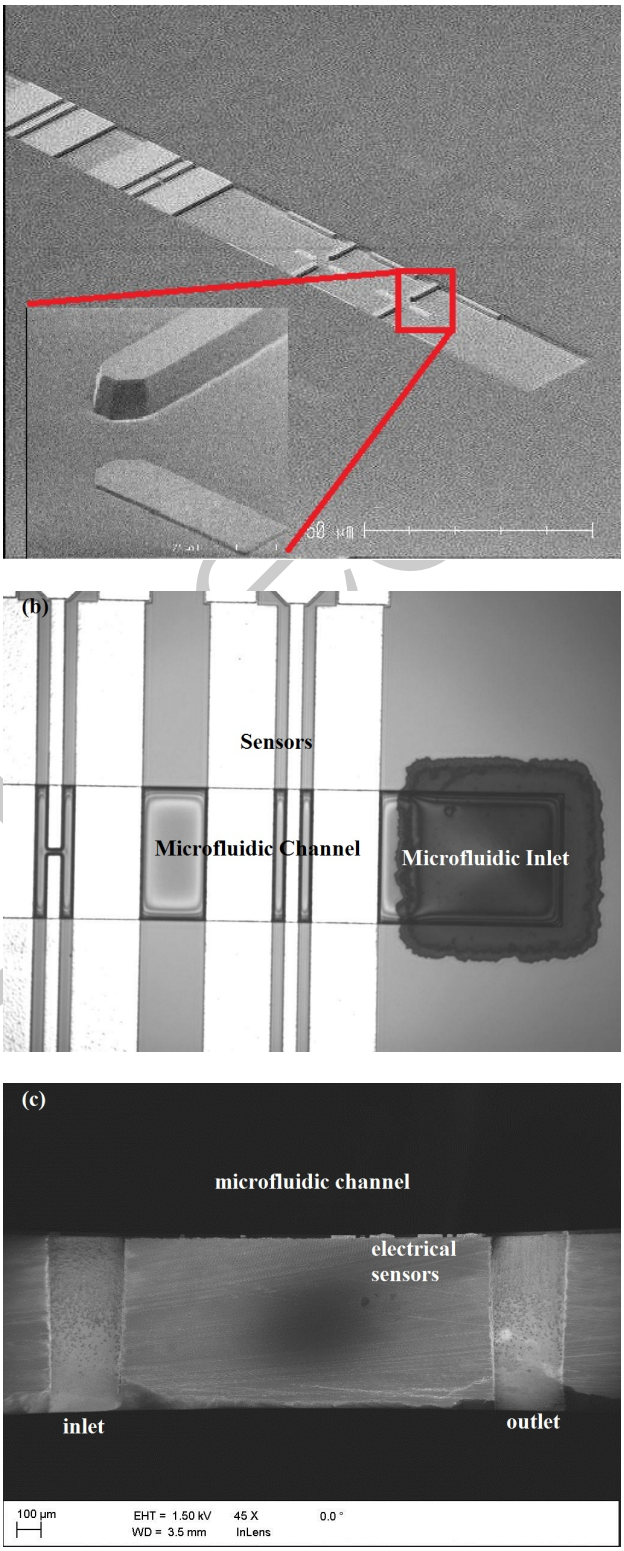

Fig. 8: Integrated microfluidic channels with sensors (a) SEM image of the sensors in the microfluidic channel (b) Top view of the channel showing the inlet of the microfluidic channel. (c) Cross-section SEM image of the system, including inlet, outlet and electrical sensors.

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