World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:11, No:12, 2017

A Study on ESD Protection Circuit Applying Silicon Controlled Rectifier-Based Stack Technology with High Holding Voltage

Hee-Guk Chae, Bo-Bae Song, Kyoung-Il Do, Jeong-Yun Seo, Yong-Seo Koo

***Abstract*—**In this study, an improved Electrostatic Discharge (ESD) protection circuit with low trigger voltage and high holding voltage is proposed. ESD has become a serious problem in the semiconductor process because the semiconductor density has become very high these days. Therefore, much research has been done to prevent ESD. The proposed circuit is a stacked structure of the new unit structure combined by the Zener Triggering (SCR ZTSCR) and the High Holding Voltage SCR (HHVSCR). The simulation results show that the proposed circuit has low trigger voltage and high holding voltage. And the stack technology is applied to adjust the various operating voltage. As the results, the holding voltage is 7.7 V for 2-stack and 10.7 V for 3-stack.

***Keywords*—**ESD, SCR, latch-up, power clamp, holding voltage.

I. Introduction

As the device process technology has advanced, the ESD protection circuit is considered as a critical component due to the integrated circuit (IC) failures caused by the heat dissipation [1]. To protect the ICs from the ESD phenomena, the Gate Grounded NMOS (GGNMOS) has mainly been used as an ESD protection circuit. The GGNMOS, however, has the large area and the low current driving capability. It causes a limitation to operating frequency and impedance matching of input-output [2]. On the contrary, Silicon controlled Rectifier (SCR), the other well-known ESD protection circuit, has the high current driving capability and the low area compared to the GGNMOS. It is caused by the positive feedback of the parasitic NPN/PNP bipolar transistors. But the SCR has a trigger voltage of about 20 V and a low holding voltage of about 2 V. The electrical characteristics are vulnerable to the latch-up problem [3]. The latch-up is possible to prevent by the much higher holding voltage. Normally, the holding voltage is only varied by the structural modification [4]-[7].

This paper proposed a stacked circuit with high holding voltage and low trigger voltage. The proposed device is also stacked to get the several fold electrical properties. The simulation was conducted by Synopsys T-CAD simulator.

Hee-guk Chae, Bo-bae Song, Kyoung-il Do, Jeong-yun Seo are with the Department of Electronics & Electrical Engineering University of Dankook, 126 Jukjeon-dong, Suji-gu, Yongin-si, Gyeonggi-do, 448-701, Korea.

Yong-Seo Koo is with the Department of Electronics & Electrical Engineering University of Dankook, 126 Jukjeon-dong, Suji-gu, Yongin-si, Gyeonggi-do, 448-701, Korea (corresponding author, e-mail: yskoo@dankook.ac.kr).

II. Proposed SCR-Based ESD Protection Circuits

A. The Proposed ESD Protection Circuit

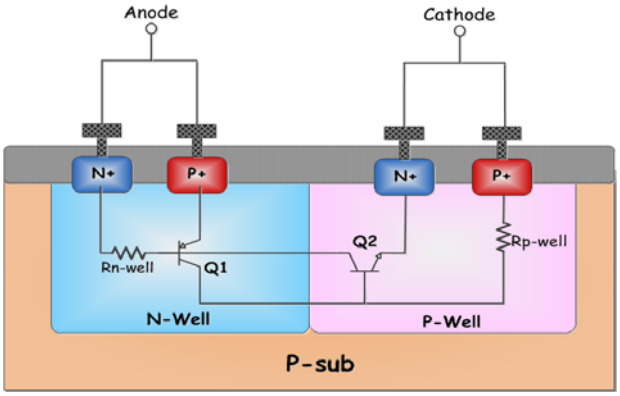

Fig. 1 A cross section view of conventional SCR

The simple conventional SCR structure is shown in Fig. 1. It consists of the N/P wells and the four diffusion regions. The operation principle of the conventional SCR is as follows.

The ESD pulse flowing into the anode raises the N-well potential through the N+ diffusion region. At the time, as the P-well is grounded, the P-well and the N-well are reversely biased. Then, the potential at the junction region between wells is steadily increased, and when the potential exceeds the avalanche breakdown criteria, the Electron-Hole Pairs (EHPs) are generated by the breakdown phenomenon. The generated holes flow into the P+ diffusion region connected to the cathode through the P-well. As it is in process, the hole current increases the potential of the P-well. When the P-well potential is higher than the built-in potential between the P-well and the N+ diffusion region on the P-well, the junction forms the forward biasing at the edge of the N+ diffusion region. Then, as a result, the parasitic lateral NPN BJT turns on and forms the discharge path of the electron current. Then, the piled potential at the N-well flows into the cathode and the potential is being decreased. At the same time, the junction between the N-well and the P+ diffusion region forms forward biasing. It leads to turn on the parasitic lateral PNP BJT, while the base current is being caught by the parasitic lateral NPN BJT. The turn on of the PNP BJT causes the increased base current of the NPN BJT, and on the same principle the base current of the PNP BJT is also increased. That is called as “positive feedback”. The positive feedback forms a high-current discharge path and consequently the ESD current discharge rapidly. Therefore, the

SCR can rapidly discharge the currents to the cathode.

The SCR has the structural feature that avalanche breakdown occurs in wide junction region between wells under the surfaces. So, it has a high trigger voltage of about 19V. Also, the holding voltage, which is mainly influenced by the total length and the N-well resistance, is too low to avoid the latch-up [8]. Due to the two electrical properties, the SCR is difficult to design for the ESD protection circuit [9]-[13].

The reasons are as follows. At first, the high trigger voltage has the possibility to cause the damage to the core IC before the protection circuit is triggered under the ESD conditions. Secondly, the holding voltage is too low to prevent the latch-up problem. The holding voltage lower than the operating voltage of the core IC can cause the not-turning-off after discharging the ESD current. Such a latch-up could induce the leakage current and the noise to the input signal. Therefore, the SCRs are not mainly used as the ESD protection circuit in the ICs.

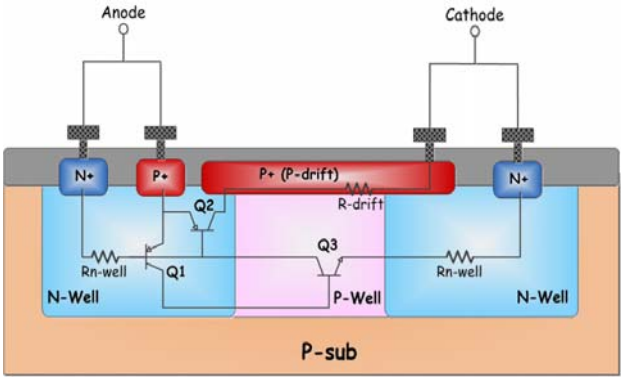

Fig. 2 The cross-sectional view of High Holding Voltage SCR (HHVSCR)

Fig. 2 shows a HHVSCR (High Holding Voltage SCR) structure, which is improved from the conventional SCR structure. The structure has the P-drift region on the middle. The operation mechanism of the HHVSCR has the one more parasitic PNP BJT operating on the surface of the P-well. The PNP BJT has the longer base region than the internal PNP BJT. The longer base region leads to decrease the emitter injection efficiency resulting in reducing the gain (β). Thus, the proposed circuit has the high holding voltage.

Fig. 3 shows the structure of a Zener Triggering SCR (ZTSCR) with the more improved electrical properties than the HHVSCR. The structural feature of the proposed circuit is the N+ bridge region combined with the P-drift region on the P-Well. The trigger voltage can be much lowered by the breakdown at the highly doped region. Therefore, the proposed circuit has the high holding voltage and the operating principle similar to the SCR due to being based on the HHVSCR. The two circuits have the high holding voltage, which prevents the latch-up. Then, the stack technology, which connects with the same structure sequentially by the previous cathode to the next anode, is applied [14]. The technology is used to take the same advantage of the unit structure though the stack number is increased. By using the stack technology, we proposed the new circuit, which can get the good electrical properties with the trigger voltage and high holding voltage.

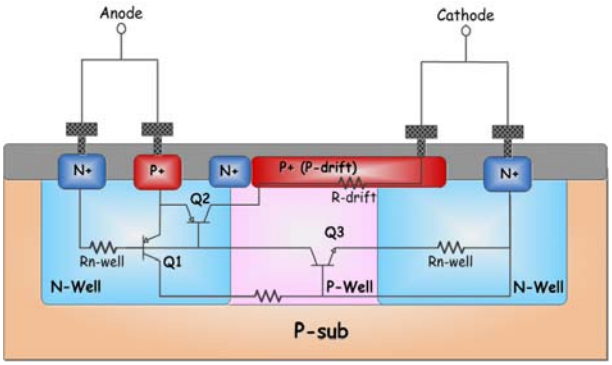

Fig. 3 A cross-sectional view of ZTSCR (Zener Triggering SCR)

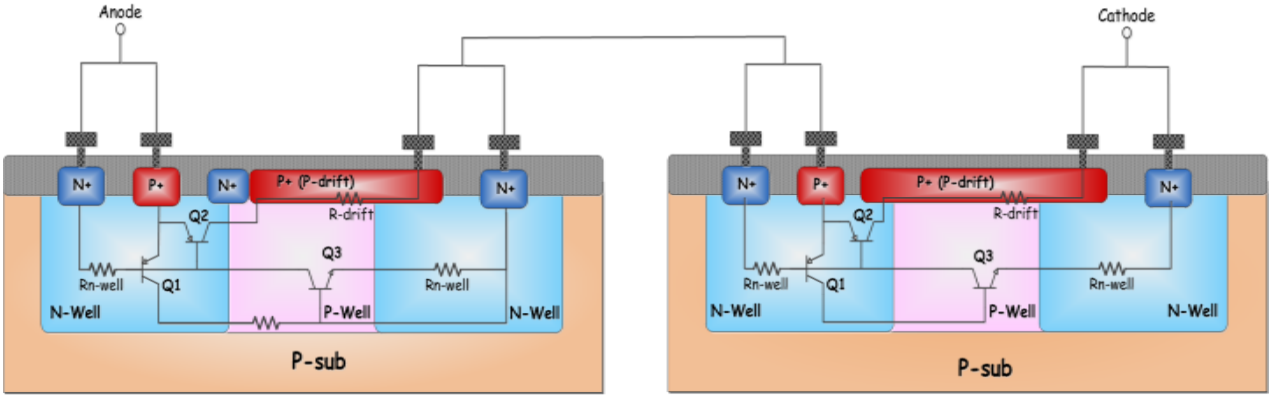

Fig. 4 A cross-sectional view of the proposed ESD protection circuit

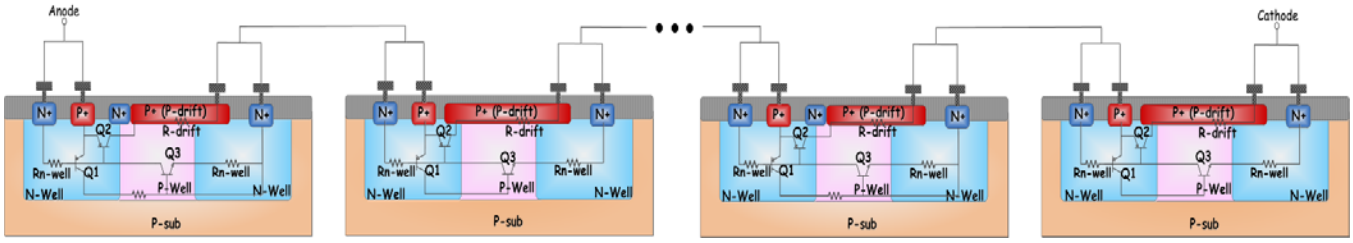

Fig. 5 A cross section view of the proposed ESD protection circuit applying the stacking technology

In comparison with the structures, the SCR has the too high trigger voltage and the too low holding voltage to apply the stack technology. For ZTSCR, the trigger voltage is too low. As the stack technology is not ideal method, the stacked ZTSCR can get the lower trigger voltage than the holding voltage, which means the design failure. For HHVSCR, the holding voltage is high enough to avoid the design failures, but the robustness of the HHVSCR can be definitely decreased due to the much higher resistance increase at the drift region. Therefore, in this paper, the newly proposed circuit is used to apply the stack technology for the better electrical characteristics. Fig. 4 shows the newly proposed circuit. The proposed circuit has lower trigger voltage and higher holding voltage than the conventional SCR.

Fig. 5 shows the proposed with applying the stack technology. The structure operates by the ZTSCR operation, and has the very high holding voltage by connecting the two structures.

III. Simulation Result

A. Analysis of the Proposed ESD Protection Circuit by T-CAD

The simulation was conducted using synopsys' T-CAD tool to analyze the electrical characteristics. To get the stacked I-V characteristics, the simulations was performed in a mixed mode. The simulated I-V characteristics of ZTSCR and HHVSCR, which is the each single component of the proposed circuits, are shown in Figs. 6 and 7. The numerical values are arranged in Table I.

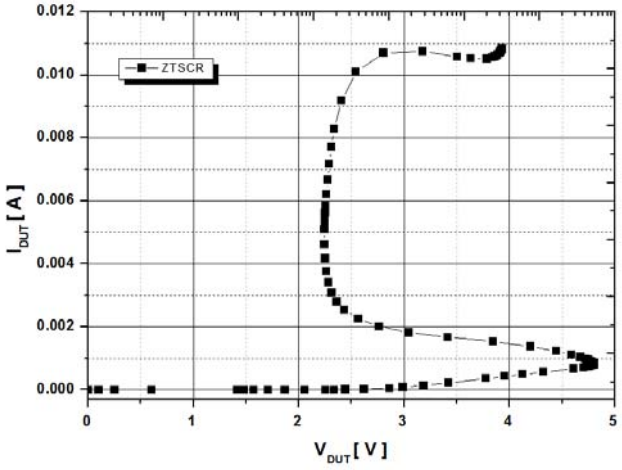

Fig. 6 I-V Characteristics curve of the ZTSCR

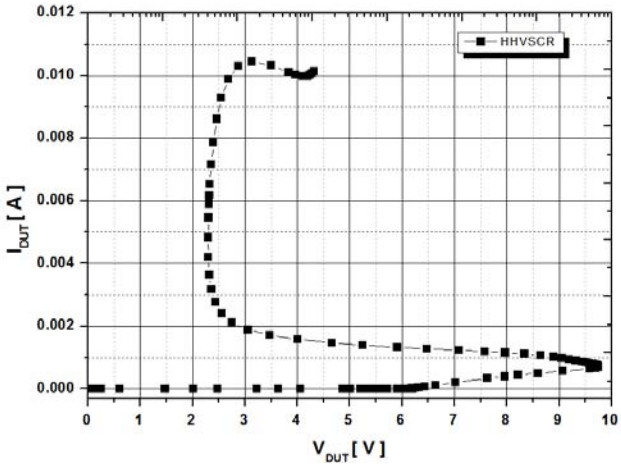

Fig. 7 I-V Characteristics curve of the HHVSCR

TABLE I
Trigger Voltage and Holding Voltage of ZTSCR and HHVSCR

Circuit	Trigger Voltage(Vt)	Holding Voltage(Vh)
ZTSCR	4.7 V	2.2 V
HHVSCR	9.7 V	2.3 V

The simulation results show that the ZTSCR has the trigger voltage of 4.7 V and the holding voltage of 2.2 V, and the HHVSCR has the trigger voltage of 9.7 V and the holding voltage of 2.3 V. The results show that the two structures have the high holding voltages. Fig. 8 and Table II show the simulation results of the electrical characteristics of the conventional SCR and the proposed circuit.

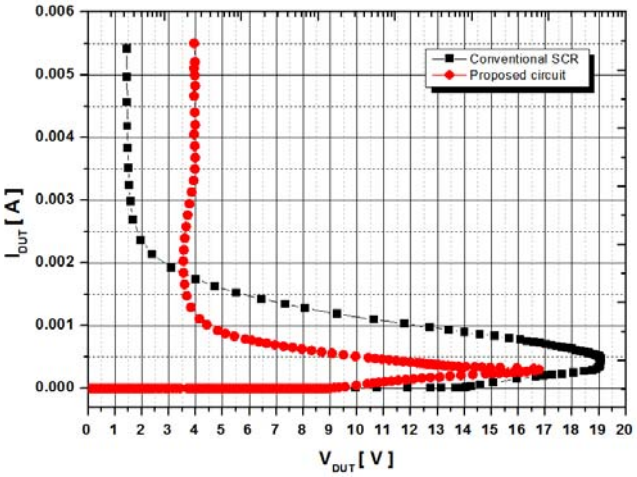

Fig. 8 I-V Characteristics curve of the proposed circuit and SCR

TABLE II
TRIGGER VOLTAGE AND HOLDING VOLTAGE OF PROPOSED CIRCUIT AND SCR

Circuit	Trigger Voltage(Vt)	Holding Voltage(Vh)
Conventional SCR	19.1 V	1.4 V
Proposed Circuit	16.7 V	3.5 V

Compared to the conventional SCR, the proposed circuit has the lower trigger voltage of 16.7V and the much higher holding voltage of 3.5 V than the SCR. Fig. 9 shows the simulation results of the electrical characteristics as the stack number is increased.

TABLE III
TRIGGER VOLTAGE AND HOLDING VOLTAGE OF STACKED STRUCTURE OF PROPOSED CIRCUIT

Circuit	Trigger Voltage (Vt)	Holding Voltage (Vh)
Proposed Circuit	16.7 V	3.5 V
2-Stack Proposed Circuit	33.5 V	7.7 V
3-Stack Proposed Circuit	50.1 V	10.7 V

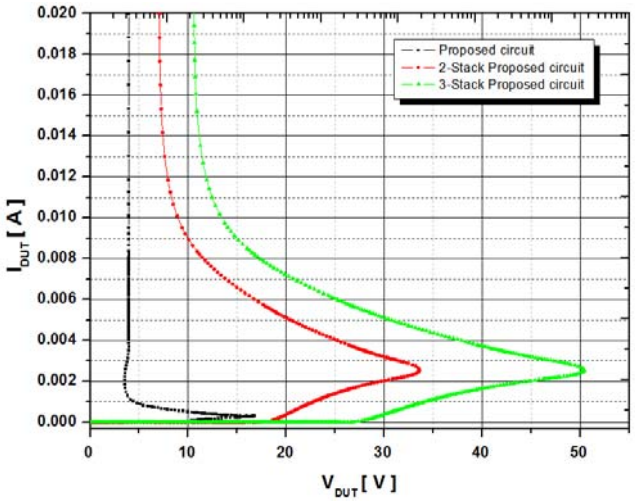

Fig. 9 I-V Characteristics curve of the structure with the proposed circuit stacked

The simulation results show that the 2-stack structure of the proposed circuit has the trigger voltage of 33.5 V and the holding voltage of 7.7 V. And the 3-stack structure has a trigger voltage of 50.1V and a holding voltage of 10.7 V. Thus, using the stack technology, the proposed circuit has the several-fold electrical properties.

IV. CONCLUSION

This paper proposed a new ESD protection circuit to protect internal ICs from the ESD events. The proposed circuit has the low trigger voltage and the high holding voltage. The simulation results show that the proposed circuit has a lower trigger voltage of 16.7 V and a higher holding voltage of 3.5 V than the conventional SCR. Also, the stack technology is used to get the several-fold electrical properties. The stacking simulation results show that the 2-Stack has the 33.5 V trigger voltage and the 7.7 V holding voltage, and for the 3-Stack, the trigger voltage of 50.1 V and the holding voltage of 10.7 V. Therefore, the proposed circuit has the better electrical properties than the conventional SCR.

ACKNOWLEDGMENT

This work was supported by the Development of Futuristic fusion-semiconductor core IP(10052009) and the Ministry of Trade, Industry & Energy (10065137, "Boosted Class-DG Audio Power Amplifier with Embedded ADC for Mobile Speaker Protection").

REFERENCES

[1] Albert Z, H. Wang, *On-Chip ESD Protection for Integrated devices* 2nd ed. Springer, US, 2002.
[2] M.D. Ker and C.C. Yen "investigation and Design of on-Chip Power-Rail ESD Clamp Circuits without Suffering Latch up-Like Failure during System-Level ESD Test" *IEEE J, Solid-State Circuit,* vol. 43, no. 11, pp.2533-2545, 2008.
[3] V. Vashchenko, A. Sinkevitch, V.F., "Physical Limitaions of Semiconductor Devices, *Springer*, p.340, 2008
[4] Yong Seo Koo, et. al., "Design of SCR-based ESD protection device for power clamp using deep-submicron CMOS technology," *Microelectronics Journal*, Vol. 40, pp. 1007-1012, 2009.
[5] Sheng-Lyang Jang, et. al., "Temperature-dependent dynamic triggering characteristics of SCR-type ESD protection devices," *Solid-State Electronics*, Vol.45, pp. 2005-2009, 2001.
[6] P.-Y Ran, M. Indrajjit, P.-H. Li and S. H. Voldman. "RC-triggered PNP and NPN Simultaneously Switched Silicon Controlled Rectrifier ESD Networks for Sub-0.18um Technology" in proc. Of IEEE int. symp. On physical and failure Analysis of Intergrated Circuits, pp. 71-75, 2005
[7] W.Y Chen, et. al., "Measurement on Snapback Holding voltage of High-Voltage LDMOS for Latch-up Consideration," *device and system, APCCAS 2008*, pp. 61-64, 2008.
[8] J. Y. Lee "Analysis of SCR, MVSCR, LVTSCR With I-V Characteristic and Turn-On-Time," j.inst.Korean.electr.electron.eng, vol. 20, no. 3, pp. 295-398, 2016.
[9] O. Quittard, Z. Mrcarica, F. Blanc, G. Notermans, T. Smedes, and H.van Zwol, "ESD protection for high-voltage CMOS technologies," EOS/ESD Symp, pp. 77-86, 2006.
[10] K. D Kim "A Study on the Novel SCR Nano ESD Protection Device Design and Fabrication," j.inst.Korean.electr.electron.eng, vol. 9, no. 2, pp. 83-91, 2005.
[11] M. D. Ker and H. H. Chang, "How to safely apply the LVTSCR for CMOS whole-chip ESD protection without being accidentally triggered on," J. Electro- statics, vol. 47, pp.215-248, 1999.
[12] Y. Koo, K. Lee, K. Kim, and J. Kwon, "Design of SCR-based ESD protection device for power clamp using deep-submicron CMOS technology," Microelectronics Journal, vol. 40, pp. 1007-1012, 2009.
[13] S.-L. Jang, L.-S. Lin, and S.-H. Li, "Temperature-dependent dynamic trig-gering characteristics of SCR-type ESD protection circuits," Solid-State Electronics, vol. 45, pp. 2005-2009, 2001.
[14] V. A. Vashchenko, A. Concannon, M. ter Beek, and P. Hopper "High Holding Voltage Cascoded LVTSCR Structures for 5.5-V Tolerant ESD Protection Clamps," IEEE Transactions on Device and Materials Reliability, vol. 4, no. 2, pp. 273-280, 2004.