Design of a CMOS Differential Operational Transresistance Amplifier in 90 nm CMOS Technology

Hafiz Muhammad Obaid, Umais Tayyab, Shabbir Majeed Ch.

Abstract—In this paper, a CMOS differential operational transresistance amplifier (OTRA) is presented. The amplifier is designed and implemented in a standard umc90-nm CMOS technology. The differential OTRA provides wider bandwidth at high gain. It also shows much better rise and fall time and exhibits a very good input current dynamic range of -50 to 50 µA. The OTRA can be used in many analog VLSI applications. The presented amplifier has high gain bandwidth product of 617.6 THz Ω. The total power dissipation of the presented amplifier is also very low and it is 0.21 mW.

Keywords—CMOS, differential, operational transresistance amplifier, OTRA, 90 nm, VLSI.

I. INTRODUCTION

THE OTRA is generally used in analog VLSI applications. In the past, a great interest has been devoted to the design of the OTRAs [1]-[4]. The bandwidth of a traditional operational amplifier is dependent on the closed loop voltage gain. On the other hand, OTRA is not slew limited like voltage op-amps. It can provide a high bandwidth which is independent of the gain. As a result, it does not suffer from constant gain-bandwidth product as in voltage op-amp circuits [5].

The block diagram of the OTRA is shown in Fig. 1. It is a three terminal analog building block that is defined by the following matrix equation [1]:

$$\begin{bmatrix} V_+ \\ V_- \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_0 \end{bmatrix} \tag{1}$$

where R_m is the transresistance gain.

In the block diagram of the OTRA, the input terminals are virtually grounded, leading to circuits that are insensitive to stray capacitance [6], [7]. The output voltage is the difference of the two input currents multiplied by transresistance R_m. Ideally, the transresistance gain R_m approaches infinity and both the input and output terminals are characterized by low

Hafiz Muhammad Obaid is with the Department of Electrical Engineering, University of Lahore, Lahore, Pakistan (corresponding author, phone: +92-313-5361020; e-mail: muhammad.obaid@ ee.uol.edu.pk).

Umais Tayyab is with the Department of Electrical Engineering, King Fahd University of Petroleum and Minerals, KSA (e-mail: g20140494@kfupm.edu.sa).

Shabbir Majeed Ch is with the Department of Electrical Engineering, University of Engineering and Technology Taxila, Taxila, Pakistan (e-mail: shabbir.majeed@uettaxila.edu.pk).

impedance. The transresistance gain R_m will apply external negative feedback which force the two input currents I_+ *and* I_- to be equal.
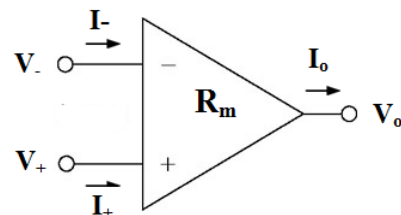

Fig. 1 Block diagram of the OTRA

II. BASIC CONCEPTS

The simplified traditional circuit of an OTRA is shown in Fig. 2. If channel length modulation factor λ and the transconductance parameter β of the PMOS transistors are equal to those of NMOS transistors and if all current mirrors have bias current I_{bias}, then the transresistance R_m is given by [3],

$$R_m = \frac{1}{2\lambda I_{bias}} \tag{2}$$

Suppose, all current mirrors are cascode current mirrors, then R_m is given as [8],

$$R_m = \frac{(0.5\beta I_{bias})^2}{(\lambda I_{bias})^2} \tag{3}$$

The traditional amplifier shown in Fig. 2 is connected as a non-inverting amplifier, as shown in Fig. 3. The voltage gain is given as

$$\frac{V_0}{V_{in}} = \frac{R_m\left(\frac{1}{z_1}\right)}{1+R_m\left(\frac{1}{z_2}\right)} \tag{4}$$

If $R_m\left(\frac{1}{z_2}\right)$ is much greater than 1, then the voltage gain is equal to z_2/z_1, which is the ideal voltage gain G. If R_m is represented as P(s)/Q(s), then (3) can be written as [3],

$$\frac{V_0}{V_{in}} = G\frac{P(s)}{P(s)+z_2 Q(s)} \tag{5}$$

In order for the poles and zeros of the voltage gain to be the same, z_2 must remain same. So, the bandwidth of this circuit is

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
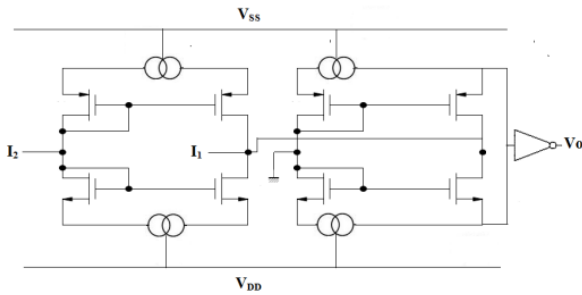Vol:11, No:6, 2017

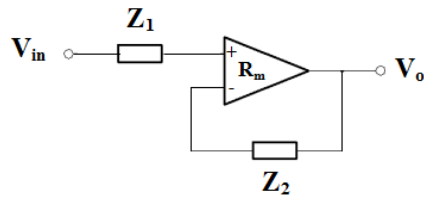a constant.

Fig. 2 Traditional circuit of an OTRA

Fig. 3 Noninverting amplifier

An inverting amplifier is shown in Fig. 4. Its voltage gain is given as,

$$\frac{V_0}{V_{in}} = -\frac{R_m\left(\frac{1}{z_1}\right)}{1+R_m\left(\frac{1}{z_2}\right)} \qquad (6)$$

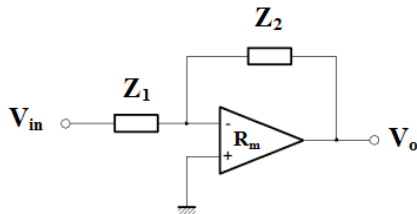Its bandwidth is also independent of the voltage gain.

Fig. 4 Inverting amplifier

III. THE PROPOSED DIFFERENTIAL OTRA

The schematic diagram of the circuit we propose in this paper is shown in Fig. 5. In the proposed high open loop gain differential OTRA, a differential gain stage is used. This low power wide band OTRA is based on a common source amplifier [4] and the cascaded connection of the modified differential current conveyor (MDCC) [6]. The transistors M12-M15 produce the inverting output and the transistors M9-M11 produce the non-inverting output. In the proposed schematic, the DC offset current is reduced and the DC open loop transresistance gain is increased due the addition of the differential gain stage.

If we assume that all the transistors are operating in the saturation region, then the current in the NMOS transistors is given by,

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \qquad (7)$$

where,

$$K = \mu_n C_{ox} \frac{W}{L} \qquad (8)$$

and V_T is the threshold voltage given as,

$$V_T = V_{T_o} + \gamma\left(\sqrt{V_{SB} + 2\varphi_f} - \sqrt{2\varphi_f}\right) \qquad (9)$$

The current (I_B) in each of the transistors M1, M2 and M3 is equal, because of the current mirrors formed by M4-M6. As a result, the gate to source voltages of M1, M2 and M3 are also equal. Hence, this forces the two input terminals to be virtually grounded. The common source amplifier M15 is used to achieve the high gain, while the transistor pairs (M5 and M6) and (M7 and M8) provide the current differencing operation.
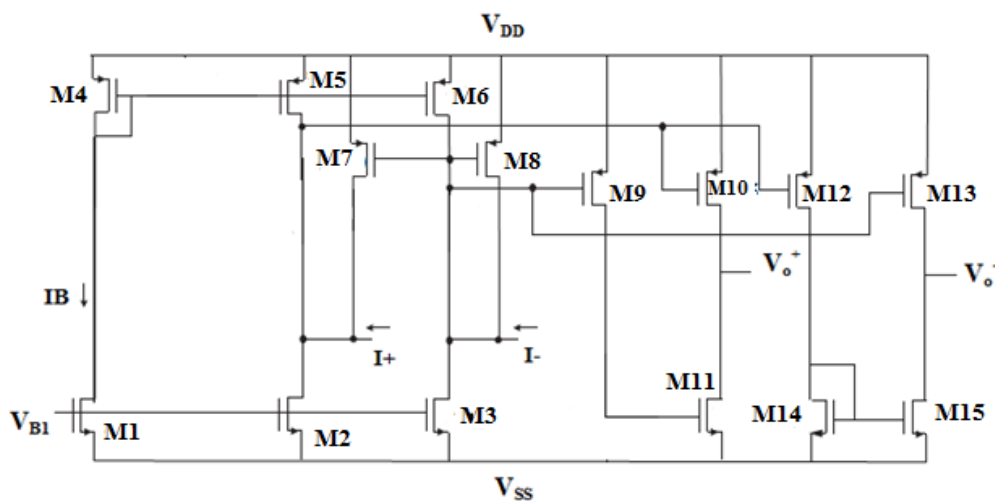

Fig. 5 The proposed differential OTRA

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:11, No:6, 2017

The proposed OTRA has smaller number of current mirrors than the OTRA proposed by Kafrawy and Soliman [1]. As the current mirrors are reduced in the proposed OTRA, this increases the frequency capabilities and also reduces the transistor mirror mismatch effect. Also, the proposed OTRA uses smaller number of transistors when compared with the Kafrawy and Soliman OTRA [1], which reduces the power dissipation.

Consider a single pole model for the transresistance R_m, it can be written as,

$$R_m(s) = \frac{R_o}{1 + \frac{s}{2\pi f_o}} \tag{10}$$

where f_o and R_o are the transresistance cutoff frequency and the DC open loop gain respectively. For high frequency applications, the transresistance gain $R_m(s)$ is expressed as,

$$R_m(s) \approx \frac{1}{sC_p} \tag{11}$$

where,

$$C_p = \frac{1}{R_o(2\pi f_o)} \tag{12}$$

IV. ANALYSIS AND VALIDATION RESULTS

The circuit in Fig. 5 is designed and implemented in UMC 1P-9M standard 90-nm CMOS technology. The simulations are carried out in Cadence IC615. Bias settings and transistor dimensions are shown in Table I. The biasing current is $I_B = 29.1$ μA and the biasing voltage is $V_{B1} = -0.9018$ V. The layout of the circuit is shown in Fig. 6. The circuit occupies an effective area of 79×53 μm^2.

Fig. 7 shows the output voltage of the circuit. This shows an input current dynamic range from -50 t0 50 μA with the offset current of 0.09 μA.

Fig. 8 shows the frequency characteristics of the open loop transresistance gain of the circuit. The DC open loop transresistance gain here is equal to 182.75 dB Ω with the gain bandwidth product of 617.6 THz Ω.
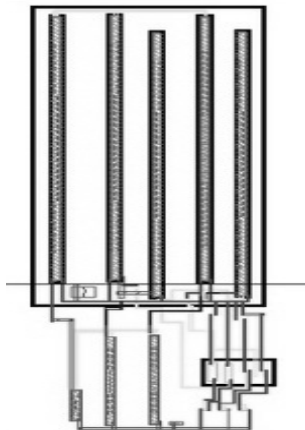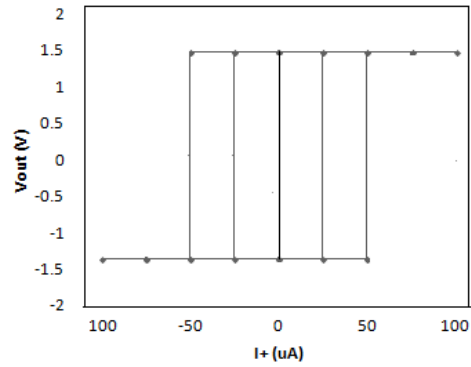

Fig. 7 Output voltage (Vo$^+$) of the proposed differential OTRA

Fig. 9 shows the transient response of the circuit. The rise time/fall time of the circuit is 0.024/0.97 ns. The settling time of the circuit is also measured giving a good settling time of 4.88 μs. The total power dissipation of the circuit is measured to be equal to 0.21 mW.

Table II summarizes the comparative advantage of the differential OTRA circuit with the OTRA circuits proposed in [1], [2] and [7]. It is clear that the proposed OTRA has more DC open loop transresistance gain and more gain bandwidth product than OTRA proposed in [1] and [7].

The open loop transresistance gain is increased from 163.2 dBΩ to 182.75 dBΩ and the gain bandwidth product is increased from 57.6 THzΩ to 617.6 THzΩ when compared with [1]. Also, the proposed OTRA has lower power dissipation. The total number of transistors in the proposed circuit are also lesser in number than the OTRA proposed in [1] and [7]. In short, the proposed design has clear advantages over the OTRA circuits proposed in [1], [2] and [7].

TABLE I
TRANSISTOR ASPECT RATIO OF PROPOSED CIRCUIT

Transistors	W (μm)	L (μm)
M1 – M3	30	1.25
M4 – M6	90	1.25
M7, M8	90	1.25
M9, M10	5.25	0.25
M11	0.25	1.25
M12, M13	0.25	0.25
M14, M15	0.25	1.25

Fig. 6 Layout of the proposed differential OTRA
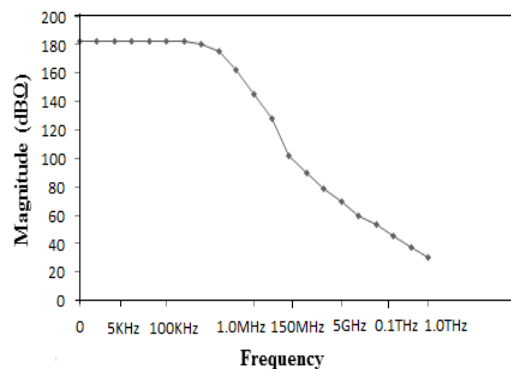
Fig. 8 Frequency characteristics of the open loop transresistance gain for the proposed circuit

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:11, No:6, 2017

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED DIFFERENTIAL OTRA AND OTRA PRESENTED IN [1], [2] AND [7]

| Parameter	OTRA proposed in [1]	OTRA proposed in [2]	OTRA proposed in [7]	Proposed differential OTRA
Power Supply (V_{DD}, V_{SS})	1.5V, -1.5V	1.5V, -1.5V	2.5V, -2.5V	1.5V, -1.5V
No. of Transistors	20	14	17	15
Total Power dissipation	0.82 mW	0.709 mW	3.96 mW	0.21mW
PSRR+	186.8 dBΩ	90.2 dBΩ	NA	198.7dBΩ
PSRR-	150.1 dBΩ	97.3 dBΩ	NA	163.4dBΩ
Input current dynamic range	-50 to 50μA	-50 to 50 μA	-20 to 20μA	-50 to 50μA
Offset current	0.1 μA	0.3 μA	0.15μA	0.09μA
DC open loop transresistance gain	163.2 dBΩ	130 dBΩ	4.054dBΩ	182.75dBΩ
Gain bandwidth product	57.6 THzΩ	3.16 THzΩ	39.8 GHzΩ	617.6THzΩ
Transresistance gain B.W. (-3dB)	0.4 MHz	1 MHz	NA	0.45MHz
Rise Time/Fall Time	0.025/1.1 ns	0.023/1.74 ns	NA	0.024/0.97ns
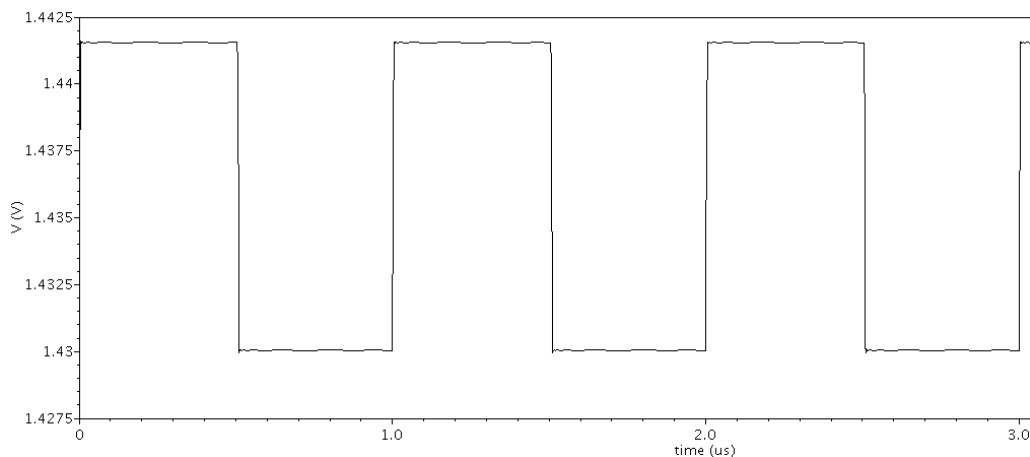
Fig. 9 Transient Response of the proposed circuit

V. CONCLUSION

A modified CMOS differential OTRA is presented. The differential OTRA is designed and implanted in a standard umc90-nm CMOS technology. Simulation results show that the OTRA has high DC open loop transresistance gain and high gain bandwidth product. It also possesses lower offset current and lower power dissipation. A comparison between the proposed differential OTRA and the OTRAs given in [1], [2] and [7] proved the strength of the given circuit.

REFERENCES

[1] K. Kafrawy and A. Soliman, "A modified CMOS differential operational transresistance amplifier (OTRA)," *International Journal of Electronics and Communication*, vol. 63, pp. 1067–1071, 2009.
[2] H. Mostafa and A. Soliman, "A modified CMOS realization of the operational transresistance amplifier," *Frequenz*, vol. 60, pp. 70–76, 2006.
[3] J. Cheng, H. Tsao and C. Chen, "Operational transresistance amplifier using CMOS technology," *Electron Lett*, vol. 28, pp. 2087–2088, 1992.
[4] K. N. Salama and A. M. Soliman, "CMOS operational transresistance amplifier for analog signal processing," *Microelectronics Journal*, vol. 30, pp. 235-245, 1999.
[5] H. O. Elwan, A. Soliman and M. A. Ismail, "A CMOS norton amplifier based digitally controlled VGA for low power wireless applications," *IEEE Trans Circuits Syst II*, vol. 48, pp. 245–254, 2001.
[6] H. O. Elwan and A. M. Soliman, "CMOS differential current conveyors and applications for analog VLSI," *Analog Integrated Circuits and Signal Processing*, vol. 11, pp. 35-45, 1996.
[7] S. Mittal, G. Kapur, C. M. Markan and V. P. Pyara, "Analog Field Programmable CMOS Operational Transrsistance Amplifier (OTRA)," *Engineering and Systems (SCES) Students Conference*, Allahabad, 12-14 April, 2013.
[8] P. E. Allen and Holberg, "CMOS analog circuit design," HRW, Inc., Orlando, Florida 1987.