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MILESTONE REPORT

APPLY TF TEST BENCH TO FEE PROTOTYPES

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Abstract:

This document is related to the implementation of Task 4.5 'Design & development of new electronics characterisation system for EMC control'. This task plans to design and develop a new automatic EMC test bench to measure the noise transfer functions (TF) of physics detectors, and a common and portable test bench to perform in-situ EMC conducted emission measurements of very small Direct Current (DC-DC) converters and power supply units in irradiation facilities.

AIDAinnova Consortium, 2023

For more information on AIDAinnova, its partners and contributors please see <http://aidainnova.web.cern.ch/>

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TABLE OF CONTENTS

1. INTRODUCTION	4
2. AUTOMATIC TRANSFER FUNCTION MEASUREMENT SYSTEM DESIGN.....	5
3. SYSTEM VALIDATION TESTS.....	7
4. ADVANCED TEST WITH RD53A CHIPS	10
4.1. RD53A TESTS AT CHIP LEVEL.....	10
4.2. 1x2 Rd53A HDI WITH 3D SENSORS SYSTEM LEVEL TESTS.....	11
5. CONCLUSIONS AND FUTURE DEVELOPMENTS.....	14
6. REFERENCES	16

Executive summary

Task 4.5 targets the upgrade of the accelerator facility for detector characterization, including studying of detector charge collection properties and radiation hardness studies of detector materials at micro-scales. The important milestone, apply TF test bench to FEE prototypes has been achieved as planned and described. This milestone includes the design and development of the full automated system, both software and hardware and validation tests using RD53A read-out chip prototypes. In addition to this, further tests using realistic prototypes (serial chain of 1x2 HDI-RD53A modules with 3D sensors) have been successfully performed.

1. INTRODUCTION

The EM transfer functions of physics detectors and Electromagnetic Compatibility (EMC) tests are powerful tools for electronics designers to evaluate grounding and shielding issues of detectors. These curves can be calculated based on susceptibility tests on FEE units. Most of the requested accesses to EMC TA facility have performed susceptibility tests to calculate the TF curves of the detectors. The idea of the susceptibility test is to inject a noise current at different frequencies and amplitudes through the power lines of the FEE and measure the output of FEE based on the DAQ of each detector. Based on these test results, the TF of the FEE can be calculated as a ratio between the injected current and the noise contribution at the output of the FEE due to the perturbing current. This test and TF calculations were not automatic, and they required a lot of time. The long duration of the test limits the number of the tested lines and it increased the cost of the access to the EMC facility.

Previous studies show that these susceptibility tests have turned out to be really useful to characterize particle detectors and improve its performance based on the results [1] [2] [3].

Therefore, the development of an automatic susceptibility test bench to measure the TF curve of any line associate to the FEE would allow users performing measurements of TF at lower cost and less time (testing time can be reduced from weeks to a few days). It will also allow further and more complex studies to analyze in detail any element that can be critical for the noise sensitivity and robustness of the final detector. ITAINNOVA provides the design and control of EMC test equipment and IPHC-CNRS will be in charge of the design of the interface between EMC system and DAQ of the detector.

2. AUTOMATIC TRANSFER FUNCTION MEASUREMENT SYSTEM DESIGN

The system has been designed in different blocks or programmed in Python. The main blocks of the automatic transfer function measurement system shown in Figure 1 are:

- A1. Control and configuration of test equipment
- A2. Interface with DAQ to obtain equivalent noise charge (ENC) value results
- A3. Results printing tables and plots

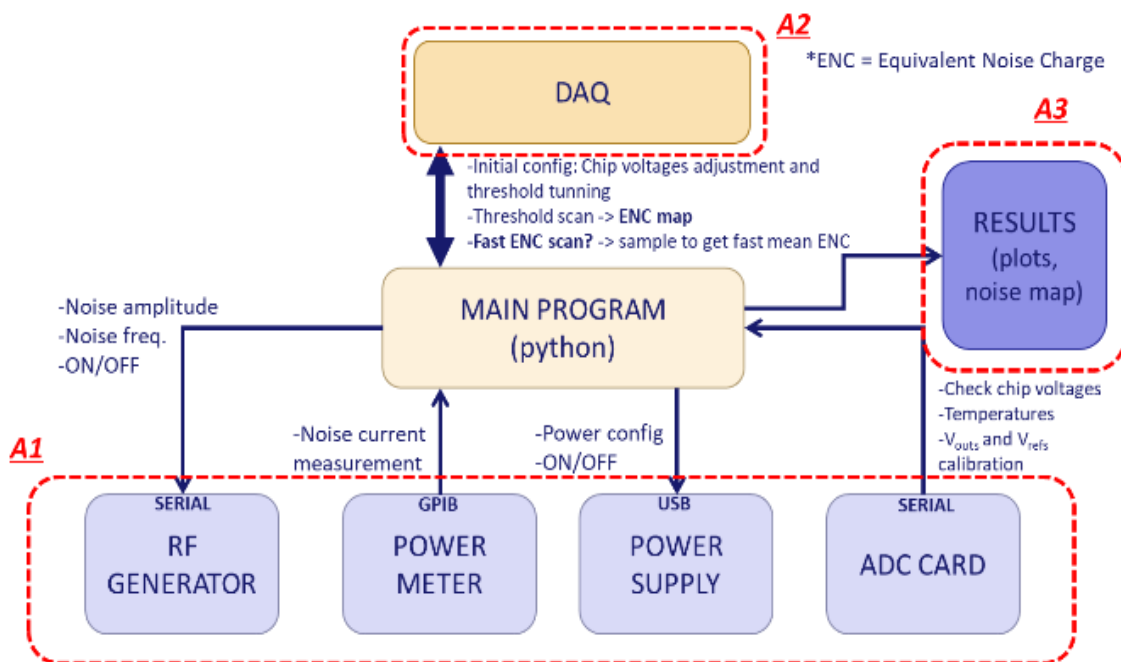


Figure 1: Block diagram of new TF measurement system

The routines to control the test instruments have been developed and tested during the first stage of the project. They have been designed to run correctly on Windows and Linux operating systems, for easy adaptation to any DAQ detector. The automatic platform has been designed to read and modify the DAQ configuration files to adjust different test parameters, configure the readout chip, launch noise scans and read the results of the DAQ output. The different elements of the platform have been programmed and implemented.

The layout of the instruments which are used in the automatic TF measurement system can be found in Figure 2.

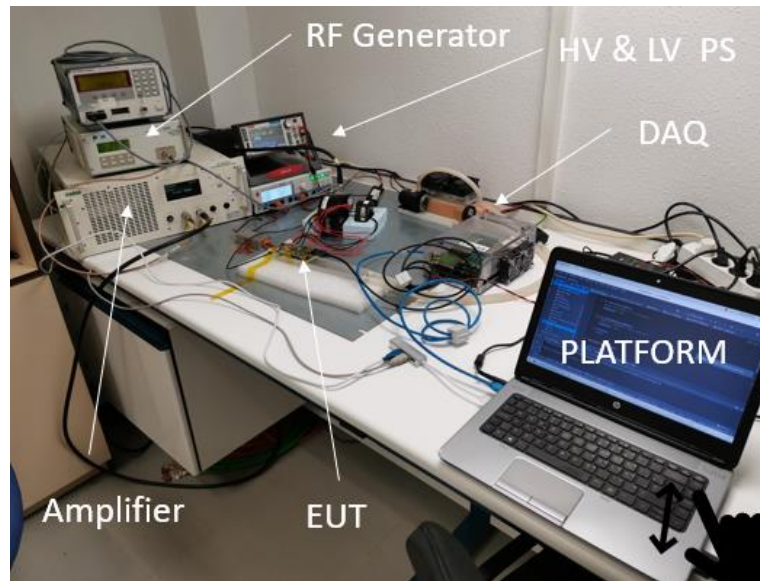


Figure 2: Automatic TF measurement system set-up

After the test is completed, the software generates two basic files. The first one is a text file table containing all the test data (See Figure 3). This table is composed of the injected current (mA), injected power (dBm), ENC values (e-) and TF (e-/mA) for each frequency (MHz).

Freq. (MHz)	Current (mA)	Level (dBm)	ENC (e-)	TF (e-/mA)
REF	REF	REF	71.8	0
0.1	150.9	-13.2	90.6	0.367
0.2	197.4	-13.6	86.9	0.248
0.3	249.6	-13.2	81.8	0.157
0.4	404.0	-10.1	83.8	0.107
0.5	399.3	-10.7	78.5	0.08
0.6	426.6	-10.7	76.2	0.06
0.7	426.8	-11.0	72.5	0.023
0.8	449.2	-10.7	74.2	0.042
0.9	448.6	-10.9	74.9	0.048
1	395.6	-12.1	73.7	0.042
1.5	303.6	-14.3	74.7	0.069
2	398.6	-13.5	78.5	0.079
3	398.5	-16.0	79.9	0.088
4	352.0	-17.7	81.9	0.112
5	299.8	-17.8	82.2	0.134
7	253.9	-16.8	85.3	0.181
10	301.4	-14.1	110.5	0.279
12	303.5	-13.6	131.3	0.362
15	302.3	-13.8	178.9	0.542
17	300.2	-12.2	218.1	0.686
20	241.6	-10.0	207.8	0.807
22	224.2	-10.0	178.3	0.728
25	149.6	-15.5	107.7	0.537
27	124.3	-17.5	88.9	0.422
30	126.3	-16.3	78.6	0.253
40	101.0	-12.7	75.6	0.234
50	90.7	-10.0	72.9	0.138

Figure 3: Text file with the raw data

The second file is a plot (See Figure 4) representing the TF (e-/mA) as a function of frequency (MHz), the aim of this plot is to help the user to interpret the results while running the tests.

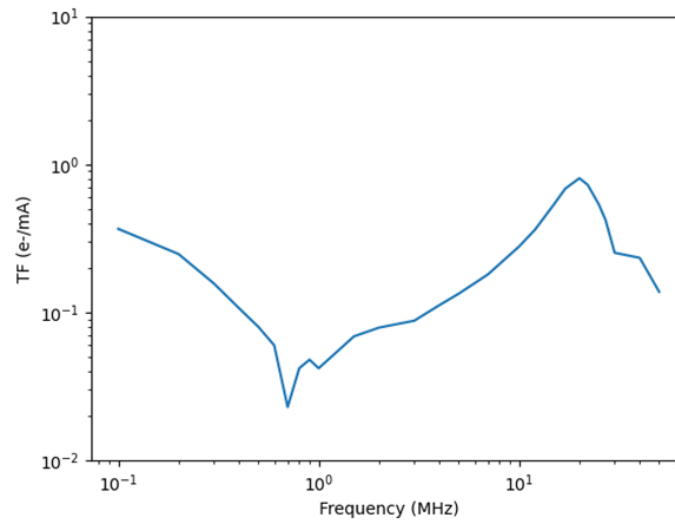


Figure 4: Plot generated by the software

The raw data generated by the DAQ software is also stored for post-processing purposes in case more detailed analyses are needed.

3. SYSTEM VALIDATION TESTS

Having a first operational version of the automated characterization system in place, the focus during the second stage of the project has been on improving and debugging the software to ensure greater robustness, reliability, safety, repeatability, and to start using this platform to automatically run more complex tests.

In terms of the system safety, some protections have been added in order to safeguard the electronics of the chips. These protections correspond to a limitation on the power and current that can be supplied to the chips. Additionally, a timeout has been implemented to prevent a continuous injection of noise into the chips in case the software gets frozen (typically because of DAQ communication lost) at any point during the test.

Regarding the chip prototypes used for these tests, RD53A and RD53B are read-out chip demonstrators that have been developed within the RD53 collaboration [4]. RD53A is an ATLAS-CMS common chip that includes 3 different analogue front-ends to evaluate their performance and reliability, in order to choose one of them for the final read-out chip design. However, RD53B is a prototype which is very close to the final version that includes the chosen analogue front-end. There are 2 versions adapted to each detector requirements and front-ends, one for ATLAS, called ITkPix-V1 and one for CMS, called CROC-V1.

For these tests, in order to have comparable results, only the Linear FE has been used with RD53A chips, as it is the one included in CROC-V1.



Figure 5: RD53A single chip card

To be able of measuring the repeatability of these tests, 10 tests are performed using a RD53A single chip card (See Figure 5) as reference system. 10 full characterization curves (transfer functions) are used to measure the uncertainty of the whole system.

The uncertainty range is represented by a vertical bar at each measurement point as it is shown in figure 6. The uncertainty in the left plot is defined as the difference between maximum and minimum values of the series of measurements. In the right plot it is defined as \pm standard deviation ($\pm\sigma$).

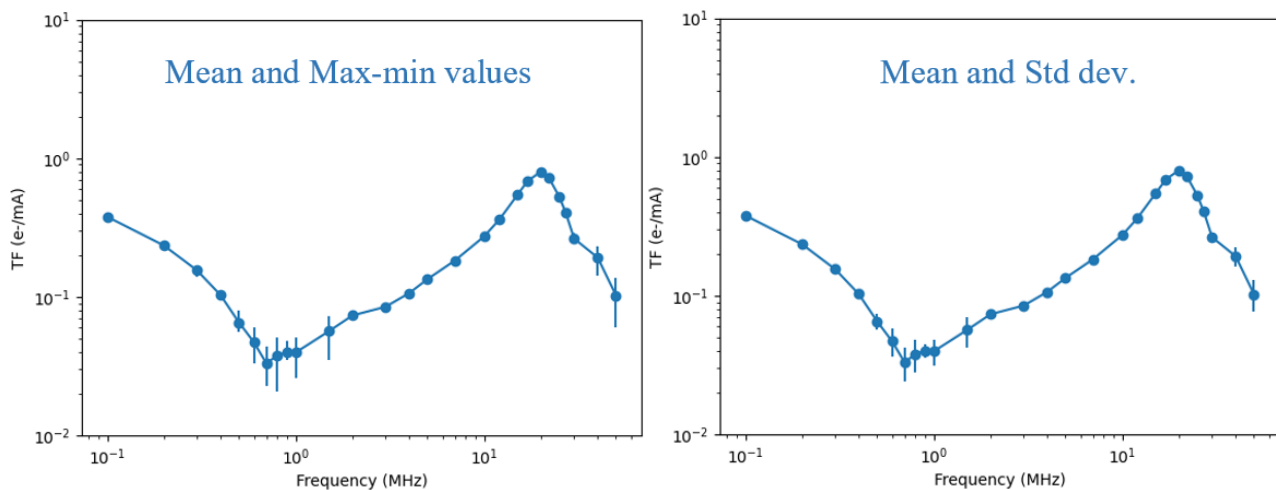


Figure 6: TF uncertainty measurement test result

In most cases the repeatability is very good, with almost negligible uncertainty. The highest uncertainty can be seen in the points with lower TF values ($< \sim 0.1 \text{ e-/mA}$). This was expected since in the cases of sensitivities under 0.1 e-/mA , the measured noise mean value is very close to the thermal noise floor making it difficult to measure with precision.

Performing each of these tests could take many hours and full dedication of one person using the old manual system, so reducing the test time was a key requirement. Therefore, different test speeds have been programmed, considering that no significant changes were observed in the results depending on the testing speed (See Figure 7).

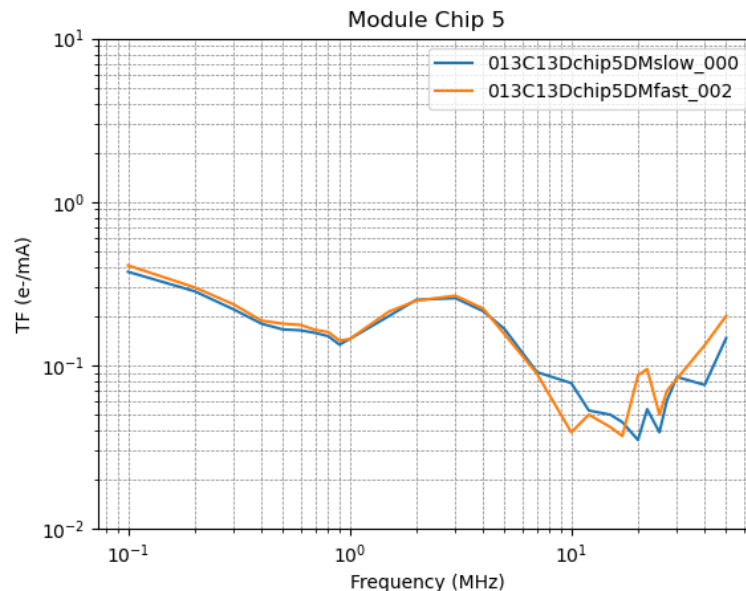


Figure 7: Comparison between fast and slow mode

The test speed is mainly determined by the number of pixels used. In case maximum detail and precision is needed, the full array of pixels is used. This kind of test is slow but very useful for further analysis studies at chip level, as the data of every single pixel is stored for each frequency.

For system level (serial powering) studies where local effects at chip level are not relevant, a certain sample of pixels can be selected to run the tests much faster. This sample has to be chosen carefully, evenly covering as much chip surface as possible to avoid local chip region bias effects.

With the new system, time has been substantially reduced, and everything is run automatically, which also improves repeatability and reduces possible human errors. In addition, the user receives a notification via email when the test finishes. Thus, the user doesn't have to keep an eye on the test progress either, allowing the user to perform other tasks during the test. The email sent to the user also includes the test results (raw data and interpreted plots), which provides online backups of the tests.

Once the software was confirmed to be functional and reliable, the next stages were focused on improving functionalities and making the system as much compatible as possible with any hardware set-up or DAQ software.

Regarding the testing hardware, an option to add the injection and measurement clamp calibration curves has been added, which will allow to use any current clamp just by adding its transfer function. Apart from that improvements, new DAQ software compatibility has been added. First, BDAQ53 from ATLAS, which is compatible with both RD53A and RD53B. And second, the new versions of CMS Ph2 ACF (Acquisition and Control Framework) which is an early version of the final DAQ

hardware and software, and is compatible with RD53A, CROC-V1 and any future version of CROC. This assures that the system will be compatible with the final detector chip with almost no adjustments needed. Figure 8 (right) shows test results of a RD53B single chip card.

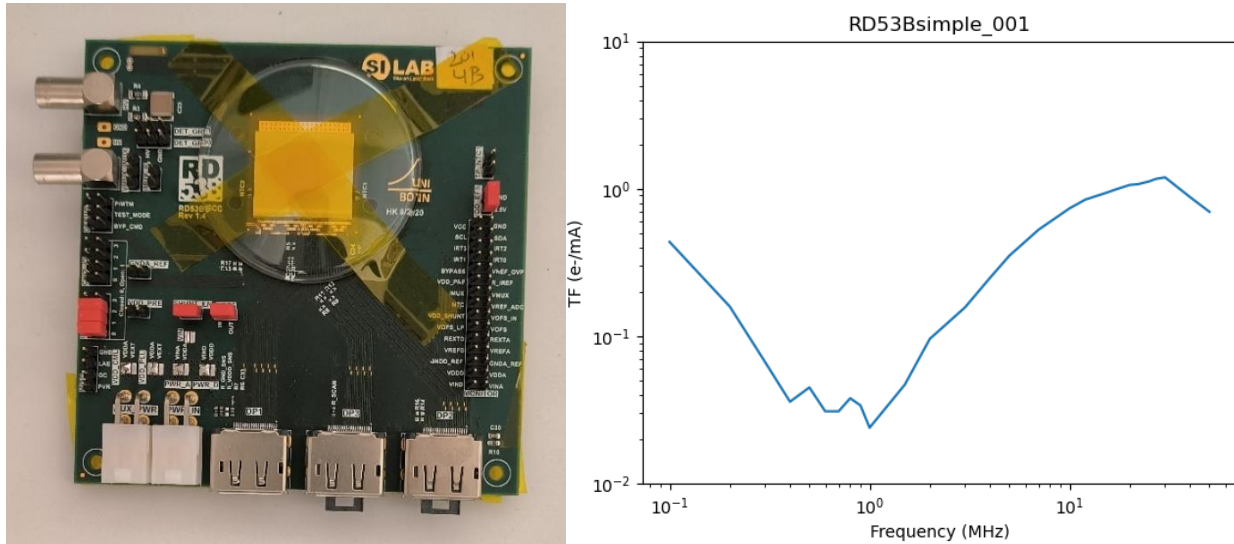


Figure 8: RD53B (CROC v1) single chip card (left) and its measured TF (right)

4. ADVANCED TEST WITH RD53A CHIPS

4.1. RD53A TESTS AT CHIP LEVEL

RD53A and RD53B integrate a complex linear current and voltage regulator integrated on-chip, that allows connecting chips or modules in series (serial powering). This regulator is called Shunt-LDO (SLDO) [5], which is a hybrid of a Shunt and an LDO regulator. As this regulator has a quite high bandwidth ($>1\text{MHz}$), it works as an active filter from the point of view of input noise. In previous tests campaigns (before having the automatic system), several results have proven that the chip sensitivity to noise was very dependent on the working point (input/output current and voltage) of the SLDO [6]. In the next plot, the effects of different working points of the SLDO regulator are shown. In this case the SLDO is configured as LDO only, which is a mode useful when serial powering is not needed.

Left plot shows the TF for different input voltage configurations, varying it from 1.6V to 2.0V in steps of 0.1V. In this case results are almost identical in all the cases. These results are interesting to understand that, considering the SLDO an active filter, it behaves completely different depending on its working mode, SLDO or LDO mode. SLDO is very dependent on its configuration, but LDO gets similar results in any conditions.

Right plot shows the TF for different chip threshold configuration, varying it from 800 to 2000 electrons. It was expected that a lower threshold meant a higher noise sensitivity, as it is closer to the noise floor of the chip analogue front end, but the results show quite similar behaviour with just some small variation depending on the frequency. Lower threshold has higher TF values in low frequency

but lower TF in higher frequency. It is important to note that during this set of tests the RD53A chip was configured with the linear FE.

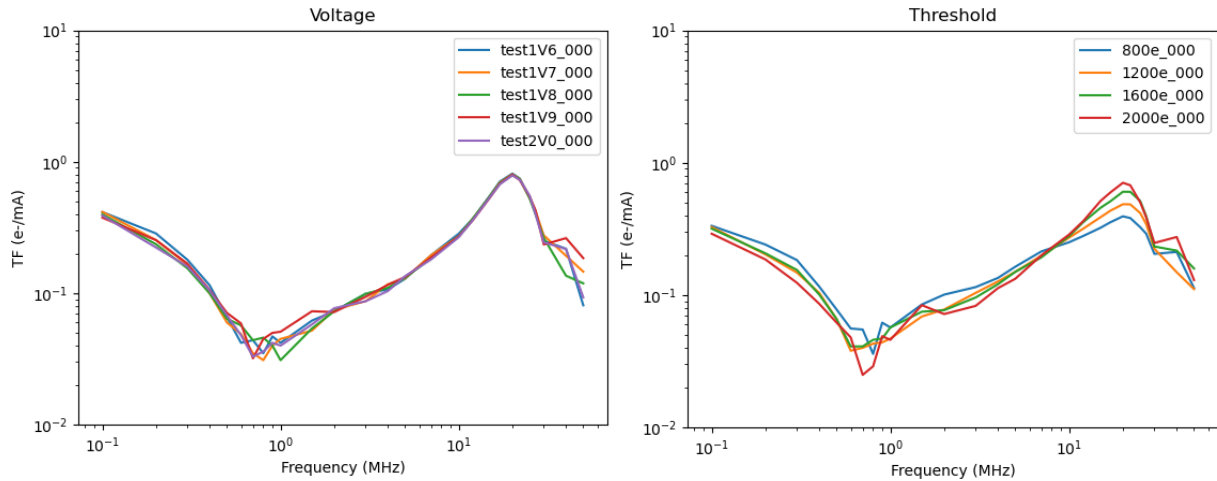


Figure 9: Effect of system configuration on noise sensitivity in LDO mode: Input voltage in volts (left). Front-end threshold charge in electrons (right)

4.2. 1X2 RD53A HDI WITH 3D SENSORS SYSTEM LEVEL TESTS

After completing some automated tests and studies in a simple single chip card, the next step was moving to more realistic prototypes, which are closer to the final detector set-up. This is the case of HDI assemblies. A schematic view of a 1x2 HDI module is shown in figure 10, where HDI, sensor and chips can be distinguished.



Figure 10: HDI 1x2 RD53A module with sensors schematic

Preliminary tests using 1x2 HDI modules (see figure 11) with 3D sensors have been carried out. These HDI are prototypes of the flex PCB with 2 chips and 3D sensors that are going to be mounted in the inner-most layers of the barrel of the inner tracker pixel detector of CMS (TBPX).



Figure 11: HDI 1x2 RD53A + 3D sensors

In a first stage, the study is focused in measuring the noise sensitivity variation between the chips in a single module. Big differences on noise sensitivity could mean that the layout of the PCB has strong contribution to it. In our preliminary results (figure 11), some differences can be seen but they are quite low overall. This difference can be explained by the layout of the PCB and the location of the filtering capacitors, that can make different filtering effect on the chips depending on where they are placed.

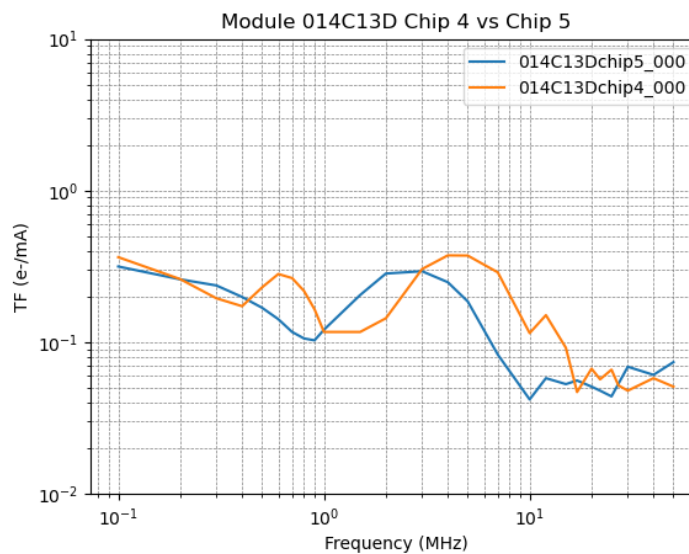


Figure 11: TF measured in chip 4 vs in chip 5 of a 1x2 module (SN: 014C13D)

The same curves have been also measured in all the chips of 3 different modules (010C13D, 013C13D, 014C13D).

A comparison among all the modules have done to check the variability of the sensitivity from one module to another. This variability can be given by any of the elements of the module such as: chip fabrication tolerances, sensor effects, HDI components tolerances, small variation in the set-up, etc. The results seen in figure 12 show that the module-to-module variation is very low when they are characterized one by one.

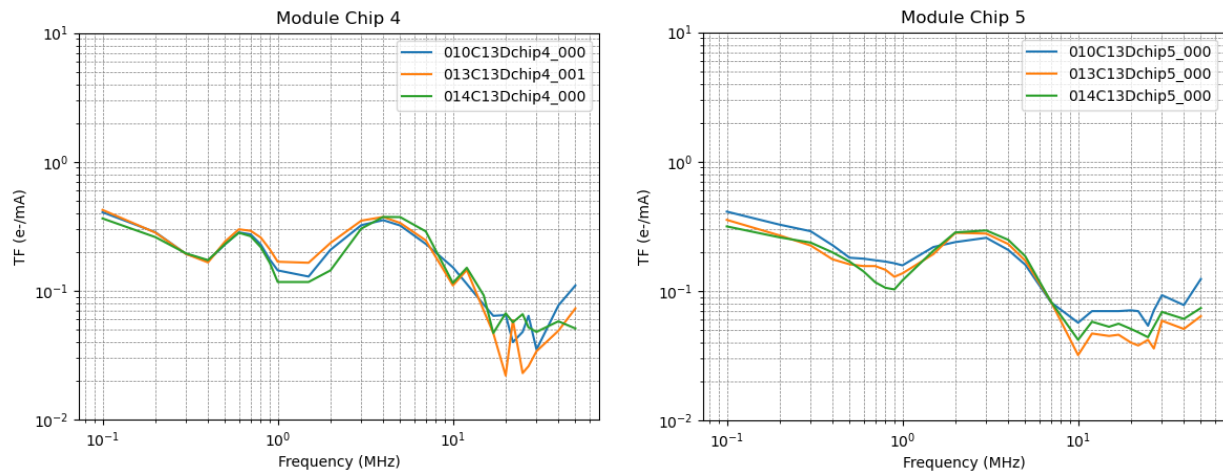


Figure 12: TF measured in chips 4 (left) and in chips 5 (right)

The latest tests that have been done using the new system, and still working on them, are the characterization of the noise sensitivity in a system formed by three modules connected in series. The order of the modules starting from the one closest to the power supply is: 014C13D, 010C13D and 013C13D (See Figure 13).

In this set-up, the HDIs cannot be seen as they are located below the e-links adapter cards. Besides, the modules are covered with Kapton tape that assures a strong fixation of the modules to the cooling plate. To get reliable results, it is important to assure a constant temperature in all the modules during these tests, as the noise floor of each chip is strongly dependent on temperature.

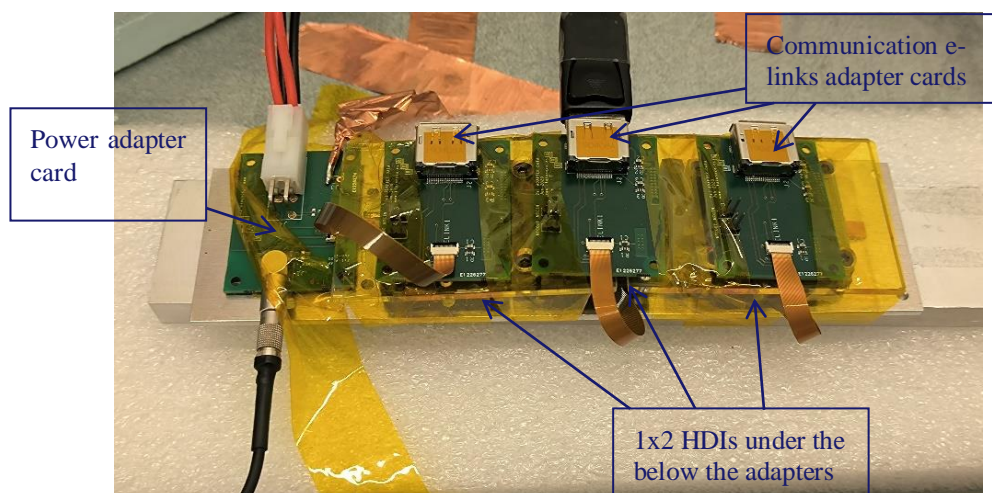


Figure 13: System formed by three modules in series

In Figure 14, it can be observed how the position of the module in the chain with respect to the power supply affects the noise sensitivity. The closer the module is to the power supply, the more sensitive it is to the injected noise. This effect was expected, and it happens due to the noise filtering capability of each module. Each module filtering is able of bypassing part of the injected noise back to the

source. This produces a filtering accumulation effect being the modules connected in series. This means that the modules further from the power supply will have higher noise filtering capacity, and hence, they will have a lower noise sensitivity.

Regarding figure 14, it should be mentioned that there were issues measuring the TF in the higher frequencies.

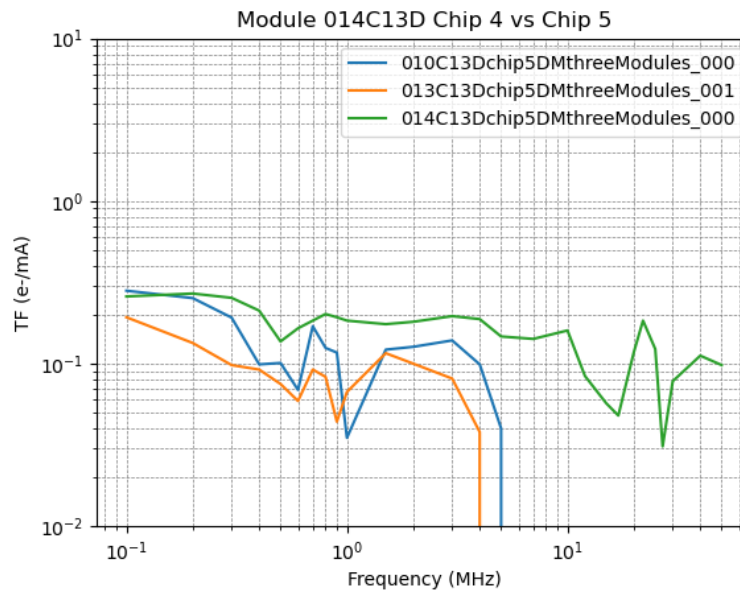


Figure 14: TF measurement of chip 5 in the system formed by three modules in series.

5. CONCLUSIONS AND FUTURE DEVELOPMENTS

Planned activities within the AIDAInnova Task 4.5 have been realized as scheduled, and the milestone MS17 has been achieved. The automatic system has been fully developed and validated with tests in the lab using RD53A chip prototypes. In addition, further improvements and tests in more realistic prototypes (RD53A 1x2 HDI serial chain) have been successfully performed.

In the future, a graphical user interface will be incorporated into the software to make the interaction between the user and the program more intuitive. It will allow any person with basic knowledge of read-out chips configuring and launching complex tests as well as the subsequent interpretation of the results. In addition, it is planned to create a database where the results will be automatically stored. This will achieve a better organization and access to the generated result files and will simplify further post-processing and data analysis.

Temperature and its effect on noise sensitivity is important in a detector and a clear topic of interest. Therefore, a temperature control system, both hardware and software, is planned to be developed and integrated in the automatic control system. This implementation will add new possibilities to the automatic system: running the tests with precise temperature control, tests at different temperatures to analyse noise effects and possible issues, and also the possibility of implementing thermal protections to assure the prototypes safety.

Finally, further improvements in the software are also going to be implemented in the future. For instance, parametric tests which depend on the parameters of the chip configuration files will be automated. An example of this parametric tests is shown in Figure 9, although in that case it was performed semi-automatically.

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