

1. Description

1.1. Project

Project Name	met4FOF_SSU_V2
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 5.0.1
Date	03/22/2019

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SYS_TRACECLK	
2	PE3	I/O	SYS_TRACED0	
3	PE4	I/O	SYS_TRACED1	
4	PE5	I/O	SYS_TRACED2	
5	PE6	I/O	SYS_TRACED3	
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0 *	I/O	GPIO_Output	LCD_RESET
11	PF1 *	I/O	GPIO_Output	LCD_DC/RS
14	PF4	I/O	ADC3_IN14	
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Output	LCD_CS
19	PF7 *	I/O	GPIO_Output	SD_CS
21	PF9	I/O	DAC_EXTI9	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC2_IN10	
27	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ- TR_MDC]
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM2_CH1	
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ- TR_REFCLK0]
36	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ- TR_MDIO]
37	PA3	I/O	TIM2_CH4	
38	VSS	Power		
39	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PA4	I/O	DAC_OUT1	
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	ETH_CRSDV	RMII_CRSDV [LAN8742A-CZ-TR_CRSDV]
44	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
47	PB1	I/O	ADC1_IN9	
49	PF11	I/O	ADC3_EXTI11, ADC2_EXTI11	
51	VSS	Power		
52	VDD	Power		
55	PF15 *	I/O	GPIO_Output	LED_BT2
56	PG0 *	I/O	GPIO_Output	CAN1_MODE
58	PE7	I/O	UART7_RX	
59	PE8	I/O	UART7_TX	
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	TIM1_CH2	
66	PE13	I/O	TIM1_CH3	
67	PE14	I/O	TIM1_CH4	
69	PB10	I/O	TIM2_CH3	
71	VCAP_1	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
76	PB15	I/O	RTC_REFIN	
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
79	PD10 *	I/O	GPIO_Output	GPIO1_2
80	PD11 *	I/O	GPIO_Output	GPIO1_1
81	PD12 *	I/O	GPIO_Output	GPIO2_2
82	PD13 *	I/O	GPIO_Output	GPIO3_2
83	VSS	Power		
84	VDD	Power		

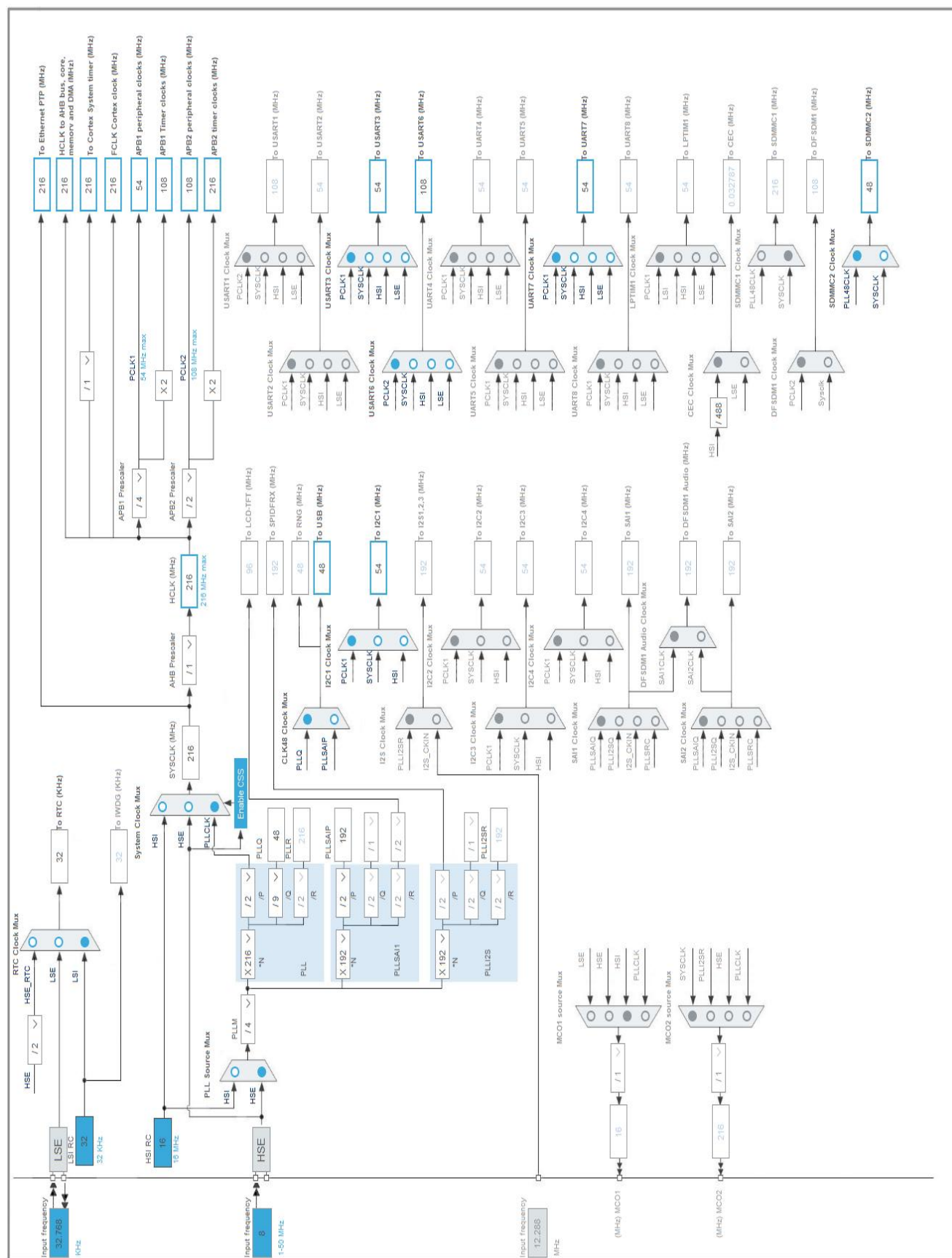
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
85	PD14 *	I/O	GPIO_Output	GPIO2_1
86	PD15 *	I/O	GPIO_Output	GPIO3_1
89	PG4 *	I/O	GPIO_Input	BT_1
90	PG5 *	I/O	GPIO_Input	BT_2
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
93	PG8	I/O	USART6_DE	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
98	PC8 *	I/O	GPIO_Output	USART6_RE
99	PC9 *	I/O	GPIO_Output	SENSOR_CS2
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	USB_ID
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
110	PA15	I/O	SYS_JTDI	
111	PC10	I/O	SPI3_SCK	
112	PC11	I/O	SPI3_MISO	
113	PC12	I/O	SPI3_MOSI	
114	PD0	I/O	CAN1_RX	
115	PD1	I/O	CAN1_TX	
116	PD2 *	I/O	GPIO_Output	F_CS
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6	I/O	SDMMC2_CK	
123	PD7	I/O	SDMMC2_CMD	
124	PG9	I/O	SDMMC2_D0	
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A- CZ-TR_TXEN]

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ- TR_TXD0]
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SYS_JTDO-SWO	SWO
135	PB5	I/O	SPI1_MOSI	
136	PB6	I/O	I2C1_SCL	
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	SENSOR_CS1
140	PB9	I/O	I2C1_SDA	
141	PE0 *	I/O	GPIO_Output	LED_BT1
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	met4FOF_SSU_V2
Project Folder	C:\Users\seeger01\Met4FoF-SmartUpUnit\doc
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.14.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN9

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 6 *
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 9
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. ADC2

mode: IN10

mode: External-Trigger-for-Regular-conversion

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 6 *
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Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	EXTI Line11
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 10
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0
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WatchDog:

Enable Analog WatchDog Mode	false
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7.3. ADC3

mode: IN14

mode: External-Trigger-for-Regular-conversion

7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode
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ADC_Settings:

Clock Prescaler	PCLK2 divided by 6 *
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	EXTI Line11
External Trigger Conversion Edge	Trigger detection on the rising edge

Rank	1
Channel	Channel 14
Sampling Time	3 Cycles
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

7.4. CAN1

mode: Mode

7.4.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	64 *
Time Quantum	1185.1851851851852 *
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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7.5. DAC

mode: OUT1 Configuration

mode: External Trigger

7.5.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

7.6. ETH

Mode: RMII

7.6.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation Enabled

General : Ethernet Configuration:

Ethernet MAC Address 00:80:E1:00:00:00

PHY Address 0 *

Ethernet Basic Configuration:

Rx Mode Interrupt Mode

TX IP Header Checksum Computation By hardware

7.6.2. Advanced Parameters:

External PHY Configuration:

PHY LAN8742A_PHY_ADDRESS

PHY Address Value 0

PHY Reset delay these values are based on a 1 ms SysTick interrupt 0x000000FF *

PHY Configuration delay 0x00000FFF *

PHY Read TimeOut 0x0000FFFF *

PHY Write TimeOut 0x0000FFFF *

Common : External PHY Configuration:

Transceiver Basic Control Register 0x00 *

Transceiver Basic Status Register 0x01 *

PHY Reset 0x8000 *

Select loop-back mode 0x4000 *

Set the full-duplex mode at 100 Mb/s 0x2100 *

Set the half-duplex mode at 100 Mb/s 0x2000 *

Set the full-duplex mode at 10 Mb/s 0x0100 *

Set the half-duplex mode at 10 Mb/s 0x0000 *

Enable auto-negotiation function 0x1000 *

Restart auto-negotiation function 0x0200 *

Select the power down mode 0x0800 *

Isolate PHY from MII	0x0400 *
Auto-Negotiation process completed	0x0020 *
Valid link established	0x0004 *
Jabber condition detected	0x0002 *

Extended : External PHY Configuration:

PHY special control/status register Offset	0x10 *
PHY Speed mask	0x0002 *
PHY Duplex mask	0x0004 *
PHY Interrupt Source Flag register Offset	0x000B *
PHY Link down interrupt	0x000B *

7.7. I2C1

I2C: I2C

7.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x20404768 *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.8. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.9. RTC

mode: Activate Clock Source

mode: Activate Calendar

mode: Reference clock detection

7.9.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.10. SDMMC2

Mode: SD 1 bit

7.10.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

7.11. SPI1

Mode: Full-Duplex Master

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	16 *
Baud Rate	6.75 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.12. SPI3

Mode: Full-Duplex Master

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits

First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	2
Baud Rate	27.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.13. SYS

Debug: JTAG with Trace Synchro(4 bits)

Timebase Source: TIM14

7.14. TIM1

Slave Mode: Trigger Mode

Trigger Source: ITR0

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Trigger Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.15. TIM2

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.16. UART7

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.17. USART3

Mode: Asynchronous

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.18. USART6

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High

Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. USB_OTG_FS

Mode: Device_Only

mode: Activate_SOF

mode: Activate_VBUS

7.19.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

7.20. FATFS

mode: SD Card

7.20.1. Set Defines:

Version:

FATFS version	R0.12c
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Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled

USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

7.20.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance	SDMMC2
Use dma template	Enabled

7.21. FREERTOS

mode: Enabled

7.21.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
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MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15

LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

7.21.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

7.22. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.22.1. General Settings:

LWIP Version:

LWIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **) 2.0.3

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module) Enabled

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **) Enabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation) Enabled
 LWIP_IGMP (IGMP Module) Disabled
 LWIP_DNS (DNS Module) Disabled
 LWIP_UDP (UDP Module) Enabled
 MEMP_NUM_UDP_PCB (Number of UDP Connections) 4
 LWIP_TCP (TCP Module) Enabled
 MEMP_NUM_TCP_PCB (Number of TCP Connections) 5

7.22.2. Key Options:

Infrastructure - OS Awareness Option:

NO_SYS (OS Awareness) OS Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout) Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection) Enabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size) 1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs) 16
 MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks) 4
 MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections) 8
 MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued) 16
 MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List) 1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool) 16
 PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool) 592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality) Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets) 255
 TCP_WND (TCP Receive Window Maximum Size) 2144
 TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets) Enabled
 TCP_MSS (Maximum Segment Size) 536
 TCP_SND_BUF (TCP Sender Buffer Space) 1072
 TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender) 9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Disabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled
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Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled
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Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0

7.22.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled
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7.22.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled
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7.22.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled
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7.22.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent) Disabled

7.22.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **) Disabled

7.22.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **) Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **) Disabled

7.22.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks) Disabled

LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks) Disabled

Performance Options:

LWIP_PERF (Performance Testing for LwIP) Disabled

7.22.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statistics Collection) Disabled

7.22.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **) Enabled *

LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif) Disabled

CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets) Disabled

CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets) Disabled

CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets) Disabled

CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets) Disabled

CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.22.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All
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* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC0	ADC2_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PF11	ADC2_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
ADC3	PF4	ADC3_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PF11	ADC3_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
DAC	PF9	DAC_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
RTC	PB15	RTC_REFIN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SDMMC2	PD6	SDMMC2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	SDMMC2_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG9	SDMMC2_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PE2	SYS_TRACECLK	n/a	n/a	n/a	
	PE3	SYS_TRACED0	n/a	n/a	n/a	
	PE4	SYS_TRACED1	n/a	n/a	n/a	
	PE5	SYS_TRACED2	n/a	n/a	n/a	
	PE6	SYS_TRACED3	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	STLK_TX [STM32F103CBT6_PA2]
USART6	PG8	USART6_DE	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	USB_VBUS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_DP
Single Mapped Signals	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_ID
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RESET
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DC/RS
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_CS
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD_CS
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_BT2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAN1_MODE
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO1_2
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO1_1
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO2_2
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO3_2
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO2_1
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO3_1
	PG4	GPIO_Input	Input mode	Pull-up *	n/a	BT_1
	PG5	GPIO_Input	Input mode	Pull-up *	n/a	BT_2
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USART6_RE
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SENSOR_CS2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	F_CS
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SENSOR_CS1
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_BT1

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	0	0
Ethernet global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
CAN1 TX interrupts	unused		
CAN1 RX0 interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
USB On The Go FS global interrupt	unused		
USART6 global interrupt	unused		
FPU global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
UART7 global interrupt		unused	
SDMMC2 global interrupt		unused	

* User modified value

9. Software Pack Report