# A Highly Linear Dual Stage Amplifier with Beyond 1.75 THz Gain-Bandwidth-Product

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*Abstract*— **This work reports a multi-purpose highly linear ultra-wideband amplifier with a gain bandwidth product (GBP) of 1.75 THz, the highest reported in any MMIC process. A transimpedance amplifier is cascaded with a distributed amplifier, emulating a receiver subsystem. Using a diamond heat spreader, to dissipate heat from transistors, the cascaded amplification subsystem can achieve very high OIP3 from 20 to 24 dBm when measured between 5 to 65 GHz. A small signal average gain of 24 dB is observed over a frequency range exceeding the maximum measurable bandwidth from DC to 110 GHz. Compared with other ultra-wideband MMIC amplifiers beyond 110 GHz bandwidth, the circuit offers a unique combination of high linearity (OIP3) and high gain. As a result, the cascaded amplifier is suitable for applications in optical-electrical converters, spectroscopy and ultrawideband measurement systems in the sub-THz frequency range.**

*Index terms*— *Gain bandwidth product (GBP), distributed amplifier (DA), InP double heterojunction bipolar transistor (DHBT), monolithic microwave integrated circuit (MMIC).*

## I. INTRODUCTION

Data transceiver systems have developed rapidly in the past years, both for wireline, wireless and hybrid (RF over fiber) systems. Recently, wireless communication has been commercially rolled out for 5G, promising >1 Gbps to user's end. Development is running towards future standards for even higher throughputs. Wireline communication is racing towards commercial implementation with >100 Gbps single-channel optical throughput. Clearly, the communication world now requires ultra-wideband amplifiers for high bit-rate transceiver applications for both wireless and wireline technologies. As a domino effect, characterizing such broadband systems requires ultra-wideband measurement platforms, which in turn demand for ultra-wideband multi-purpose amplifiers as well. Typical figure of merits for such amplifiers are: high gain-bandwidth-product (GBP), decent efficiency, low deviation from linear phase, high linearity and low dc power consumption.

Distributed amplifier (DA) topology has historically shown to cater the more than an octave bandwidth the aforementioned applications require. With the first report of a DA being based on GaAs MESFET MMICs [1], several technologies have been used since then to improve in GBP, power, and low deviation from linear phase. With state-of-the-art CMOS [2] and SiGe BiCMOS [3] technologies, high bandwidths up to 180 GHz have been achieved. With InP HEMT [4] an InP DHBT [5-9] technology, bandwidths up to 241 GHz have been reported. Overall, however, distributed amplifiers based on InP DHBTs [8,9] have shown the strongest promise regarding the above-mentioned features. The challenge now is to realize entire front-end modules, e.g. a transimpedance amplifier (TIA) with a buffer amplifier in an optical-to-electronics communication system, or high-gain power amplifiers with power buffers in a measurement system.

This paper presents a significant leap forward towards amplifiers demonstrating a high gain-bandwidth-product as well as high linearity. Using a transistor with $f_t$, $f_{max}$ values of 350/450 GHz and a dual-stage amplifier subsystem, a measured GBP of >1.75 THz has been obtained with a gain of 24 dB over a frequency from DC to >110 GHz. These highest reported gain and GBP values are obtained using a transimpedance gain stage followed by a distributed amplifier for bandwidths above 110 GHz. The transimpedance stage serves as a versatile input stage, the input impedance of which can be adjusted when intended for use in optical transceivers to match the photodiode impedance or when in measurement systems 50 Ω characteristic impedance have to be realized.

## II. TECHNOLOGY

The circuit presented in this article is based on the 3-inch FBH transfer-substrate InP-DHBT technology as illustrated in Fig. 1. (a).

In this process, emitter, base and ground layers of the HBT are processed before the complete structure is flipped and bonded on a carrier silicon wafer using a BCB bonding process. After substrate removal, collector contacts are processed, aligned to the emitter contacts. In the first planarization step, the base, collector and emitter are connected to the first metallization layer G1. To realize the passives, SiN-based Metal-Insulator-Metal capacitors (MIMs) with a capacitance of 0.3 fF/µm² and NiCr resistors with 25 Ω/□ sheet resistance are used. Three routable metal layers

G3, G2, G1 and a ground metal layer Gd with respective thicknesses of 4 µm, 4.5 µm, 1.5 µm, and 3 µm serve the electrical connection. For thermal reasons, a diamond heat spreader is bonded on top of the final wafer [10].
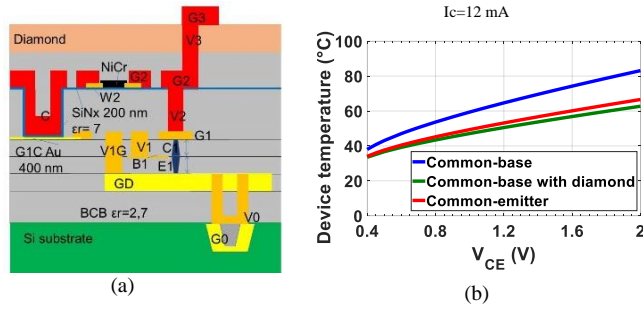


Fig. 1(a). Layer stack of the transferred-substrate process. (b) Self-heating improvement of common-base transistor (0.5 x5µm$^2$) using diamond heat spreader.

### A. Advantage of Using Diamond Heat Spreader

Due to the transistor stack and layout, the common-base configuration suffers significantly from thermal load as compared to the common-emitter configuration. The disparity in the thermal performance stems from the fact that in the common-emitter case the transistor is thermally grounded through the ground layer metallization. In the common base configuration, such a thermal path cannot be realized as the emitter contact serves as RF signal input. Hence by adding a diamond heat spreader, the performance of the common base transistor is significantly improved. This effect can be visualized by the TCAD simulations shown in Fig. 1(b). The simulation takes into account the vias, transistor self-heating as well as the diamond heat spreader. It is clear from the simulation that without a heat spreader the common base transistor can heat up to 80°C in comparison to only 57°C for the common emitter. By adding the diamond heat spreader, the device temperature for the common base can be lowered down to 62°C at VCE of 2 V.

### III. CIRCUIT DESIGN

This dual stage high gain amplifier MMIC consists of a high gain transimpedance stage and a power buffer stage in the form of a distributed amplifier [5]. The simplified circuit diagram is given in Fig. 2(a). The transimpedance stage is designed as a versatile gain stage with a gain of 12 dB and a bandwidth of 130 GHz. The low input impedance of the transimpedance stage mitigates the capacitive effect from the photodiode when it acts as a regular TIA, converting the current signal of the photodiode to a voltage signal with 50 Ω output impedance. When it is intended to be used in a measurement system, the input can be easily redesigned to match 50 Ω, with the sole purpose of voltage gain. The use of a transimpedance stage can, therefore, be optimized with minimum design effort.

The power buffer stage consists of a distributed amplifier with a simulated gain of 14 dB and a large-signal P$_{1dB}$ beyond 10 dBm and a bandwidth of more than 110 GHz [5]. With a diamond heat spreader, the circuit can achieve even higher linearity over the bandwidth as already presented in [11].

Therefore, it can be used as a buffer amplifier for high bandwidth applications which require amplification from near DC to 110 GHz and beyond. The distributed amplifier consists of five equally spaced cells, each cell containing a cascode-stacked transistor with reduced Miller capacitance and higher bandwidth. The cells act as loss compensators of the distributed lines, which accounts for the large bandwidth of the buffer and its high linearity. When cascaded together, they are intended to provide very high gain over the bandwidth of the amplifiers. The most important feature obtained in this way is having at the same time high gain, large bandwidth, and good linearity in a single subsystem. The chip photo of the realized InP-DHBT MMIC is shown in Fig. 2 (b).
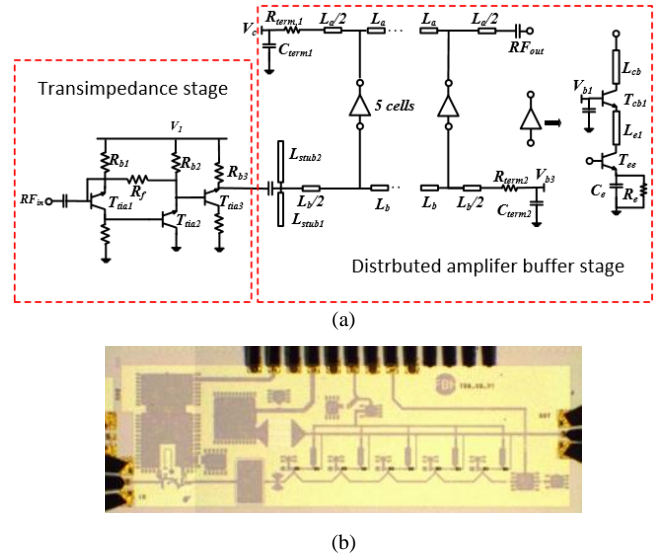


Fig, 2. (a) Simplified circuit diagram of the amplifier subsystem. (b) Chip photo (1.8×1 mm$^2$).

### IV. MEASUREMENTS AND DISCUSSION

### A. Small-Signal Measurements

The small signal performance was measured from DC to 110 GHz using on-wafer probing with 100 µm pitch and mTRL (multiline through-reflect-line) on-wafer calibration.
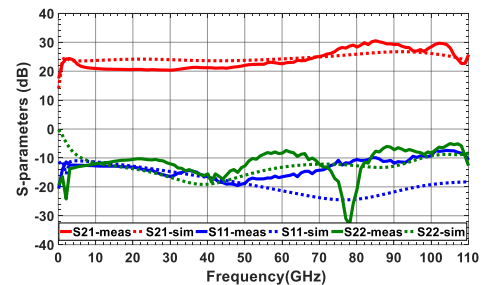


Fig. 3. S-parameter data with simulation (dotted line) and measurement values (solid lines)

Fig. 3 presents the simulated vs. measured data of the sub-system. The overall small signal gain, represented in the 50 Ω environment by S$_{21}$, varies between 21 and 30 dB with an average value of 24 dB. For the reflection coefficients, S$_{11}$ and S$_{22}$, the values are below -10 dB except between 50 to 70 GHz and 80 to 110 GHz where it reaches a value of -7 dB.

Table 1. Ultra-wideband DAs with bandwidth larger than 110 GHz (table is arranged in order of increasing GBP).

| Ref. | GBP (GHz) | Technology | MMIC Topology | BW (GHz | Gain (dB) | $P_{DC}$ (mW) | Linearity as $P_{1dB}$ or OIP3 (dBm) @Freq (GHz) |
|---|---|---|---|---|---|---|---|
| [13] | 278 | 40 nm GaN DHFET | Cascode | 120 | 7.3 | 448 | $P_{1dB}$= 15.5@20 |
| [12] | 390 | 50 nm InGaAs mHEMT | Cascode | 110 | 11 | 450 | $P_{1dB}$= 7@75 |
| [5] | >491 | 500 nm InP DHBT | Cascode | >110 | 13 | 129 | $P_{1dB}$= 10@ 5-110 |
| [11] | 597 | 500 nm InP DHBT | Tricode | 150 | 12 | 340 | $P_{1dB}$= 13@110 |
| [7,8] | 697 | 500 nm InP DHBT$^+$ | Tricode | 175 | 12 | 180 | $P_{1dB}$= 8.4@150 |
| [9] | 1483 | 250 nm DHBT | 2 Cascade-cascode | 235 | 16 | 117 | NA |
| [14] | 1550 | 250 nm SiGe HBT | Cascaded, cascode | 180 | 18.7 | 86 | $P_{1dB}$= 0@100 |
| **This work** | **>1743** | **500 nm DHBT** | **Feedback, distributed, cascode** | **>110** | **24** | **350** | **OIP3= 20-24@5-65** |

The measured forward gain $S_{21}$ shows slight deviations from simulation between 5 and 60 GHz. In order to have a better match, the circuit would have to be redesigned using EM co-assisted simulation for the entire cell. To be used as a receiver block in optical-to-electrical data converters, the deviation from linear phase for signal propagation has to be minimum. Fig. 4(a) shows the deviation from linear phase and the group delay of the amplifier subsystem. The deviation from linear phase remains within ±15° from near DC up to 80 GHz. This proves the quality of the circuit when to be used in optical-electrical data converters for data rates beyond 100 Gbps. For its use as transimpedance amplifier-buffer subsystem, the overall transimpedance has to be very large over the bandwidth. According to Fig. 4(b), an average value of 65 dB-Ω has been achieved within the bandwidth from near DC to 110 GHz frequency.
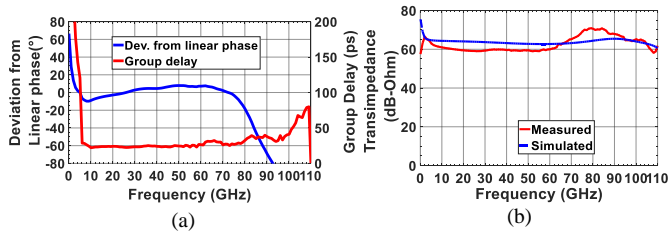


Fig. 4. (a) Group delay (ps) and deviation from linear phase (°) vs frequency and (b) transimpedance ($Z_{21}$) in dB-Ω vs. frequency (GHz)

### B. Large-Signal Measurements

The large signal measurements of the subsystem were carried out using a PNA-X network analyser. Since the signal distortion is a crucial component for receivers, IM3 measurements between 5 to 65 GHz were carried out rather than the saturated power measurements. This linearity measurement was done applying the standard procedure of using two signal tones, directly generated by the PNA-X, with a frequency separation of 1 MHz. The input and output power and that of the intermodulation products were recorded for the fundamental and 3rd harmonic, compensating the path losses, e.g. in probes, cables and attenuator. The fundamental and 3rd harmonic data are plotted in Fig. 5(a) for the frequency of 35 GHz. The 10 dB/dec slope of the fundamental output power data and the 30 dB/dec slope describing the 3rd harmonic data cross at OIP3 = 23 dBm. With the same

approach, the OIP3 points have been extracted from 5 to 65 GHz and plotted in Fig. 5(b). The OIP3 varies between 20 and 24 dBm, which is very high for this class of subsystem (with beyond 110 GHz bandwidth) and has been demonstrated so far in only a single broadband circuit [11] with OIP3 = 24 dBm. This high value of OIP3 is indicative of the linearity, which is very high and essential for such broadband systems. Moreover, the value remains constant over the frequency which is unlike other previous reports, where linearity degrades when increasing measurement frequency.
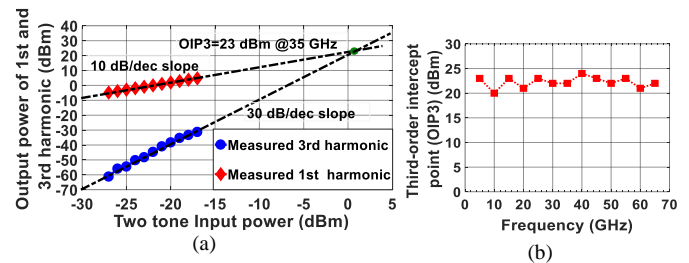


Fig.5. (a) Output third-order-intercept point (OIP3) for 35 GHz and (b) OIP3 as a function of frequency between 5 and 65 GHz.

With reference to Table 1, this work has the following merits that signifies its unique contribution to the literature. First of all, it demonstrates the highest GBP reported for any wideband MMIC circuit or subsystem with beyond 110 GHz bandwidth. Secondly, very high linearity is achieved together with good group delay behaviour, as required in optical-to-electrical receivers, for instance.

### V. CONCLUSIONS

The work presented demonstrates a receiver subsystem integrating a multipurpose amplifier and a power buffer in InP DHBT technology. Not only that it achieves the highest GBP so far, it does so with high linearity, relatively low power consumption, low signal phase distortion and a broadband input-output match. The results show the potential of highly complex multi-circuit integration in InP DHBT based MMICs, for transceiver systems operating in the mm-wave to Terahertz frequency range.

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