

# On Structure and Implementation of Algorithms for Carrier and Symbol Synchronization in Software Defined Radios

fred harris

College of Engineering, San Diego State University, San Diego, CA, USA  
[fred.harris@sdsu.edu](mailto:fred.harris@sdsu.edu)

Chris Dick

Xilinx Inc., 2100 Logic Drive, San Jose, CA 95124, USA  
[Chris.dick@xilinx.com](mailto:Chris.dick@xilinx.com)

## Abstract

Synchronization techniques based on DSP implementations are often digital emulations of their analog prototypes. Such solutions do not include structures and algorithms responsive to DSP system considerations and implementation strengths and weaknesses. We present a number of unconventional algorithms and structures used in carrier and timing recovery schemes. Multirate signal processing, polyphase filter structures, and CORDIC subsystems are at the heart of efficient first principle DSP based solutions to carrier recovery, matched filtering, timing recovery, and phase detection tasks required for synchronization.

## 1. Introduction

Digital Signal Processing has become the standard method of signal conditioning and signal processing in receivers of many synchronous communication systems. These systems require acquisition and tracking of a carrier and a timing clock from the received signal when neither carrier nor clock is present. Synchronization techniques abound with clever ad-hoc methods developed by clever designers. These sub-optimal synchronization techniques emerged concurrently with the development of the theoretical basis of synchronization processes with many techniques developed prior to the heavy reliance upon DSP. As the transition to DSP occurred, analog based synchronization schemes often survived the change and were implemented as digitized versions of the analog prototype technique. A lesson to be learned in developing DSP based solutions is that it may be imprudent to emulate analog solutions. Often techniques rendered in an analog prototype contain legacy implementation compromises that can be avoided in DSP based solutions. In addition, DSP offers a number of options and solutions not previously available to the analog system designer.

A simple example to cite is that an error signal can be derived in a DSP based phase locked loop (PLL) from the ATAN of a detected angle as opposed to approximating the angle by the SINE of the angle as is the common practice in an analog based PLL. Of course we must obtain the output of the ATAN without performing the ATAN, a computationally unattractive option if implemented in the obvious manner. Another

example we can cite is early-late gates used to extract timing information in analog timing recovery loops. The difference between the outputs of the early gate and the late gate drives the loop in the direction to set the difference to zero. We recognize that the early-late gate difference forms an estimate of the derivative of the matched filter output. Thus rather than form three filters, the matched filter and bracketing early and late matched filters, we can build two filters, the matched filter and the derivative-matched filter.

It makes sense to review signal-processing tasks performed in the analog world with the naïve perspective of questioning, "What function do we desire from the operation as opposed to what function do we obtain from the operation". In this light we review various processing tasks addressed in receiver designs and present a number of algorithm and hardware structures that convey the desired outputs more directly. These systems may offer significant performance and implementation benefits in modern hardware and software defined radio systems. We first review conventional receiver structures and their digital counterparts. We then examine carrier and timing recovery schemes in terms of modern DSP based implementations. Multirate signal processing and polyphase filter structures form the core of timing recovery schemes, while the CORDIC structure forms the core of down-conversion and phase detector functions required for carrier synchronization.

### 1.1 First Generation Receiver

Figure 1 presents the block diagram of the signal conditioning performed in a first generation receiver used in modern communication systems. It includes a section to perform analog preconditioning, an interface segment to convert the preconditioned data to a sampled data representation, a digital post conditioning segment to minimize the contributions of channel distortion and noise to the output signal, and a detector to estimate the parameters of the modulated signal. The Detector also supplies feedback information to a carrier recovery loop, a timing recovery loop, and the equalizer controller. The carrier recovery loop aligns the frequency and phase of the controlled oscillator (in the final down converter) to the carrier frequency and phase of the received signal. Similarly, the timing re-

covery loop aligns the frequency and phase of the sampling clock so that the position of the data samples at the output of the digital block coincide with the time location of the maximum eye opening.

Now we comment on weaknesses in the standard receiver structure. Our first concern is the analog components in the signal-conditioning path. We note that since there are two paths in the quadrature down-converter their components require a specified degree of gain and phase balance (or matching) to assure signal fidelity. We know that the degree of matching is limited by manufacturing tolerances and further that the degree of matching tends to degrade with time and temperature. Our second concern is the analog components in the feedback paths of the carrier and timing loops. Analog signals are required to control the VCOs of the carrier and timing recovery loops. The levels of the control signals are determined by the digital loop filters implemented in the DSP segment of the receiver. The level of the digital control signals must be brought to the analog domain via Analog to Digital Converters (ADC). The support hardware required to operate the ADCs include analog smoothing filters, registers for word framing and latching, and data and control signal lines. It would be nice to drop this hardware.

## 1.2 Second Generation Receiver

In retrospect, it almost seems silly to return to the analog world with control signals to modify signals residing and monitored in the digital world. With this thought in mind, we are led to the architecture of figure 2. In this version of the receiver the ADC is positioned to be the interface to the analog signal at the I-F stage. The sampling and quantization occurs prior to the quadrature down conversion. We have two options here. In the first option, we select a sample rate satisfying the Nyquist criterion for the maximum frequency of the I-F stage. In the second option we select a sample rate satisfying the Nyquist criterion for the two-sided bandwidth of the I-F stage, while intentionally violating the Nyquist criterion for the I-F center frequency. Let us examine both options for a specific example such as for an I-F center frequency of 25 MHz with a two-sided bandwidth of 6 MHz containing a signal with a 5 MHz symbol rate.

### 1.2.1 First Option: Direct Sampling

For the first option defined above, we select a sampling rate to satisfy the Nyquist criterion by satisfying the following equation:  $f_s > 2 (25 + 3) \text{ MHz} = 56 \text{ MHz}$ . We must always select a sample rate that allows for excess spectral interval to support a transition bandwidth separating the spectral masses. This margin is typically on the order of 10 to 20 percent over the minimum sample rate, and for this example is in the neighborhood of 62 to 67 MHz. Now we have a chance to be creative, here is where art and science meet. We may

select a sample rate to be an integer multiple of the symbol rate such as 65, 70, or 75 MHz (multiples of 13, 14, & 15 respectively). This selection might have advantages later in the timing recovery process as we resample to the symbol rate. We may also select the sample rate to be an integer multiple of the I-F center frequency such as 75 or 100 MHz (multiples of 3 & 4 respectively). This selection assuredly has advantages in the subsequent quadrature down conversion process. In particular, the input sample rate is often chosen to be 4-times the I-F center frequency, which for our example is 100 MHz. As a result of this choice, the down conversion requires only four trivial values of the complex exponential to be applied to the sample data,  $\exp(j 0)$ ,  $\exp(-j 2\pi/4)$ ,  $\exp(-j 4\pi/4)$ , and  $\exp(-j 6\pi/4)$ , or  $(1+j0)$ ,  $(0-j1)$ ,  $(-1+j0)$ , and  $(0+j1)$ , or if you would rather  $j^0, j^{-1}, j^{-2}$ , and  $j^{-4}$ .

The digital down conversion, whether obtained by trivial heterodynes from cleverly chosen locations on the unit circle, or by brute force complex scalar products from arbitrary locations on the unit circle, is never beset with the gain and phase balance problems associated with analog mixers. The balance of the multipliers performing the products is related only to the number of bits in the product, an easily selectable parameter. Further note, that the digital multipliers are actual product devices unlike the analog mixers that are in fact time varying impedances (or switches) that perform heterodynes with all harmonics of the mixing frequency.

### 1.2.2 Second Option: I-F Sub-Sampling

In the second option defined in the second-generation receiver we can select the sample rate to intentionally alias the I-F frequency to a lower frequency such that the aliases from the positive and negative spectral regions do not overlap. A common trick is to have the sample I-F frequency alias to the quarter sample rate. This occurs when the sample rate satisfies the following equation for an arbitrary integer K:  $K f_s + \{1/4\} f_s = f_{IF}$ . The solution of this expression for K=0 was cited in the previous section and we now consider the case for K=1. Then  $(5/4)f_s = f_{IF}$  or  $f_s = 20 \text{ KHz}$ . Sampling the 25MHz I-F frequency at 20 MHz rate will result in an aliasing to 5 MHz or  $1/4$  of the sample rate. As indicated in the previous section, the quadrature translation from this frequency is trivial.

After the down digital down conversion, the sampled signal is filtered to the signal bandwidth (plus any frequency offset uncertainty) and then down sampled to the reduced bandwidth's Nyquist rate such as 10 MHz for this ongoing example. The signal sampled at 100 MHz, would be translated to base band, filtered, and down sampled 10-to-1. The signal sampled at 20 MHz would alias to 5 MHz, then be translated to base band, filtered, and down sampled. At this point, after the

down sampling thus operating at the lower sample rate, a tight carrier recover loop can remove any frequency offsets related to Doppler or local oscillator drift.

### 1.3 Third Generation Receiver: Polyphase Filters

The common theme in the second-generation receiver is that the sampled signal is translated, filtered and down sampled after being collected and sampled as a real signal from the I-F stage. The sequence of operations consisting of translate, filter, and select sample rate is the digital version of the analog operations performed in the first-generation receiver. We have access to other DSP unique solutions. Rather than move the desired band to base band with a complex digital heterodyne, we can move the base band filter to the desired center frequency and perform the filtering to reduce the bandwidth at the digital I-F frequency.

The reduced bandwidth signal, drawn from the I-F filter, can be down-sampled M-to-1, to its appropriate Nyquist rate  $f_s/M$ . The down sampling aliases the center frequency to a new spectral position which is the I-F frequency minus an integer multiple of the new output sample rate. This is shown in the following expression:  $f_{\text{alias}} = f_{\text{IF}} - K f_s/M$ . When the I-F frequency is positioned at a multiple of the output sample rate, the down sampling aliases the frequency directly to base band. If the signal is offset from a multiple of the output sample rate, the aliasing will deliver the signal to base band plus the offset. The offset can then be removed with a carrier recovery scheme operating at the reduced sample rate. The advantage of this scenario is that the spectral translation performed by the carrier recovery loop occurs after the filtering at the low output rate rather than before the filtering at the high input rate.

Note that the I-F filter has a complex impulse response as a result of the complex translation and consequently has a non-Hermetian spectral response. This means the digital filter does not have a negative frequency image, which permits the filter output to be down sampled without concern for the positive and negative frequencies overlapping as a result of the aliasing,

What we have accomplished to this point in this section is slide the heterodyne through the filter and through the re-sampling switch so that it occurs at the reduced output rate. We now continue our rearrangement process by sliding the re-sampling switch through the filter so that the re-sampling occurs prior to the filter rather than after. The structure resulting from this rearrangement is the commutated polyphase filter. This structure commutates the input to M stages of an M-path partition of the original prototype filter. Since the paths are operated sequentially, an efficient implementation constructs only one sub-filter that sequentially access the coefficients of the successive M-path partition.

A unique attribute of the down-sampling operation is that we can change the phase of the sample locations in the down sampled time series relative to the epochs in the series. If we are performing M-to-1 down sampling, we have access to the output time series with M-different sample phase offsets. We can use the existence of these M possible output series to affect a timing recovery process. Rather than have the timing recovery loop modify the locations of samples points during the ADC process, as done in first and second generation receivers, we can have loop control the phase of the re-sampling process in the re-sampling filter. Since the phase of the re-sampling filter is defined by the selection of the phase weights in the single path structure, the timing recovery process defaults to controlling an index pointer in the filter's coefficient space. We note that when the polyphase filter is used as part of the timing loop, the number of stages in the partition must be increased to satisfy the timing granularity requirements of the timing loop rather than the down sampling requirement. The structure of this third generation receiver that we have just described is seen in figure 3.

### 1.4 CORDIC Translator

When we use the re-sampling in the polyphase filter to effect both a spectral translation and a timing recovery process we obtain a complex base-band signal at the reduced sample rate, with the correct timing, but not with the correct carrier frequency and phase correction. This correction is performed on the low-rate complex offset base-band signal by a complex heterodyne after the polyphase filter and prior to the final processing performed by the equalizer and matched filter. The heterodyne requires four multiplies when performed here on the complex base-band signal as opposed to the two multiplies when performed on the real I-F centered signal. The complex multiply can be embedded in the Direct Digital Synthesizer forming the values of the complex exponential required for the down conversion. We manage this by substituting the data for the initial condition in a CORDIC algorithm that rotate the initial condition  $(X_0, Y_0)$  to the desired angle to form  $X_0 \cos(-)$  and  $Y_0 \sin(-)$ . We thus accomplish the de-rotation or final heterodyne without the need of a complex product. This option offers marked advantages when a system is implemented in an FPGA.

## 2 Conclusions

We have presented a description of an evolutionary modifications in which the processes of translation, filtering, and re-sampling are rearranged and intertwined in clever ways that reduce operation count while increasing utility of the operations. The reference list presents some tutorial background material to help the novice and the seasoned practitioner master these new concepts.

### 3. References

Chris Dick, fred harris, and Michael Rice, "Synchronization in Software Radios: Carrier and Timing Recovery Using FPGAs", IEEE Symposium on Field Programmable Custom Computing Machines, Napa Valley, CA, 16-19 April 2000.

Chris Dick and fred harris, "FPGA Signal Processing Using Sigma-Delta Modulation:", IEEE Special Issue Magazine on Industrial Signal Processing, January 2000.

fred harris, "Band Edge Filtering and Processing for Timing and Carrier recovery", COMCON-7, Athens Greece, 28-June - 2-July 1999.

fred harris, "Oversampled Data Simplifies Design" EE-Times. 26-April 1999, pp. 76 & 96.

Chris Dick and fred harris, "Configurable Logic for Digital Communication: Some Signal Processing Perspectives", IEEE Communication Magazine, August 1999.

Les Sable and fred harris, "Using the High Order Nyquist Zones in the Design of Efficient Multichannel Digital Up converters", IEEE Personal Indoor and Mobile Radio Conference, Helsinki, Finland, 1-4 September 1997.

fred harris, "Digital Signal Processing in Radio Receivers and Transmitters", International Journal Wireless Information Networks (IJWINS) 1997.

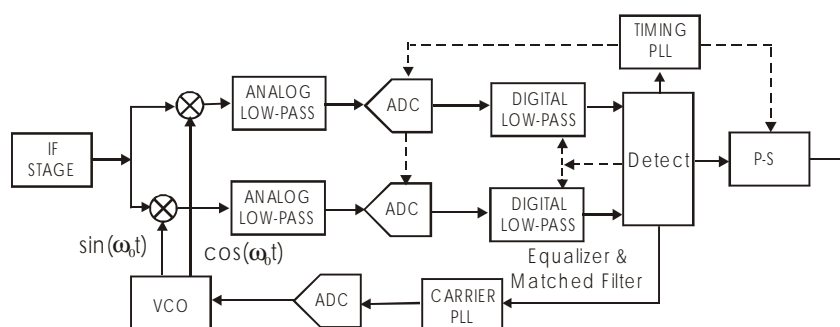


Figure 1. Block Diagram of Signal Processing Performed in First Generation Receiver

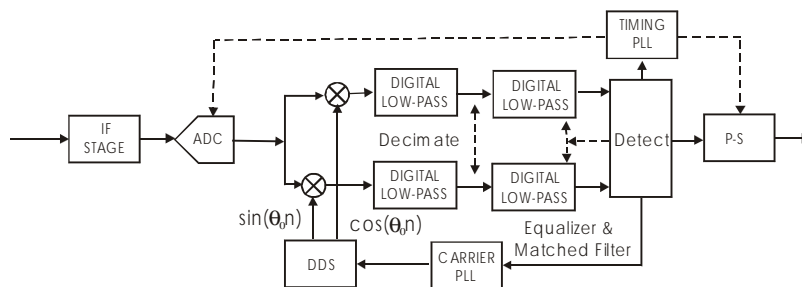


Figure 2. Block Diagram of Signal Processing Performed in Second Generation Receiver

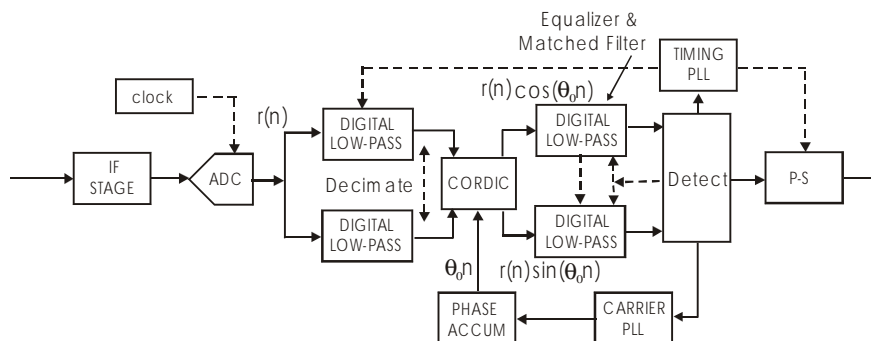


Figure 3. Block Diagram of Signal Processing Performed in Third Generation Receiver