

# Metal-oxide readout electronics based on Indium-Gallium-Zinc-Oxide and Indium-Tin-Zinc-Oxide for in-panel fingerprint detection application

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## Abstract

This work describes integrated readout electronics for on-panel fingerprint detection, focusing on two key building blocks: charge sense amplifier (CSA) and analog-to-digital converter (ADC). The CSA has been realized in a dual-gate self-aligned IGZO thin-film transistor (TFT) technology with channel length downsizing to  $3\mu\text{m}$ , enabling 1.3mm bezel size for the peripheral readout electronics and 1fps readout of a 1-Mpixel 500dpi sensor array. The ADC has been realized in two different transistor technologies, IGZO and Indium-Tin-Zinc-Oxide (ITZO). The ITZO ADC achieves a sampling rate of 1kS/s, which is 7.5x faster compared to the IGZO ADC, due to the larger mobility of ITZO.

## Author Keywords

In-panel; imager; sensor; readout; CSA; ADC; IGZO; ITZO; TFT

## 1. Introduction

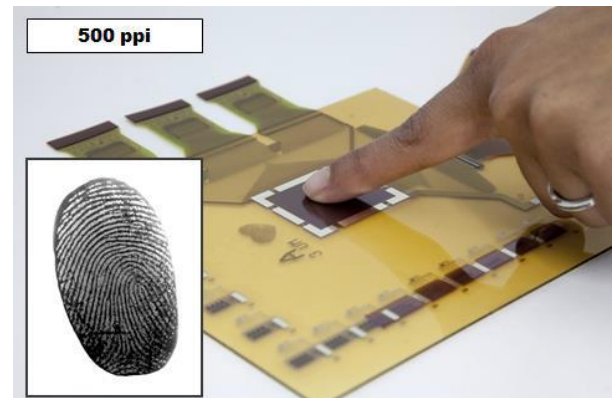
In this paper a readout system is proposed targeting high resolution sensor readout integrated side-by-side on a flat panel display. Fingerprint sensor arrays (Fig.1) [1] are becoming a mainstream security mechanism for mobile devices but is today available as autonomous component. The integration of the fingerprint sensor array together with the display [2]-[4] would benefit the footprint of the mobile device and the functionality, enabling detection of multiple fingers at once or even a palmprint. Moreover, the integration of the peripheral readout circuitry in panel side-by-side with the display peripherals is beneficial for resolution, connectivity and potential lower cost of the device. In Fig.1 the block diagram of the in-panel readout system is shown.

Analog to digital converters (ADC) and amplifiers on large area electronics technologies has been demonstrated in the past [5]-[11]. Metal-oxide technologies are preferable due to uniformity, very low leakage currents and cost. The ADC and analog blocks shown in literature are not sufficient in terms of speed or power dissipation and have relatively large footprint. This work focuses on fast and small footprint ADCs and charge sense amplifiers (CSA) to meet the readout time and lower the total bezel size of the sensor array.

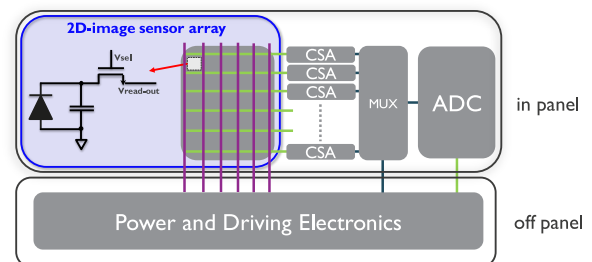
The next section discusses the various blocks of the readout system, after which the TFT technologies are explained. Subsequently, the different analog blocks are analyzed including measurement results. Finally, we evaluate the advantages and disadvantages of the different blocks in both ITZO and IGZO technologies and its feasibility for in-panel integration.

## 2. In panel readout system

In Fig. 2 the high-level block diagram of the in-panel readout



**Figure 1.** 500 ppi IGZO-OPD fingerprint sensor Stand-alone fingerprint scanner based on IGZO TFT backplane and BHJ OPD frontplane. The inset show a fingerprint image of 500 ppi taken with this scanner.

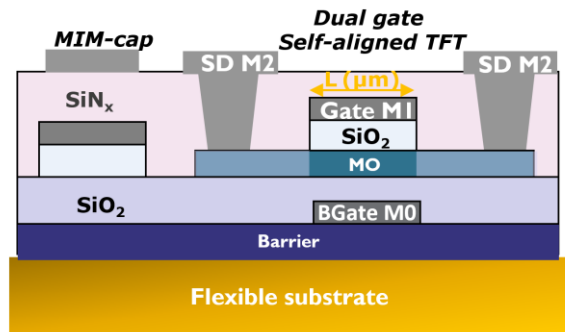


**Figure 2.** Block diagram of the proposed in-panel fingerprint sensor array with integrated CSA for each line, multiplexer (MUX) and ADC. Power and driving electronics remain off-panel.

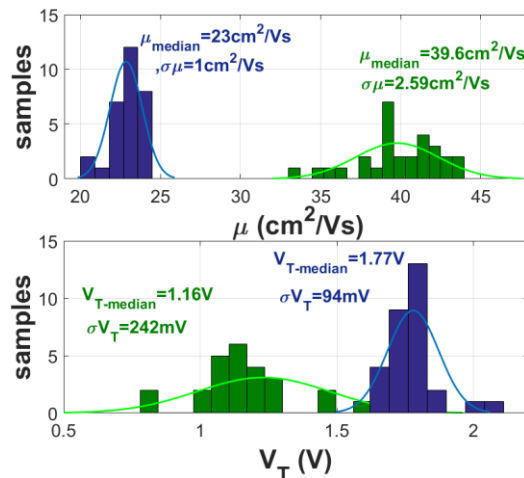
system is shown, detailing five main blocks: 2D-image sensor array, CSAs, multiplexers (MUX), ADC and off-panel power and driving electronics. Each column of the 2D-image sensor array is readout by a CSA. Multiple columns are subsequently converted to digital using a MUX and an ADC. The MUX enables a larger footprint of the ADC, up to 4 to 8 times larger compared to a single line ( $50\mu\text{m}$ ). Hence, the ADC needs to be 4 to 8 times faster with the integrated MUX. A 1-2 fps readout of 1Mpixel imager ( $1000 \times 1000$  pixels) sets a readout speed of 1-2kS/s per line. The introduction of the MUX increases this spec to 4-16kS/s depending on the order of multiplexing and the fps of the imager array.

## 3. Metal-oxide technology

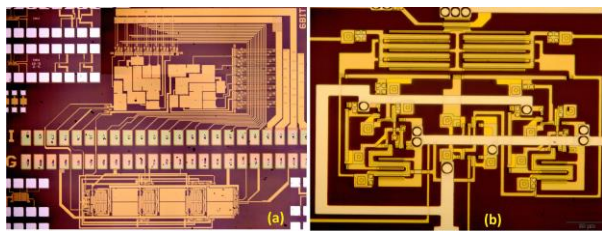
Fig. 3 depicts the cross section of the dual-gate self-aligned metal-oxide (MO) technology on a  $15\mu\text{m}$  thick polyimide film



**Figure 3.** Cross-section of dual-gate self-aligned metal oxide technology on flexible polyimide substrate.



**Figure 4.** Extracted effective mobility (due to dual gate structure) and threshold voltage from experimental data of 480/20 ( $\mu\text{m}/\mu\text{m}$ ) dual-gate self-aligned ITZO (green) and IGZO (blue) TFTs.



**Figure 5.** Microphotos of the (a) ADC and (b)  $L=3\mu\text{m}$  CSA on flexible substrate.

[12], [13]. The metal-oxide (IGZO or ITZO) TFTs are fabricated with two metal gates (M0, M1) and source-drain metal contacts

(M2). An additional metal layer (M3), not shown in cross section, is beneficial for footprint but also for performance and noise. The CSA experimental results shown in the following are designed with an extra metal layer, also used as anode layer.

Fig. 4 shows the extracted threshold voltage and mobility from transfer characteristics of 480/20 ( $\mu\text{m}/\mu\text{m}$ ) IGZO (blue) and ITZO (green) dual-gate TFTs. The IGZO TFTs exhibits a

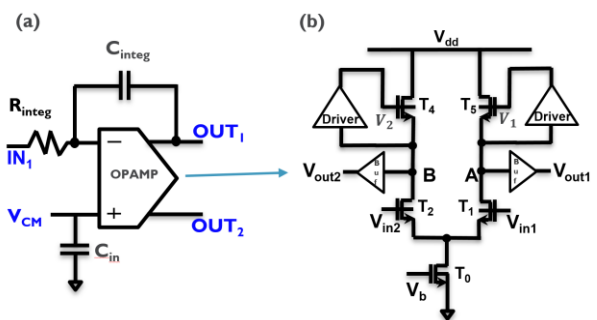
threshold voltage of 1.77V and effective dual-gate mobilities around  $23\text{cm}^2/\text{Vs}$  whereas the ITZO dual-gate TFT exhibits a threshold voltage of 1.16V and effective dual-gate mobilities around  $39.6\text{cm}^2/\text{Vs}$ . The apparent mobility is larger compared to literature because of the effect of having two gates controlling the channel. The 480/20 TFT is the largest footprint TFT used in the implemented designs. In Fig.5 microphotos of the (a) ADC and (b) the  $L=3\mu\text{m}$  CSA are shown.

**Table 1** In-Ga-Zn-O-TFT Differential Amplifiers Comparison (\*estimated)

Circuit	This work		2018 [11]	2012 [8]	2013 [10]	2014 [9]
Supply (V)	15	15	15	10.5	5	50
Gain (dB)	43	38.6	32	~21	18.7	19.2
GBW (kHz)	205	660	140	2	472	100*
pm (°)	52	27	53	50*	neg	46
Area (mm <sup>2</sup> )	0.28	0.07	0.3	<i>discr ete</i>	2.08	-
Substrate	PI	PI	PI		PI	glass
L (μm)	5	3	5	10	6	10

#### 4. Charge Sense Amplifier

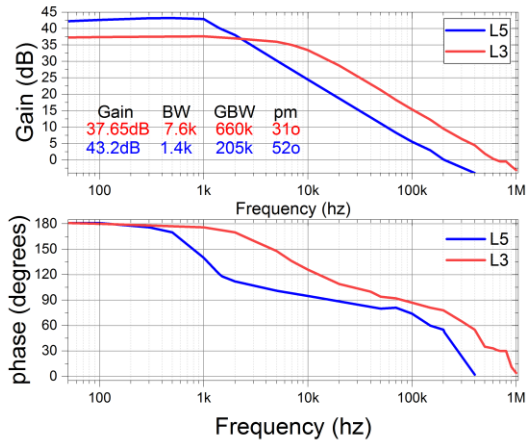
The first block connected to the readout lines of the image sensor is the CSA. The schematic of the CSA is shown in the Figure 6 (a). The schematic of the operational amplifier (OPAMP) used in the CSA is shown in Figure 6 (b). The OPAMP comprises a differential pair and a load that is driven by a two-stage buffer, initiated by a start-up circuit. The driver consists of two diode-connected load inverters as input and output stages. The output stage is driven by a start-up circuit to initialize the operation and provide  $\sim 1$  loop gain positive feedback bias to the n-type load of the differential amplifier such that  $V_G$  follows  $V_S$ . A buffer is also included at the output nodes



**Figure 6.** Schematics of (a) charge sense amplifier (CSA) and (b) the opamp schematic using dual-gate self aligned TFTs used in the CSA in (a).

A and B to increase the speed of the amplifier.

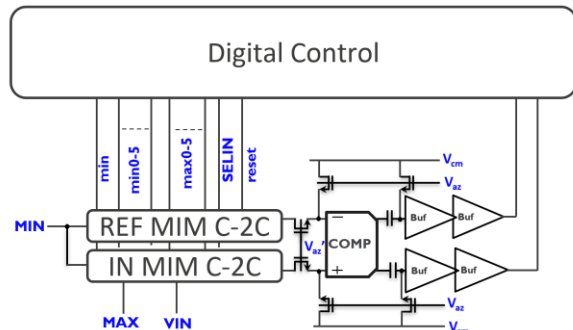
The experimental results of open-loop experiments are shown in Figure 7 for dual-gate self-aligned IGZO TFTs of  $L=5\mu\text{m}$  and  $L=3\mu\text{m}$ . The maximum gain for the  $5\mu\text{m}$  design is 43.2dB with a phase margin of  $52^\circ$ , whereas the  $3\mu\text{m}$  implementation results in a gain and phase margin of 37.65dB and  $31^\circ$  respectively. Both



**Figure 7.** Experimental bode plots of the OPAMP using dual-gate self-aligned IGZO technology for  $L=5\mu\text{m}$  and  $L=3\mu\text{m}$ .

parameters are critical for stable closed loop operation of an operational amplifier. The obtained bandwidth (BW) are 1.4kHz and 7.6kHz for 5 and  $3\mu\text{m}$  respectively. Gain-bandwidth reaches 205kHz and 660kHz for both designs. These specs are compared to earlier publications in the state-of-the-art Table 1.

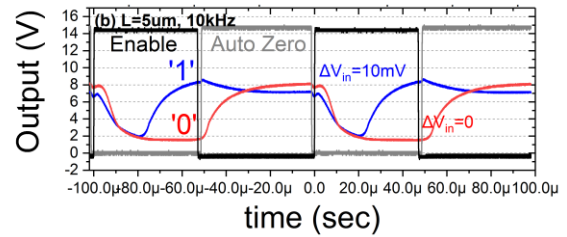
The footprint of the CSA can be decreased from  $0.28\text{mm}^2$  to  $0.07\text{mm}^2$  for the  $5\mu\text{m}$  and  $3\mu\text{m}$  designs with the capacitors. These footprints will result in a bezel width of 5.5mm ( $L=5\mu\text{m}$ ) and 1.3mm ( $L=3\mu\text{m}$ ) for a  $50\mu\text{m}$  pixel size.



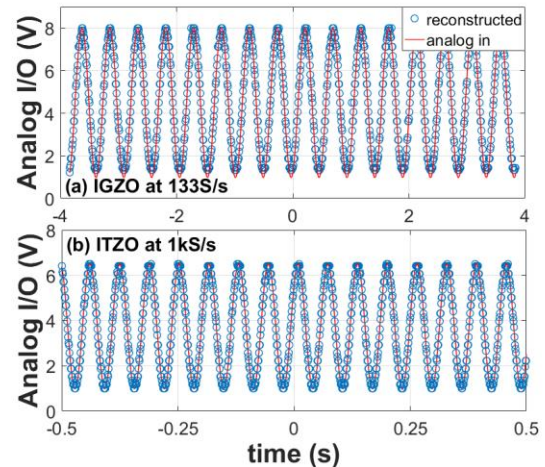
**Figure 8.** The implemented SADG TFT ADC block diagram driven with offset compensation.

## 5. Analog to Digital Converter

We selected the successive approximation architecture as ADC architecture for the dual-gate self-aligned technology. To leverage the 0.1% uniformity of metal-insulator-metal capacitors across  $150\text{mm}^2$  wafers, a C-2C architecture is chosen. The schematic of the C-2C dual-gate ADC is shown in Figure 8. The comparator is the most critical building block of the ADC for speed and accuracy, mainly determined by the offset of the comparator. To improve the accuracy of the comparator, open-loop offset cancellation is used. The response of a  $L=5\mu\text{m}$  dual-gate self-aligned TFT-based comparator at 10kHz for two inputs  $\Delta V_{in}=0$  and 10mV is shown in figure 9. The comparator with offset cancellation can distinguish a 10mV signal even though the  $V_t$  variation of the TFTs is one order larger.



**Figure 9.** Measured comparator output with auto-zero offset cancellation for designs using TFTs of minimum  $L=5\mu\text{m}$  at 10kHz.



**Figure 10.** (a) The analog input 2.061Hz sinewave signal to the ADC and the reconstructed output points from the digital output of the ADC at a clock frequency of 2kHz

Two variations of the ADC have been realized, differentiating in the used semiconductor (IGZO and ITZO). Experimental results of the reconstructed samples from a sinusoidal analog wave applied at the input of the IGZO and

ITZO ADC is shown in Figure 10. The IGZO ADC achieves 6bit resolution at a sampling speed of 133S/s at 15V power supply using a  $L=20\mu\text{m}$  comparator. The clock speed of the IGZO ADC is at 2kHz matching the bandwidth of the comparator, 15 clocks are required to complete the conversion. In this work, we describe two options to increase the sampling speed matching the application requirements: downscaling to  $5\mu\text{m}$  and switching to ITZO as semiconductor. The first validated solution to achieve faster sampling speed is to scale down the comparator to  $5\mu\text{m}$ , as indicated in Fig. 7. The  $5\mu\text{m}$  comparator can increase the sampling speed by 4 times compared to the  $20\mu\text{m}$ .

The second option is to adapt the design for ITZO, which have 0.5V lower  $V_t$  and double effective mobility compared to IGZO. These differences are depicted in the improvement in speed observed in Fig.10 (b). The ITZO ADC achieves a 5b resolution of the applied sinusoidal wave at 1kS/s sampling speed at 10V supply voltage. Combining, both ITZO and downscaling of the comparator will lead to sampling speeds above 4kS/s as required for the in-panel readout system.

## 6. Conclusion

This work discussed the proposed peripheral on-panel TFT-based circuits to readout on-panel fingerprint or palmprints side-by-side integrated with a flat panel display. Two critical blocks are discussed, being an analog to digital converter and charge sense amplifier. Two ADCs have been implemented, based on IGZO and ITZO TFTs. The ITZO ADC results in faster operating converters, reaching up to 1kS/s conversion rate. Two different CSAs have been implemented, downscaling the channel length from 5 $\mu$ m and 3 $\mu$ m. The 3 $\mu$ m version reaches faster amplification and enables a smaller bezel.

## 7. Acknowledgements

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