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RESEARCH ARTICLE

A Highly Efficient Low Power and Compact CCDD RFEH Rectifier Design With MOSFET-Modeled Capacitors and Bio-Inspired Metaheuristic Optimization for Wearable and IoT Applications

RUPAM BORA[1], (Student Member, IEEE), MANASH PRATIM SARMA[1], (Member, IEEE), LACHIT DUTTA[1], (Senior Member, IEEE), PRANJAL BARMAN[2], (Member, IEEE), AND BRIAN AZZOPARDI[3,4,5,6], (Senior Member, IEEE)

[1]Department of Electronics and Communication Engineering, Gauhati University, Guwahati, Assam 781014, India
[2]Assam Skill University, Mangaldoi, Assam, India
[3]Design Centre, The Foundation for Innovation and Research-Malta (FiR.mt), Birkirkara, Malta
[4]MCAST Energy Research Group, Institute of Engineering and Transport, Malta College of Arts, Science and Technology (MCAST), PLA9032 Paola, Malta
[5]Department of System and Control Engineering, Faculty of Engineering, University of Malta, Malta
[6]Azzopardi & Associates, Birkirkara, Malta

Corresponding author: Rupam Bora (rupambora13@gmail.com)

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ABSTRACT This paper presents a novel modified cross-coupled differential-drive (CCDD) rectifier designed for Radio Frequency Energy Harvesting (RFEH) applications. The proposed design incorporates MOSFET-modeled capacitors to reduce area consumption while maintaining a high power conversion efficiency (PCE). A comprehensive mathematical model was developed to analyze the behavior of the circuit, and the Walrus Optimization Algorithm (WaOA) was employed to optimize the transistor aspect ratios. The simulation results demonstrate that the modified rectifier achieves a maximum PCE of 93.24% at an input power of −17.5 dBm, significantly outperforming both the conventional and dual MOSFET-based configurations, particularly at low input power levels. Notably, the proposed design achieves a wide power dynamic range of 25 dB and occupies an ultra-compact area of 35.22μm^2, making it suitable for ambient RFEH scenarios. This work represents a significant advancement in RFEH technology, offering a more efficient and compact solution for powering low-energy devices such as Internet of Things (IoT) sensors and wearable electronics.

INDEX TERMS Cross-coupled differential drive rectifier, Internet of Things, low-power electronics, MOSFET-modeled capacitors, power conversion efficiency, RF energy harvesting, walrus optimization algorithm, wireless sensor networks.

I. INTRODUCTION

With the rapid expansion of the Internet of Things (IoT) and the deployment of wireless sensor networks (WSN), there is an urgent need for sustainable and maintenance-free power sources to support a vast number of low-energy devices. Radio Frequency Energy Harvesting (RFEH) systems have emerged as promising technologies for powering low-energy devices by converting ambient RF signals into usable energy. This method exploits the electromagnetic waves that pervade sources such as cellular networks, Wi-Fi routers, and broadcast transmitters, offering a sustainable solution for applications such as IoT devices, wireless sensors, and medical implants [1], [2]. RFEH systems typically consist of an antenna to capture RF signals, a rectifying circuit to convert the RF signal to DC, and a power management

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unit to store and regulate the harvested energy. Despite the generally limited amount of harvestable energy, advances in low-power electronics and efficient harvesting techniques have made this technology increasingly viable for powering sensors, IoT devices, and other small-scale applications in urban and industrial settings [2]. The early work of [3] on differential drive rectifiers for UHF RFIDs laid the foundation for modern cross-coupled differential-drive (CCDD) rectifier designs, which have since been adapted for ambient RF energy harvesting.

At the heart of RF energy harvesting systems lies a rectifier that converts captured RF signals to DC power. The efficiency of this conversion is crucial because it directly affects the amount of usable energy available to power devices, particularly in scenarios with weak RF signals [2]. High-efficiency rectifiers minimize power losses during the conversion process, enabling the energy harvesting of weak RF signals and expanding the effective range of energy harvesting systems. In addition, well-designed rectifiers can operate over a wide range of input power levels and frequencies, enhancing the adaptability of the system to various RF environments. By maximizing the power conversion efficiency (PCE), optimized rectifier designs contribute to the development of compact, cost-effective, and sustainable RFEH solutions, advancing their applications in IoT devices, wearable technology, and remote sensing [4].

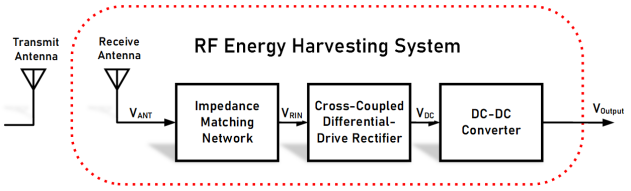

FIGURE 1. RFEH system block diagram.

CCDD rectifiers are an advanced class of rectification circuits designed to enhance the PCE and performance of RFEH systems. These rectifiers employ a unique topology that combines cross-coupling and differential drive principles, allowing bidirectional current flow and reducing the voltage stress on the components, thus improving overall efficiency [5], [6]. However, conventional CCDD rectifiers exhibit limitations, particularly in their dynamic range of PCE and performance at very low input power levels, which are common in ambient RFEH applications. Furthermore, these designs often require discrete components, increasing area consumption and design complexity, which pose challenges for integration into compact devices such as IoT sensors or medical implants [5], [7].

The increasing demand for ultra-low-power devices, such as IoT sensors and wearable electronics, underscores the need for RFEH systems that can operate efficiently at extremely low input power levels. Increasing the rectifier efficiency and reducing area consumption are essential for making these systems viable and scalable [2]. Recent research has focused on addressing these challenges using innovative design and optimization techniques. For example, [8] established fundamental analytical models for CCDD rectifiers using BSIM4 transistor models, providing closed-form equations for the output voltage and input resistance. Similarly, [9] developed models that accurately predicted rectifier performance under varying input conditions, achieving a precision of more than 90%. Furthermore, [10] proposed a hybrid RF-DC converter that combines CCDD with PMOS-only stages to reduce fabrication costs while achieving 45% PCE, and Grasso et al. [11] explored the co-design of differential drive rectifiers and inductively coupled antennas to optimize system performance

In RF energy harvesting systems, maintaining a high PCE across a wide range of input power levels remains a significant challenge, particularly for ambient applications in which the signal strength fluctuates. Traditional rectifier designs often struggle to adapt to these variations, leading to suboptimal performance. To address this, advanced optimization strategies have been developed, focusing on architectural innovations and adaptive techniques. To address the challenge of maintaining a high PCE over a wide range of input power levels, [12] proposed a CMOS cross-coupled differential drive rectifier design that achieves a wide dynamic range of PCE, making it particularly suitable for ambient RF energy harvesting applications. This approach improves efficiency by dynamically adjusting to varying input conditions and offers practical solutions for real-world deployment.

Threshold voltage compensation and biasing techniques have emerged as critical strategies for enhancing rectifier performance. Reference [13] introduced a fully differential CMOS bootstrap rectifier with dynamic threshold-voltage compensation, achieving a PCE of 71% at 434 MHz. Reference [14] used adaptive body biasing to dynamically adjust the PMOS threshold voltage, resulting in a peak PCE of 78.2% at −27.5 dBm. Reference [15] demonstrated a self-biased differential rectifier with enhanced dynamic range, achieving a sensitivity of −15.2 dBm for 1 V output and a peak PCE of 65%. Reference [16] proposed a CMOS rectifier with a cross-coupled latched comparator, achieving high efficiency for wireless power transfer, while [17] presented a modified cross-coupled rectifier that eliminates the Vth dependence, improving DC extraction efficiency. Reference [18] conducted a performance analysis of multistage CCDD rectifiers and provided insight into their efficiency and design considerations.

Architectural innovations have also expanded the capabilities of CCDD. Reference [19] proposed a differential RF front-end with an integrated step-up stacked transformer on the chip, demonstrating high efficiency in a 65-nm CMOS process. Reference [20] developed a reconfigurable RFEH system with dynamic path selection logic for optimized power conversion. Furthermore, [21] presented a fully integrated CMOS RFEH front end that uses a stacked step-up transformer as an IMN integrated on-chip with a CCDD rectifier, achieving a sensitivity of −20 dBm at a 1 V output. Reference [22] introduced a measurement-based technique to

design IMNs for differential drive rectifiers, which enhances system efficiency.

The adaptability of the frequency band is another area of focus, with [23] introducing an improved CCDD rectifier for quad-band operation, achieving a conversion efficiency of over 80 % from RF to DC in the FM-100, DTV-600, GSM-1800, and WiFi-2400 frequency bands. Reference [24] developed a dual-antenna RF energy harvester for biomedical applications, achieving 75.2% efficiency at low input power. Reference [25] presented a dual-band rectifier operating at 13.56 MHz and 915 MHz, demonstrating the potential for multi-band systems in wireless power transfer. Reference [26] presented a triple-band RFEH system operating at 900, 1900, and 2400 MHz, with a power range of −11 to 7 dBm and 99.99% peak tracking efficiency.

Specialized designs have also been developed for specific applications, such as [27] an RF energy harvesting system for Wi-Fi 6/6E bands targeting implantable medical devices and [28] a body-coupled communication system with 93% voltage conversion efficiency for neural interfaces. Reference [29] designed a DC-DC converter with a rectifier and resonator for wireless charging in vehicles, demonstrating versatility in energy harvesting applications. Reference [30] presented a 100 MHz cross-coupled stacked rectifier integrated into an isolated DC-DC converter, which achieved high efficiency.

Performance optimization strategies are crucial for addressing the challenges associated with low-power RF signal processing. Reference [31] developed a two-stage cross-coupled rectifier with impedance-aware sizing, achieving a peak power harvesting efficiency of 31.1%. Reference [32] introduced a differential drive cross-coupled bridge rectifier with reverse DC feed self-body biasing, achieving a PCE peak of 72. 2% at 953 MHz. Reference [33] fabricated a three-stage cross-coupled active rectifier-booster integrated circuit, eliminating discrete diodes, while [34] introduced a high-efficiency rectifier with LC source degeneration employing coupled inductors for voltage reshaping.

Despite these advancements, conventional CCDD rectifiers still face challenges in achieving high efficiency at ultra-low input power levels and reducing area consumption for compact integration. This study aims to address these limitations by proposing a modified CCDD rectifier design that enhances performance, particularly at low input power levels. The proposed modification leverages MOSFET-modeled capacitors for gate coupling, which occupy less area than traditionally modeled capacitors. The design is optimized using bio-inspired algorithms to achieve superior performance under constrained conditions. By improving the PCE and dynamic range while reducing area consumption and design complexity, this study contributes to the development of more efficient and scalable RF energy harvesting systems for emerging IoT and wireless sensor network technologies.

The key contributions of this research article are as follows:

- A modified CCDD rectifier design incorporating MOSFET-modeled capacitors for gate coupling is proposed.
- Design optimization by dint of bio-inspired algorithms to enhance performance under constrained conditions.
- Improved PCE and dynamic range are achieved, particularly at ultra-low input power levels.
- Reduced area consumption and design complexity facilitate compact integration in IoT and wireless sensor network applications.

The remainder of this paper is organized as follows. Section II describes the proposed rectifier design and mathematical modeling. Section III presents the optimization methodology using Walrus Optimization Algorithm (WaOA). Section IV discusses simulation results and performance comparison. Section V provides the summary and conclusions.

II. RECTIFIER DESIGN

The novel modified CCDD rectifier, as illustrated in Figure 4, employs an innovative design approach that uses MOSFET-modeled capacitors. This is achieved by connecting the gate and source terminals of the MOSFETs to create a capacitive effect, effectively integrating the capacitive function into the MOSFETs. By eliminating the need for discrete passive components, such as external capacitors, this approach significantly reduces the overall area required for the circuit and simplifies the design. The modified circuit maintains the enhancements in current drive and circuit efficiency observed in previous configurations while addressing the limitations of traditional rectifier designs, particularly in terms of space consumption and design complexity. This integration not only streamlines the layout but also enhances the suitability of the circuit for applications in which compactness and performance are critical.

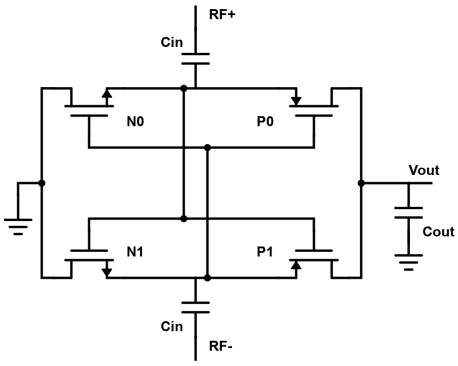

FIGURE 2. Conventional rectifier circuit.

The conventional CCDD rectifier, as detailed in [35], serves as the foundation, with its bridge-structured differential CMOS configuration being effective for RFID applications. However, limitations in current drive, area consumption, and performance at low input power levels

necessitated advancements, leading to the exploration of dual configurations and ultimately a novel modified design.

The conventional CCDD rectifier, shown in Figure 2, employs a cross-coupled differential CMOS bridge structure suitable for low- and high-frequency operations, including UHF RFIDs. Its operation involves generating a common mode voltage at the internal RF nodes, which is approximately half the steady-state output DC voltage and acts as a static gate bias to compensate for the threshold voltage (Vth). This compensation improves the rectification efficiency by reducing the effective turn-on voltage of the transistors.

In addition, the differential mode signal dynamically biases the transistor gates. During forward bias, the gate voltage is positively biased, lowering the ON resistance and improving the current drive. During reverse bias, the gate voltage decreases rapidly, minimizing the reverse leakage currents. The rectifier reaches a steady state when the forward-transferred charges (from the input signal) balance the reverse-transferred charges (leakage) and the charges dissipated by the output load. Initially, upon applying the input power, the output DC voltage and the internal node voltages increased until equilibrium was reached, achieving a maximum PCE of 67.5% at 953 MHz with an input power of −12.5 dBm [3].

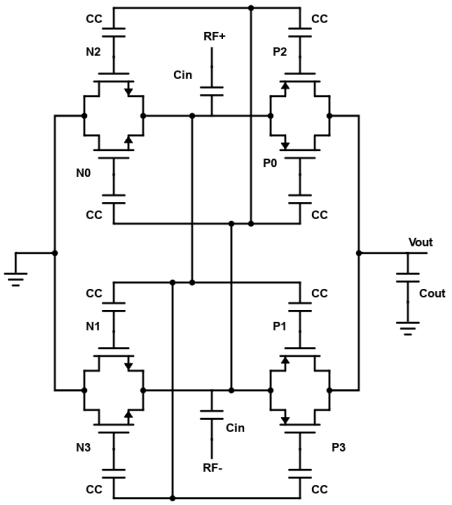

FIGURE 3. Dual rectifier circuit.

To address the limitation of low current drive in the conventional design, a dual MOSFET-based configuration was explored in [36], as shown in Figure. 3. This design modifies the conventional CCDD topology by incorporating a dual MOSFET arrangement back-to-back, thereby enhancing the current drive capability. The dual configuration achieved significant performance improvements, with a maximum PCE of 89. 41% at −2 dBm input power and a satisfactory PCE of 70.17% at −8 dBm, demonstrating robustness across a range of input power levels.

However, this improvement comes at a cost. The dual configuration increases area consumption and component count, particularly for a single-stage rectifier. This trade-off makes it less suitable for applications that require compact, space-efficient designs, such as IoT sensors or medical implants, where minimizing the physical footprint is critical.

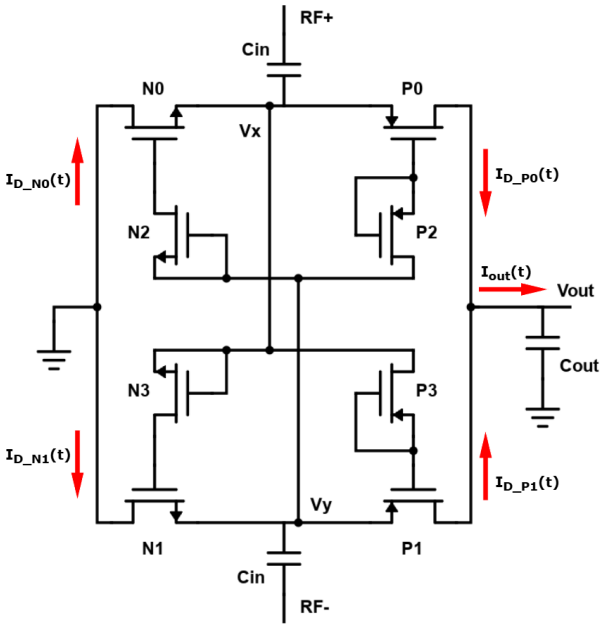

FIGURE 4. Modified design of the proposed rectifier circuit.

The trade-off between an improved current drive and increased area in the dual configuration highlights the need for a design that can maintain or improve the PCE while reducing area consumption. A novel modified CCDD rectifier, as illustrated in Figure 4, was developed to address these challenges. The high efficiency and wide dynamic range of the modified CCDD rectifier originate from enhanced gate–source coupling and optimized transistor sizing. The MOSFET-modeled capacitors increase the effective gate drive during each RF half-cycle by directly coupling the RF signal to the transistor gates. This coupling lowers the effective switching threshold voltage of the cross-coupled devices, enabling earlier turn-on at low RF input amplitudes. As a result, rectification begins at lower input power levels, improving low-power sensitivity and extending the dynamic range toward weak ambient RF signals. The key innovation lies in the use of MOSFET-modeled capacitors for gate coupling, which eliminates the need for discrete passive components, thereby reducing the layout area and simplifying the design.

This approach leverages the inherent capacitive properties of MOSFETs by connecting the gate and source terminals to create a capacitive effect, as previously described. By integrating the capacitive function into the MOSFET design, the modified circuit maintains a high current drive

and operational efficiency while achieving a more compact footprint. This design not only addresses the area constraints associated with traditional rectifier designs but also enhances the performance characteristics of previous configurations, making it suitable for low-power, space-constrained applications.

A. MATHEMATICAL MODELING

Mathematical modeling of the modified CCDD rectifier circuit is essential for understanding and optimizing its performance, particularly when MOSFET-modeled capacitors are incorporated. This modeling involves obtaining expressions for key parameters, such as output power, PCE, and the overall cost function, to quantify the improvements introduced by these capacitors. The process begins by converting the input power from decibels relative to one milliwatt (dBm) to watts using the relation.

$$P_{\text{in\_W}} = 10^{\left(\frac{P_{\text{in\_dBm}}-30}{10}\right)}, \tag{1}$$

This ensures consistent power calculations. From this, the RF voltage amplitude is calculated assuming a standard impedance 50 Ω as

$$V_{\text{RF\_amplitude}} = \sqrt{2 \cdot P_{\text{in\_W}} \cdot 50}, \tag{2}$$

In the circuit-level simulations, the RF excitation source is configured with a fixed source impedance of 50 Ω in the Cadence Virtuoso Analog Design Environment. This explicitly enforces a matched RF source condition, representing a standard RF signal generator or antenna interface. Under this condition, the conversion from input power to RF voltage amplitude used in (2) is valid and consistent with the simulated circuit environment.

and the RF voltage signal is modeled as a sinusoidal wave,

$$V_{\text{RF}}(t) = V_{\text{RF\_amplitude}} \cdot \sin(2\pi f t), \tag{3}$$

where f is the signal frequency. Several constants are integral to this modeling, including K_n and K_p (transconductance parameters for NMOS and PMOS transistors, in A V^{-2}), λ (channel-length modulation parameter, in V^{-1}), V_t (thermal voltage, in V), n (subthreshold slope factor), μ_n and μ_p (mobility for NMOS and PMOS, in $\text{m}^2\,\text{V}^{-1}\,\text{s}$), ϵ_{si} (permittivity of silicon, in F m^{-1}), q (elementary charge, in C), N_{ch} (channel doping concentration, in m^{-3}), Φ_B (surface potential barrier, in V), V_{off} (offset voltage, in V), λ_{sub} (subthreshold channel-length modulation), γ (body effect coefficient), and ϕ (surface potential, in V). A critical component is the capacitance of the depletion layer per unit area, C_d, given by

$$C_d = \sqrt{\frac{\epsilon_{si} \cdot q \cdot N_{ch}}{2 \cdot \Phi_B}}, \tag{4}$$

This is vital for understanding the capacitive behavior of MOSFET-modeled capacitors. The threshold voltage in the BSIM4 model is expressed as

$$V_{th} = V_{th0} + \Delta V_{th\_SCE} + \Delta V_{th\_DIBL} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right), \tag{5}$$

where V_{th0} is the zero-bias threshold voltage, ΔV_{th_SCE} and ΔV_{th_DIBL} account for short-channel effects and drain-induced barrier reduction, respectively, and the body effect is incorporated through γ, ϕ_F (Fermi potential), and V_{SB} (source-bulk voltage). The drain current in the BSIM4 model is formulated as

$$I_D = I_{DS0}\left(1 + \lambda V_{DS}\right), \tag{6}$$

where I_{DS0} is the drain current at zero drain-source voltage, and λ is the channel length modulation parameter that captures the increase in the drain current with the drain-source voltage V_{DS}. This detailed mathematical framework enables a quantitative assessment of the performance enhancements of the modified CCDD rectifier, facilitating its optimization for various applications.

In the BSIM4 model, mobility degradation due to vertical and lateral electric fields in the MOSFET channel is modeled with high precision, which is essential for the accurate simulation of sub-100 nm transistors in circuits such as the modified CCDD rectifier. A simplified representation of the mobility degradation is given by the following equation:

$$\mu = \frac{\mu_0}{1 + \theta V_{GS}}, \tag{7}$$

where, μ is the effective mobility, μ_0 is the low-field mobility, θ is the mobility degradation coefficient, and V_{GS} is the gate-source voltage. This equation captures the reduction in mobility as the gate voltage increases, leading to enhanced carrier scattering, which affects the rectifier efficiency. The threshold voltage, which determines the onset of conduction, is modeled differently for NMOS and PMOS transistors. For NMOS, it is given by

$$V_{th,n} = V_{th0,n} + \gamma_n\left(\sqrt{2\phi + V_{bs}} - \sqrt{2\phi}\right), \tag{8}$$

where V_{th0} is the zero-bias threshold voltage, γ is the body effect coefficient, ϕ is the surface potential, and V_{bs} is the bulk source voltage. For PMOS, the threshold voltage is

$$V_{th,p} = V_{th0,p} - \gamma_p\left(\sqrt{2\phi + V_{bs}} - \sqrt{2\phi}\right), \tag{9}$$

with the negative sign reflecting the opposite polarity of the body effect, making PMOS transistors easier to turn on as V_{bs} increases. The drain current varies according to the operating regions: subthreshold, triode, and saturation. In the subthreshold region ($V_{gs} < V_{th,n}$ for NMOS or $V_{sg} < |V_{th,p}|$ for PMOS), the current is exponentially dependent on the gate-source voltage. For NMOS, the pre-exponential factor is

$$I_{0,n} = \mu_n \cdot C_d \cdot V_t^2 \cdot \left(\frac{W_n}{L_n}\right) \exp\left(\frac{-(0.586 - V_{off,n})}{n \cdot V_t}\right), \tag{10}$$

and the drain current is

$$i_d = I_{0,n} \exp\left(\frac{V_{gs} - V_{th,n}}{nV_t}\right)\left(1 - \exp\left(-\frac{V_{ds}}{V_t}\right)\right). \quad (11)$$

For PMOS, the pre-exponential factor is

$$I_{0,p} = \mu_p \cdot C_d \cdot V_t^2 \cdot \left(\frac{W_p}{L_p}\right) \exp\left(\frac{-|0.559 - V_{off,p}|}{n \cdot V_t}\right), \quad (12)$$

and the drain current is

$$i_{sd} = I_0 \exp\left(\frac{V_{sg}}{nV_t}\right)\left(1 - \exp\left(-\frac{V_{sd}}{V_t}\right)\right) \left(1 + \lambda_{\text{sub,p}} V_{sd}\right), \quad (13)$$

including the channel length modulation. In the triode region ($V_{ds} < V_{gs} - V_{th,n}$ for NMOS or $V_{sd} < V_{sg} - |V_{th,p}|$ for PMOS), the current is linear, with the NMOS current as

$$i_d = \left(\frac{W_n}{L_n}\right) K_n \left(\left(V_{gs} - V_{th,n}\right) V_{ds} - \frac{1}{2} V_{ds}^2\right), \quad (14)$$

and PMOS as

$$i_{sd} = \left(\frac{W_p}{L_p}\right) K_p \left(\left(V_{sg} - |V_{th,p}|\right) V_{sd} - \frac{1}{2} V_{sd}^2\right). \quad (15)$$

In the saturation region ($V_{ds} \geq V_{gs} - V_{th,n}$ for NMOS or $V_{sd} \geq V_{sg} - |V_{th,p}|$ for PMOS), the current depends quadratically on the overdrive voltage, with the NMOS current given by

$$i_d = \frac{1}{2}\left(\frac{W_n}{L_n}\right) K_n \left(V_{gs} - V_{th,n}\right)^2 \left(1 + \lambda_n V_{ds}\right), \quad (16)$$

and PMOS as

$$i_{sd} = \frac{1}{2}\left(\frac{W_p}{L_p}\right) K_p \left(V_{sg} - |V_{th,p}|\right)^2 \left(1 + \lambda_p V_{sd}\right). \quad (17)$$

In the modified cross-coupled differential drive (CCDD) rectifier circuit, the body-source voltage for the PMOS transistor is simplified as follows:

$$V_{bs\_PMOS} = V_{\text{out}}, \quad (18)$$

This indicates that the body is connected to the output voltage to prevent the forward biasing of the body-source junction, which could lead to unwanted current flow. The adaptive body bias threshold voltages for the transistors are modulated by the RF signal $V_{\text{RF}}(i)$. For PMOS transistors, the threshold voltages V_{th_P2} and V_{th_P3} are adjusted as follows:

$$V_{th\_P2} = V_{th\_P}(V_{bs\_PMOS}) + \gamma_p \left(\sqrt{2\phi_F + V_{\text{RF}}(i)} - \sqrt{2\phi_F}\right), \quad (19)$$

$$V_{th\_P3} = V_{th\_P}(V_{bs\_PMOS}) + \gamma_p \left(\sqrt{2\phi_F - V_{\text{RF}}(i)} - \sqrt{2\phi_F}\right). \quad (20)$$

Similarly, for the NMOS transistors, the threshold voltages V_{th_N2} and V_{th_N3} are expressed as

$$V_{th\_N2} = V_{th\_N}(V_{bs\_NMOS}) + \gamma_n \left(\sqrt{2\phi_F - V_{\text{RF}}(i)} - \sqrt{2\phi_F}\right), \quad (21)$$

$$V_{th\_N3} = V_{th\_N}(V_{bs\_NMOS}) + \gamma_n \left(\sqrt{2\phi_F + V_{\text{RF}}(i)} - \sqrt{2\phi_F}\right). \quad (22)$$

These expressions account for the body effect, where the threshold voltage is influenced by the body-source voltage and RF signal through their respective body effect coefficients γ_p and γ_n for PMOS and NMOS, as well as the surface potential ϕ_F. The gate-source voltages for the transistors were determined based on these adaptive threshold voltages and the required drain currents. For PMOS transistors, the gate-source voltages are as follows:

$$V_{GS\_P0} = V_{th\_P2} + \sqrt{\frac{2 \cdot I_{D\_P2}}{k'_P \cdot \left(\frac{W_{P2}}{L_{P2}}\right)}}, \quad (23)$$

$$V_{GS\_P1} = V_{th\_P3} + \sqrt{\frac{2 \cdot I_{D\_P3}}{k'_P \cdot \left(\frac{W_{P3}}{L_{P3}}\right)}}. \quad (24)$$

For the NMOS transistors,

$$V_{GS\_N0} = V_{th\_N2} + \sqrt{\frac{2 \cdot I_{D\_N2}}{k'_N \cdot \left(\frac{W_{N2}}{L_{N2}}\right)}}, \quad (25)$$

$$V_{GS\_N1} = V_{th\_N3} + \sqrt{\frac{2 \cdot I_{D\_N3}}{k'_N \cdot \left(\frac{W_{N3}}{L_{N3}}\right)}}. \quad (26)$$

These Equations ensure that the transistors operate at the desired current levels by adjusting the gate-source voltages according to the adaptive threshold voltages and device parameters, facilitating the accurate modeling and optimization of the performance of the CCDD rectifier for applications such as RF energy harvesting.

The gate-source voltages V_{GS_P0}, V_{GS_P1}, V_{GS_N0}, and V_{GS_N1}, influenced by parasitic effects, are adjusted by subtracting a term that accounts for the voltage drop due to parasitic resistance $R_{\text{parasitic}}$ and capacitance $C_{\text{parasitic}}$, as described in Equations. (27), (28), (29), and (30). This adjustment, derived from the product of the respective drain currents ($I_{D\_P2}, I_{D\_P3}, I_{D\_N2}, I_{D\_N3}$) and parasitic resistance, divided by $1 + I_D \cdot C_{\text{parasitic}}$, captures the impact of parasitic elements on the transistor behavior in practical circuits.

$$V_{GS\_P0} = V_{GS\_P0} - \frac{I_{D\_P2} \cdot R_{\text{parasitic}}}{1 + I_{D\_P2} \cdot C_{\text{parasitic}}} \quad (27)$$

$$V_{GS\_P1} = V_{GS\_P1} - \frac{I_{D\_P3} \cdot R_{\text{parasitic}}}{1 + I_{D\_P3} \cdot C_{\text{parasitic}}} \quad (28)$$

$$V_{GS\_N0} = V_{GS\_N0} - \frac{I_{D\_N2} \cdot R_{\text{parasitic}}}{1 + I_{D\_N2} \cdot C_{\text{parasitic}}} \quad (29)$$

$$V_{GS\_N1} = V_{GS\_N1} - \frac{I_{D\_N3} \cdot R_{\text{parasitic}}}{1 + I_{D\_N3} \cdot C_{\text{parasitic}}} \quad (30)$$

For the PMOS transistor drain current I_{D_P0}, the behavior between the operating regions is modeled as follows: In the subthreshold region, Equation (31) expresses I_{D_P0} as an exponential function of $V_{GS\_P0} - V_{th,p}$, modulated by the drain-source voltage $V_{\text{out}}(t) - V_{\text{RF}}(t)$ and subthreshold conduction factor $\lambda_{\text{sub,p}}$. In the triode region, Equation (32) describes a linear dependence on $V_{GS\_P0} - |V_{th,p}|$, which is influenced by the drain-source voltage and its square. In the saturation region, Equation (33) models I_{D_P0} as a quadratic function of $V_{GS\_P0} - |V_{th,p}|$, with a modulation term of the channel length.

$$I_{D\_P0} = I_0 \exp\left(\frac{V_{GS\_P0} - V_{th,p}}{nV_t}\right) \times \left(1 - \exp\left(-\frac{V_{\text{out}}(t) - V_{\text{RF}}(t)}{V_t}\right)\right) \times \left(1 + \lambda_{\text{sub,p}}(V_{\text{out}}(t) - V_{\text{RF}}(t))\right) \tag{31}$$

$$I_{D\_P0} = \left(\frac{W_{P0}}{L_{P0}}\right) K_p \left((V_{GS\_P0} - |V_{th,p}|) \times (V_{\text{out}}(t) - V_{\text{RF}}(t)) - \frac{1}{2}(V_{\text{out}}(t) - V_{\text{RF}}(t))^2\right) \tag{32}$$

$$I_{D\_P0} = \frac{1}{2}\left(\frac{W_{P0}}{L_{P0}}\right) K_p \left(V_{GS\_P0} - |V_{th,p}|\right)^2 \times \left(1 + \lambda_p(V_{\text{out}}(t) - V_{\text{RF}}(t))\right) \tag{33}$$

Similarly, the drain current I_{D_P1} for another PMOS transistor is characterized across the operating regions. Equation (34) models the subthreshold region with an exponential dependence on $V_{GS\_P1} - V_{th,n}$, incorporating the drain-source voltage and the subthreshold slope factor. In the triode region, Equation (35) describes a linear relationship, whereas Equation (36) captures the quadratic behavior in saturation, including channel length modulation

$$I_{D\_P1} = I_0 \exp\left(\frac{V_{GS\_P1} - V_{th,n}}{nV_t}\right) \times \left(1 - \exp\left(-\frac{V_{\text{out}}(t) - V_{\text{RF}}(t)}{V_t}\right)\right) \times \left(1 + \lambda_{\text{sub,n}}(V_{\text{out}}(t) - V_{\text{RF}}(t))\right) \tag{34}$$

$$I_{D\_P1} = \left(\frac{W_{P1}}{L_{P1}}\right) K_p \left((V_{GS\_P1} - |V_{th,n}|) \times (V_{\text{out}}(t) - V_{\text{RF}}(t)) - \frac{1}{2}(V_{\text{out}}(t) - V_{\text{RF}}(t))^2\right) \tag{35}$$

$$I_{D\_P1} = \frac{1}{2}\left(\frac{W_{P1}}{L_{P1}}\right) K_p \left(V_{GS\_P1} - |V_{th,n}|\right)^2 \times (1 + \lambda(V_{\text{out}}(t) - V_{\text{RF}}(t))) \tag{36}$$

For the NMOS transistor drain current I_{D_N0}, Equation (37) models the subthreshold region with an exponential function of $(V_{GS\_N0} - V_{\text{RF}}(t)) - V_{th,n}$, which is adjusted for the negative drain-source voltage $-V_{\text{RF}}(t)$. In the triode region, Equation (38) describes a linear dependence, and in the saturation region, Equation (39) captures the quadratic behavior with modulation of the channel length.

$$I_{D\_N0} = I_{0,n} \exp\left(\frac{(V_{GS\_N0} - V_{\text{RF}}(t)) - V_{th,n}}{nV_t}\right) \times \left(1 - \exp\left(-\frac{-V_{\text{RF}}(t)}{V_t}\right)\right) \tag{37}$$

$$I_{D\_N0} = \left(\frac{W_{N0}}{L_{N0}}\right) K_n \left(((V_{GS\_N0} - V_{\text{RF}}(t)) - V_{th,n}) \times (-V_{\text{RF}}(t)) - \frac{1}{2}(-V_{\text{RF}}(t))^2\right) \tag{38}$$

$$I_{D\_N0} = \frac{1}{2}\left(\frac{W_{N0}}{L_{N0}}\right) K_n \left((V_{GS\_N0} - V_{\text{RF}}(t)) - V_{th,n}\right)^2 \times (1 + \lambda(-V_{\text{RF}}(t))) \tag{39}$$

Likewise, the NMOS drain current I_{D_N1} is modeled by Equation (40) in the subthreshold region, Equation (41) in the triode region, and Equation (42) in the saturation region, following similar dependencies as I_{D_N0}.

$$I_{D\_N1} = I_{0,n} \exp\left(\frac{(V_{GS\_N1} - V_{\text{RF}}(t)) - V_{th,n}}{nV_t}\right) \times \left(1 - \exp\left(-\frac{-V_{\text{RF}}(t)}{V_t}\right)\right) \tag{40}$$

$$I_{D\_N1} = \left(\frac{W_{N1}}{L_{N1}}\right) K_n \left(((V_{GS\_N1} - V_{\text{RF}}(t)) - V_{th,n}) \times (-V_{\text{RF}}(t)) - \frac{1}{2}(-V_{\text{RF}}(t))^2\right) \tag{41}$$

$$I_{D\_N1} = \frac{1}{2}\left(\frac{W_{N1}}{L_{N1}}\right) K_n \left((V_{GS\_N1} - V_{\text{RF}}(t)) - V_{th,n}\right)^2 \times (1 + \lambda_n(-V_{\text{RF}}(t))) \tag{42}$$

The output current $I_{\text{out}}(t)$, defined in Equation (43), depends on the input voltage $V_{\text{RF}}(t)$ and is expressed as For $V_{\text{RF}}(t) \geq 0$, it is the sum of $I_{D\_P0}(t)$ and $I_{D\_N1}(t)$, and for $V_{\text{RF}}(t) < 0$, it is the sum of $I_{D\_P1}(t)$ and $I_{D\_N0}(t)$. The output voltage across the capacitor, $V_{\text{out\_cap}}$, is obtained by integrating $I_{\text{out}}(t)$ over time and dividing it by the output capacitance C_{out}, as shown in Equation (44). The time constant $\tau = R \cdot C_{\text{out}}$, given in Equation (45), governs the charging and discharging dynamics of output capacitor. The output voltage $V_{\text{out}}(t)$, described in Equation (46), evolves based on the previous voltage and the charging behavior dictated by τ.

$$I_{\text{out}}(t) = \begin{cases} I_{D\_P0}(t) + I_{D\_N1}(t) & \text{if } V_{\text{RF}}(t) \geq 0 \\ I_{D\_P1}(t) + I_{D\_N0}(t) & \text{if } V_{\text{RF}}(t) < 0 \end{cases} \tag{43}$$

$$V_{\text{out\_cap}} = \frac{1}{C_{\text{out}}} \int_0^t I_{\text{out}}\, dt \tag{44}$$

$$\tau = R \cdot C_{\text{out}} \tag{45}$$

$$V_{\text{out}}(t) = V_{\text{out\_cap}}(t-1) + \left(V_{\text{out\_cap}}(t) - V_{\text{out\_cap}}(t-1)\right) \times \left(1 - e^{-dt/\tau}\right) \tag{46}$$

The output power P_{out}, calculated as the product of V_{out} and I_{out} in Eq. (47), represents the power delivered by the circuit.

The PCE, defined in Equation (48), is the ratio of P_{out} to the input power P_{in}, expressed as a percentage, and it provides a measure of the circuit's efficiency in converting input power to output power.

$$P_{\text{out}} = V_{\text{out}} \cdot I_{\text{out}} \tag{47}$$

$$PCE = \frac{P_{\text{out}}}{P_{\text{in}}} \cdot 100\,\% \tag{48}$$

Figure 5 presents a comparison of the DC analysis results for MOSFET devices simulated using Cadence Virtuoso and MATLAB. The plot illustrates the drain current (I_D) as a function of the gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) for MOSFETs modeled with GPDK 45 nm technology. The MATLAB simulations, which incorporate a cost function derived from our mathematical model, demonstrate close agreement with the Cadence results, thus validating the accuracy and reliability of the MATLAB-based cost function for predicting MOSFET behaviour. This alignment supports the use of MATLAB simulations to optimize the aspect ratios of devices in the modified cross-coupled differential drive rectifier, particularly when bio-inspired optimization algorithms are leveraged to enhance circuit performance. Based on this validation, the performance of the circuit is further evaluated using a comprehensive set of equations that address the behavior of the transistors across different operational regions.

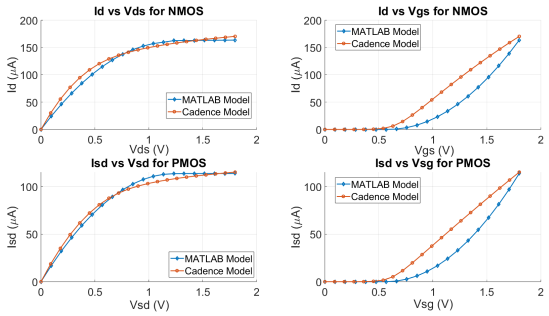

FIGURE 5. DC Analysis of circuit in figure 4 in cadence vs MATLAB.

For PMOS transistors P0 and P1, the subthreshold drain currents I_{D_P0} and I_{D_P1} are described by Equations 31 and 34, respectively, which incorporate the body effect and parasitic elements: In the triode region, the currents are modeled by 32 and 35, accounting for the interaction between V_{GS} and V_{DS}, while the saturation region currents are given by 33 and 36. Similarly, for N0 and N1 NMOS transistors, the subthreshold, triode, and saturation regions are represented by Equations 37, 38, 39 for N0 and 40, 41, 42 for N1, respectively. The overall performance of the circuit is characterized by the output current I_{out}, calculated using Eq. 43, and the output voltage $V_{\text{out\_cap}}$, determined by 44. The dynamics of capacitor charging and discharge are modeled by Equations 45 and 46, respectively. Furthermore, the output power P_{out} and PCE are derived from 47 and 48, respectively. This integrated mathematical framework provides a comprehensive approach for evaluating and optimizing circuit performance by combining detailed theoretical modeling with practical design considerations.

The mathematical model developed for the modified CCDD rectifier circuit provides a comprehensive and robust framework for analyzing and optimizing its performance in RFEH systems. This model meticulously captures the behavior of the transistor in the subthreshold, triode, and saturation regions through Equations such as (31), (32), and (33) for PMOS and (37), (38), and (39) for NMOS transistors, incorporating critical effects such as body biasing, parasitic elements, and adaptive thresholds. The inclusion of MOSFET-modeled capacitors, which are accounted for through the depletion layer capacitance in (4), suggests a novel approach to improve circuit efficiency. The precision of the model was validated by its close alignment with the Cadence Virtuoso simulations, as demonstrated in Figure 5, confirming its reliability in predicting the behavior of MOSFETs in the GPDK 45 nm technology. By integrating this model with MATLAB simulations, bio-inspired optimization algorithms can be used to optimize the aspect ratios of transistors, thus improving the performance of the rectifier for low-power applications. The derivation of key performance metrics, including output power P_{out} (47) and PCE (48), allows for a thorough evaluation of the effectiveness of the circuit. This integrated approach, which combines detailed theoretical modeling with practical simulation and optimization techniques, advances the understanding of RFEH circuits and facilitates the design of more efficient energy harvesting solutions for applications such as WSN and IoT devices.

III. RECTIFIER OPTIMIZATION

The WaOA, introduced in [37] is a population-based metaheuristic optimization algorithm inspired by the social behaviors of walruses, designed to address complex optimization problems such as the novel modified CCDD circuit. In WaOA, each walrus represents a candidate solution, with its position in the search space corresponding to the values of the decision variables. The population is randomly initialized as a matrix X, where each row X_i denotes a walrus, and each column represents a decision variable, as defined in Equation 49.

$$X = \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_N \end{bmatrix} = \begin{bmatrix} x_{1,1} & x_{1,2} & \cdots & x_{1,m} \\ x_{2,1} & x_{2,2} & \cdots & x_{2,m} \\ \vdots & \vdots & \ddots & \vdots \\ x_{N,1} & x_{N,2} & \cdots & x_{N,m} \end{bmatrix} \tag{49}$$

Here, X_i is the i-th walrus, x_{ij} is the j-th decision variable of the i-th walrus, N is the number of walruses, and m is the number of decision variables. The quality of each solution is evaluated using an objective function, producing a vector F

of the values of the objective function (Equation 50):

$$F = \begin{bmatrix} F_1 \\ F_2 \\ \vdots \\ F_N \end{bmatrix} = \begin{bmatrix} F(X_1) \\ F(X_2) \\ \vdots \\ F(X_N) \end{bmatrix} \tag{50}$$

The walrus that yields the best objective function value is designated as the strongest, guiding the population search.

The WaOA operates through three bio-inspired phases that balance exploration and exploitation, as outlined in Algorithm 1. In the first phase, the feeding strategy, global exploration is improved by simulating walrus foraging under the guidance of the strongest walrus. A new position for the i-th walrus is generated using Equation 51.

$$X_{ij}^{P1} = x_{ij} + rand_{ij} \cdot (SW_j - I_{ij} \cdot x_{ij}) \tag{51}$$

where X_{ij}^{P1} is the new position, SW_j is the position of the strongest walrus, $rand_{ij}$ is a random number, and I_{ij} is a random integer (1 or 2). If the new position improves the objective function, it replaces the current position (Equation 52).

$$X_i = \begin{cases} X_{ij}^{P1}, & F_{ij}^{P1} < F_i \\ X_i, & \text{else} \end{cases} \tag{52}$$

The second phase, migration, promotes exploration by modeling walruses moving to new regions of the ocean. Each walrus randomly selects another walrus and adjusts its position using Equation 53.

$$X_{ij}^{P2} = \begin{cases} x_{ij} + rand_{ij} \cdot (x_{kj} - I_{ij} \cdot x_{ij}), & F_k < F_i \\ x_{ij} + rand_{ij} \cdot (x_{ij} - x_{kj}), & \text{else} \end{cases} \tag{53}$$

where x_{kj} is the position of the randomly selected walrus, and F_k is its objective function value. The position is updated if the new objective function value is better (Equation 54).

$$X_i = \begin{cases} X_{ij}^{P2}, & F_{ij}^{P2} < F_i \\ X_i, & \text{else} \end{cases} \tag{54}$$

The third phase, escaping and fighting against predators, focuses on local exploitation by simulating positional adjustments within a walrus's neighborhood. The new position is calculated using Equation 55.

$$X_{ij}^{P3} = x_{ij} + \left(l_{b_{localj}} + \left(u_{b_{localj}} - rand \cdot l_{b_{localj}}\right)\right) \tag{55}$$

with local bounds defined in Equation 56.

$$\begin{aligned} l_{b_{localj}} &= \frac{l_{bj}}{t} \\ u_{b_{localj}} &= \frac{u_{bj}}{t} \end{aligned} \tag{56}$$

where l_{bj} and u_{bj} are the global lower and upper bounds, respectively, and t is the current iteration. The position is updated if the new position improves the objective function (Equation 57).

$$X_i = \begin{cases} X_{ij}^{P3}, & F_{ij}^{P3} < F_i \\ X_i, & \text{else} \end{cases} \tag{57}$$

These phases are iterated for a specified number of iterations T, with the best solution updated at each step. The algorithm ends when T is reached, outputting the best solution. The pseudocode is provided in Algorithm 1.

In this work, the WaOA is explicitly applied to the transistor-level design of the modified CCDD rectifier. The decision variables are the channel widths and lengths (W, L) of all eight core transistors, namely NMOS devices N0–N3 and PMOS devices P0–P3. Each walrus represents one candidate solution containing a complete set of these device dimensions. For every candidate solution, the rectifier performance is evaluated by computing the PCE using the developed mathematical model, which is validated against Cadence Virtuoso simulations. The objective function is defined as the average PCE over an input power range of −40 dBm to 0 dBm at the operating frequency. Technology constraints are enforced during optimization, including the minimum channel length of the 45 nm CMOS process and practical upper bounds on device width. During each iteration, WaOA updates the transistor dimensions to improve the objective function while maintaining circuit stability. The final output of the algorithm is the optimized set of (W, L) values that maximizes PCE across the specified input power range.

The WaOA was selected for transistor sizing in this work. As demonstrated in [37], WaOA exhibits superior exploration-exploitation balance compared to Particle Swarm Optimization (PSO) and nine other metaheuristic algorithms across 68 benchmark functions and 22 real-world engineering problems. The feeding and migration phases enable effective global search of the high-dimensional transistor sizing space, while the local exploitation phase prevents premature convergence. This makes WaOA particularly suitable for the rectifier optimization problem, which contains multiple local optima. We refer readers to [37] for detailed statistical comparison and convergence analysis.

For the optimization of the proposed modified CCDD rectifier, WaOA adjusts the transistor channel widths and lengths to directly maximize the power conversion efficiency. By combining global exploration through feeding and migration phases with local exploitation through predator-avoidance behavior, the algorithm efficiently searches the high-dimensional transistor sizing space and iteratively converges toward an optimal rectifier configuration [37].

IV. RESULTS AND DISCUSSION

A comprehensive analysis of the proposed modified rectifier circuit was conducted to thoroughly investigate its performance in RF energy-harvesting applications. The results, illustrated through various graphs, provide information on key parameters, such as the output voltage, conversion efficiency, and output power. Additionally, the impact of input and output capacitances on circuit performance was examined, along with the effect of transistor aspect ratio variations, which influence the width-to-length ratio of MOSFETs and, thus, the electrical characteristics of the

Algorithm 1 WaOA Applied to Transistor Sizing of the Modified CCDD Rectifier

Provide all details of the optimization problem.
Define the population size of walruses (N) and the maximum number of iterations (T).
Initialize the positions of the walruses in the search space.
for $t = 1$ to T **do**
  Identify the walrus with the best objective function value so far.
  for $i = 1$ to N **do**
    Phase 1: Exploration through feeding behavior
    Compute a potential new position using the formula in Eq. 51.
    Update the position of the ith walrus according to Eq. 52.
    Phase 2: Migration behavior
    Select a migration target for the ith walrus.
    Compute a new potential position using the formula in Eq. 53.
    Update the ith walrus's position according to Eq. 54.
    Phase 3: Exploitation through escaping and fighting predators
    Generate a new position near the current location of the ith walrus using the Equations 55 and 56.
    Update the ith walrus's position based on Eq. 57.
  end for
  Update the best solution found so far.
end for
Return the optimal or near-optimal solution discovered by the WaOA for the specified problem.

circuit. All simulations were performed using the Cadence Virtuoso Analog Design Environment to ensure the accuracy and reliability of the data.

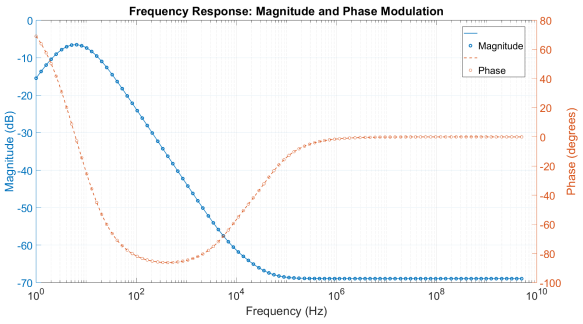

FIGURE 6. Frequency response of the modified rectifier.

Figure 6 presents the frequency response analysis of the modified rectifier circuit, illustrating both the magnitude and phase responses of the circuit. This analysis is essential for understanding the behavior of the circuit across different frequency ranges. The plot reveals that at lower frequencies, the circuit exhibits a significant AC component, indicating its responsiveness to these frequencies. However, as the frequency exceeded 100 kHz, the phase response stabilized at 0 °, and the magnitude response showed negligible AC components. This indicates that the circuit effectively filtered out the AC components at higher frequencies, stabilizing its performance in the desired range. These characteristics are particularly advantageous for RF energy-harvesting applications, where operation at high frequencies is crucial. The frequency response analysis confirmed that the modified rectifier was well-suited for the high-frequency ranges typical of RF energy harvesting, demonstrating stability and efficiency under these conditions.

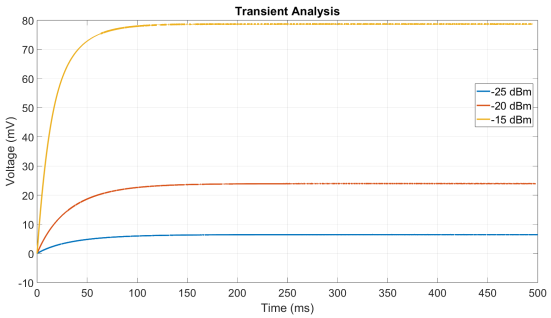

FIGURE 7. Transient analysis at input power −15, −20, and −25 dBm.

Figure 8 presents the simulated transient voltages of the RF input, MOSFET gate node, and rectified output. The gate voltage follows the RF excitation and shows periodic modulation resulting from the voltage-dependent capacitance of the MOS device. The inset highlights steady-state switching behaviour over a selected interval. The waveform demonstrates stable oscillation amplitude without ringing or divergence during the simulated time window. This indicates that nonlinear capacitance effects are present but remain bounded under the evaluated operating conditions. The rectified output increases smoothly and monotonically, and no instability is observed that would influence the efficiency estimation derived from simulated currents and voltages. These observations suggest that gate capacitance nonlinearity does not introduce observable fluctuation in circuit operation within the simulated range. The results are obtained from post-layout circuit simulation and therefore depend on the accuracy of the device models and extracted parasitic elements used in the analysis.

For a fair and consistent comparison in the steady-state performance results shown in Figures 9, 11, and 12, all three rectifier structures (conventional, dual, and modified) are evaluated under identical electrical conditions. All simulations use the same CMOS technology (GPDK 45 nm), the same RF input frequency, and a continuous-wave RF source with a fixed source impedance of 50 Ω. The input power is swept from −40 dBm to 0 dBm for all cases. The input

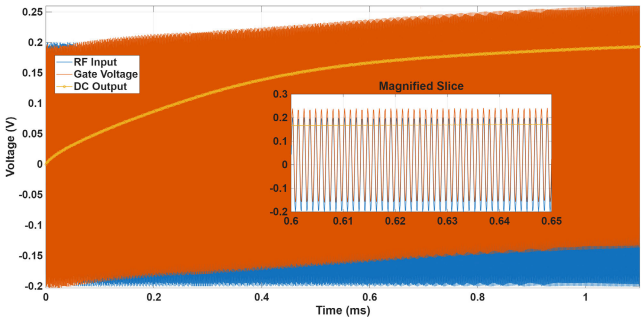

FIGURE 8. Transient voltages of RF input, MOSFET gate node, and rectified DC output. The inset shows a steady-state interval highlighting periodic gate modulation due to voltage-dependent MOS capacitance. The waveform confirms stable switching behaviour and consistent output charging under simulated conditions.

matching conditions, input capacitance, and output storage capacitance C_{out} are kept identical across all three designs. The output node definition and measurement methodology are also the same. The only differences among the three structures are the rectifier topology and the transistor aspect ratios (W/L). The conventional rectifier uses empirically selected device sizes, the dual rectifier follows reported sizing from prior work, and the proposed rectifier employs WaOA-optimized transistor dimensions. These controlled conditions establish a common electrical basis for the comparative results shown in Figure 9,11, and 12.

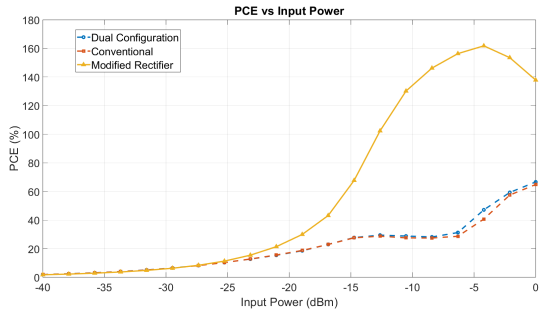

FIGURE 9. PCE is analysed for various input powers.

Figure 9 illustrates the PCE of different circuit configurations (modified, dual, and conventional) as a function of the input power, ranging from −40 to 0 dBm. The modified configuration consistently achieved higher PCE values, demonstrating its superior efficiency in converting the RF input power to the DC output power compared with the dual and conventional configurations.

It should be noted that the PCE values exceeding 100% are apparent (calculated) values and do not represent physical power gain [38]. In this work, PCE is defined as the ratio of the DC output power to the available RF input power. Due to the nonlinear and time-varying operation of the cross-coupled rectifier, energy is accumulated on the output capacitor C_{out} over multiple RF cycles through charge pumping. When the DC output power is computed from the steady-state output voltage and load current, it can exceed the time-averaged available RF input power at the source, resulting in calculated PCE values above 100%. This behavior reflects the adopted power definition and energy storage effect and does not violate the law of energy conservation. In addition to threshold reduction, the transistor aspect ratios are optimized using the WaOA to minimize ON-resistance during conduction while suppressing reverse leakage in the off state. Reduced ON-resistance lowers conduction losses at moderate and high input power, whereas reduced leakage limits power loss at low input power. This combined optimization maintains high PCE across the entire input power range. The simultaneous reduction of switching loss and leakage directly explains the higher PCE and the wider dynamic range observed in Figures 9 – 12.

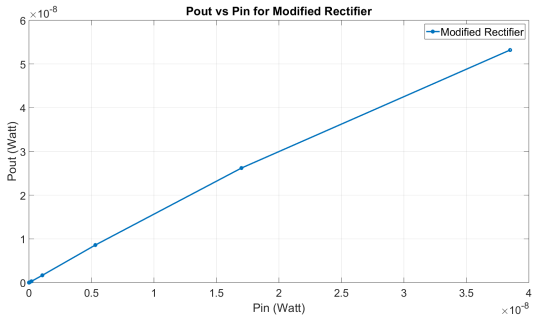

FIGURE 10. Comparison between the input and output powers.

Figure 10 presents the relationship between the input and output powers of the modified circuit, revealing a monotonic relationship that indicates stable power conversion behavior across the tested input power range, which is a critical feature for applications with varying input power levels.

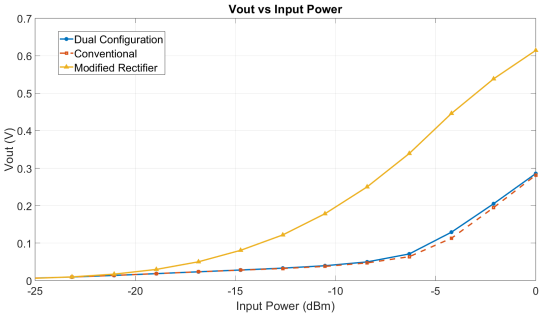

FIGURE 11. Output voltage is plotted against different input powers.

Figure 11 shows the steady-state DC output voltage as a function of input RF power for the modified, dual, and conventional rectifier configurations. Across the entire input power range, the modified rectifier produces a higher DC output voltage than the other two designs. This behavior indicates more effective rectification and charge accumulation at the output, primarily due to reduced effective switching threshold and improved forward conduction of the

cross-coupled devices in the proposed topology. The output voltage reported in Figure 11 is obtained under open-circuit DC conditions. The rectifier output is terminated only by the storage capacitor C_{out}, as shown in Figure 4, and no external resistive load is connected. A continuous-wave RF input signal with a fixed source impedance of 50 Ω is applied, and the circuit is simulated until steady state is reached. The plotted voltage corresponds to the steady-state DC voltage accumulated across C_{out} due to nonlinear charge pumping over multiple RF cycles. Therefore, Figure 11 represents the unloaded rectified output voltage and does not correspond to power delivery conditions.

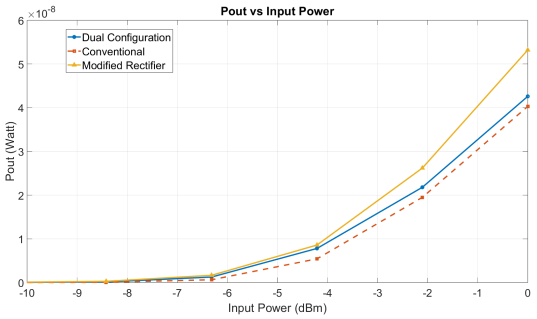

FIGURE 12. Output power is observed for different input powers.

The output power shown in Figure 12 is calculated under steady-state operating conditions. A continuous-wave RF input signal with a fixed source impedance of 50 Ω is applied. The DC output is connected to a constant resistive load. For each input power level, the circuit is simulated until steady state is reached. The output power is then computed as $P_{\text{out}} = V_{\text{out}} \times I_{\text{out}}$, using the steady-state DC output voltage and the corresponding load current. This output power curve represents the absolute DC power delivered to the load. In contrast, the PCE curve represents a normalized metric defined as the ratio of output power to available RF input power. Therefore, Figure 12 quantifies how much DC power is harvested, whereas the PCE plot indicates how efficiently the rectifier converts RF power to DC.

This improvement is a direct result of reduced conduction loss and improved charge transfer efficiency in the proposed topology. For the parametric analysis shown in Figures 13–20, the PCE is evaluated by varying only one transistor parameter (either width or length) at a time, while all other electrical and simulation parameters are kept constant. The simulations use the GPDK 45 nm CMOS technology and a continuous-wave RF source with a fixed source impedance of 50 Ω. For each sweep, the input frequency and the input power level are fixed. The input capacitance and the output storage capacitance C_{out} are identical in all cases. During each sweep, the remaining transistors are fixed at their default dimensions ($L = 45$ nm and $W = 120$ nm). The PCE is recalculated at each iteration using the same definitions of P_{out} and P_{in} given in Equations (47) and (48). Therefore, any change in PCE is caused only by the variation of the selected transistor dimension.

Based on this parametric analysis of the modified CCDD rectifier shown in Figure 4, the sensitivity of output voltage and PCE to transistor sizing is evaluated for all eight devices (N0–N3 and P0–P3). The resulting trends, shown in Figures 13–20, demonstrate that transistor dimensions strongly affect rectifier performance through their impact on ON-resistance, threshold modulation, and leakage current. The optimal device dimensions are summarized in Table 1. These dimensions represent a trade-off between low ON-resistance during conduction and reduced leakage during the off state, enabling high PCE and stable operation over a wide input power range.

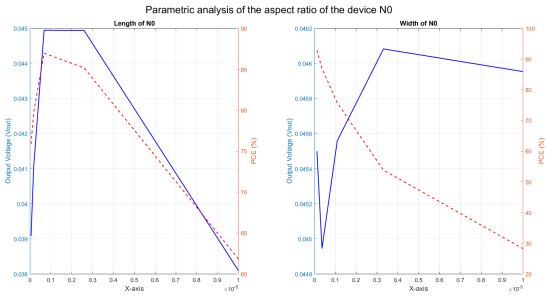

FIGURE 13. Parametric analysis of N0 aspect ratio.

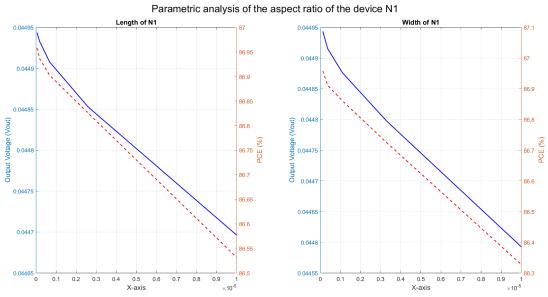

FIGURE 14. Parametric analysis of N1 aspect ratio.

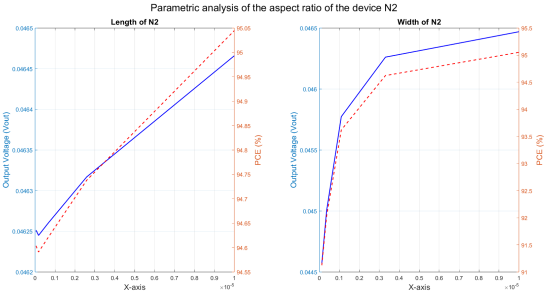

FIGURE 15. Parametric analysis of N2 aspect ratio.

Following the parametric analysis, the rectifier circuit was optimized by applying carefully selected aspect ratios,

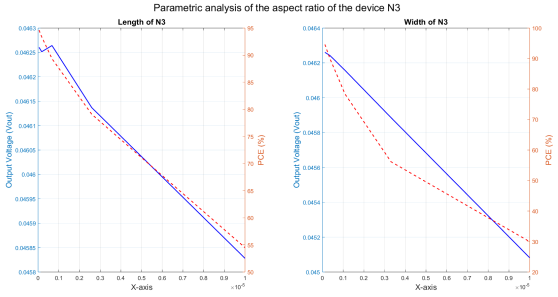

FIGURE 16. Parametric analysis of N3 aspect ratio.

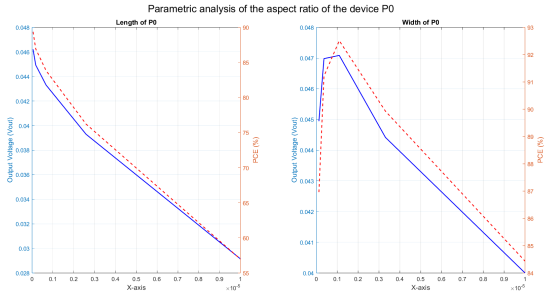

FIGURE 17. Parametric analysis of P0 aspect ratio.

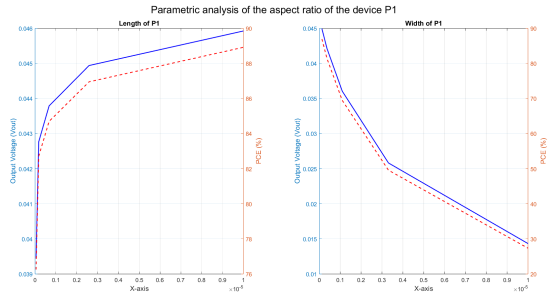

FIGURE 18. Parametric analysis of P1 aspect ratio.

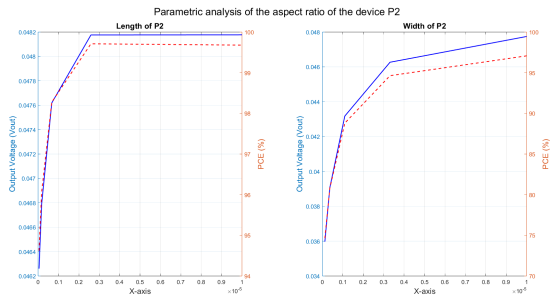

FIGURE 19. Parametric analysis of P2 aspect ratio.

as detailed in Table 1. These ratios were determined by fine-tuning the width and length of each device to maximize its performance. The optimized design was simulated, and its performance was evaluated through transient analysis. Figure 21 presents the output voltage from this analysis,

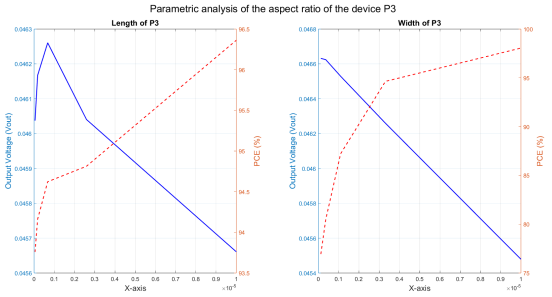

FIGURE 20. Parametric analysis of P3 aspect ratio.

TABLE 1. Optimized aspect ratios of devices in the circuit.

Devices	Length (m)	Width (m)	Aspect Ratio
N0	6.70E-07	1.20E-07	0.179104478
N1	4.50E-08	1.20E-07	2.666666667
N2	1.70E-07	1.00E-06	5.882352941
N3	4.50E-08	1.20E-07	2.666666667
P0	4.50E-08	1.00E-06	22.22222222
P1	2.60E-06	1.20E-07	0.046153846
P2	6.70E-07	3.30E-06	4.925373134
P3	6.70E-07	3.30E-06	4.925373134

revealing a marked improvement in stability and efficiency compared to the original circuit with the default device sizes. This enhanced performance is critical for the intended circuit applications, ensuring reliable operation under various conditions of use.

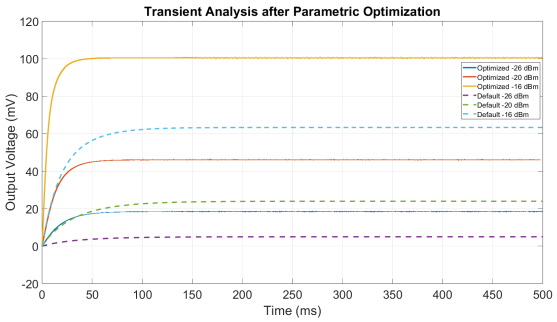

FIGURE 21. Transient analysis of circuit in figure 4 after optimization.

To evaluate the extent of the performance improvements, Figure 22 compares the PCE of the optimized and default circuit configurations over a range of input power levels. The optimized circuit exhibited a significant increase in PCE, particularly at lower input power levels, indicating its superior ability to convert power efficiently under challenging conditions. In addition, the optimized circuit demonstrated an extended dynamic range, enabling effective performance over a broader spectrum of input power levels. This enhanced flexibility makes the circuit more adaptable to varying operational conditions, thereby extending its applicability across diverse scenarios.

A comparative analysis of the PCE for different rectifier designs is presented in Table 2. The conventional design

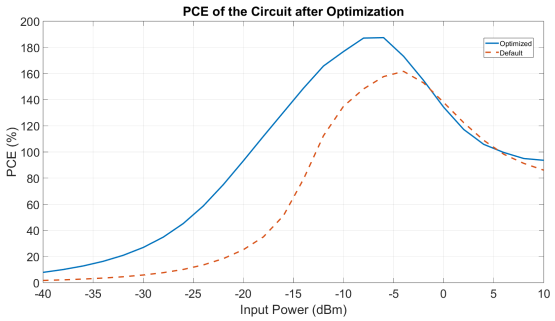

FIGURE 22. PCE vs Pin (dBm) after optimization using parametric analysis.

TABLE 2. Comparison of PCE for various rectifier designs.

Work	Input power (dBm)	PCE (%)
Conventional	-2	26.05
Dual	-2	89.41
Dual	-8	70.17
This Work	-22	85.12

achieved a PCE of 26.05% at an input power of -2 dBm, whereas the dual configuration reached 89.41% at −2 dBm but dropped to 70.17% at −8 dBm. In contrast, the proposed design operates at a significantly lower input power of -22 dBm but maintains a high PCE of 85.12%, highlighting its exceptional efficiency under low-power conditions.

The optimization of the device dimensions was further refined using the WaOA, as shown in Figures 23 and 24. These figures show the iterative adjustment of the width (W) and length (L) of the NMOS and PMOS devices over 100 iterations, ensuring optimal aspect ratios that maximize output performance while maintaining efficiency. This process is crucial for improving the performance of both NMOS and PMOS devices, which contributes to the overall effectiveness of the circuit design.

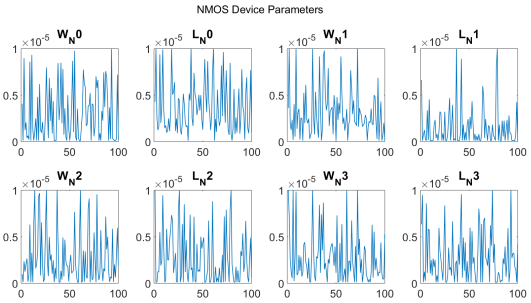

FIGURE 23. NMOS device aspect ratio.

Following WaOA optimization, an additional parametric analysis was performed to identify reduced transistor dimensions that preserve near-optimal PCE while minimizing device area. Figures 25 and 26 illustrate the parametric trends in the device width and length, demonstrating consistent performance across a range of sizes. This flexibility allows

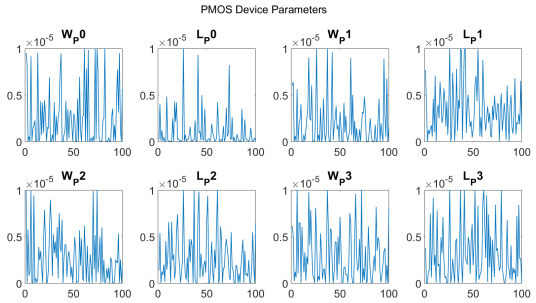

FIGURE 24. PMOS device aspect ratio.

for the minimization of the device size and optimization of the circuit for compactness and efficiency.

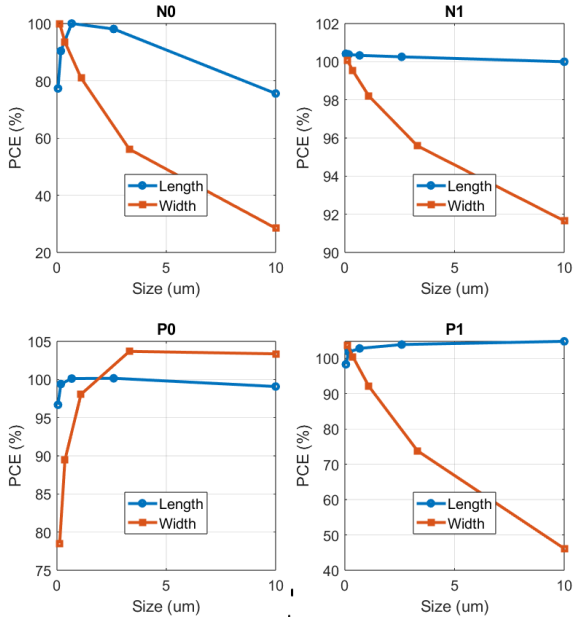

FIGURE 25. Parametric analysis after obtaining device sizes from WaOA (Part 1).

The device dimensions reported in Table 3 are not initial parameter values. For all transistors, the initial dimensions were set to the technology default values of $L = 45$ nm and $W = 120$ nm as defined by the GPDK 45 nm CMOS process. These default values were used only to initialize the WaOA-based optimization and the conventional parametric analysis. Table 3 lists the final optimized transistor dimensions obtained after convergence using three methods: (i) global optimization using WaOA, (ii) conventional parametric optimization, and (iii) post-WaOA parametric refinement. Each reported value corresponds to a converged solution that maximizes PCE under fixed electrical conditions and does not represent an initial design guess.

Table 3 compares the optimized transistor dimensions obtained through WaOA, conventional parametric analysis, and post-WaOA refinement, highlighting WaOA's ability to identify better-optimized transistor dimensions by exploring

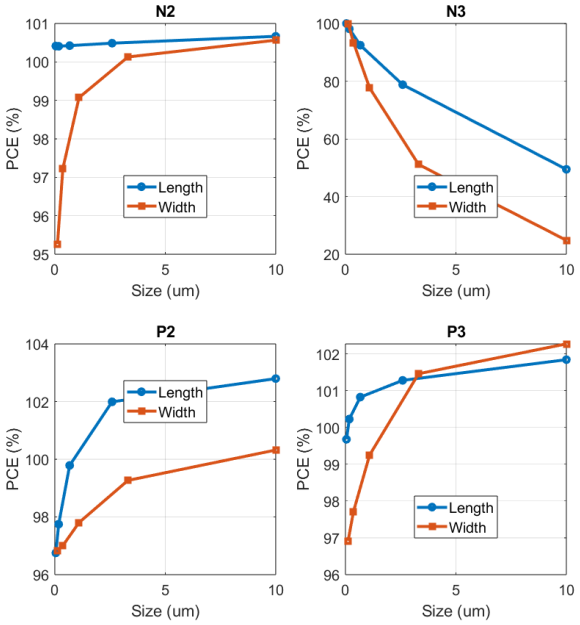

FIGURE 26. Parametric analysis after obtaining device sizes from WaOA (Part 2).

TABLE 3. Final optimized transistor dimensions obtained using WaOA-based optimization, conventional parametric analysis, and post-WaOA refinement. Initial device dimensions for all transistors were $L = 45$ nm and $W = 120$ nm (GPDK 45 nm defaults) and were used only as starting points for optimization.

Device	WaOA		Parametric		Post-WaOA	
	Length	Width	Length	Width	Length	Width
N0	4u	120n	670n	120n	670n	120n
N1	8u	120n	45n	120n	45n	120n
N2	45n	6u	170n	1u	45n	3.3u
N3	45n	120n	45n	120n	45n	120n
P0	570n	1.5u	1u	1u	670n	3.3u
P1	2u	120n	45n	120n	670n	120n
P2	9u	5u	670n	3.3u	670n	3.3u
P3	4u	1.1u	670n	3.3u	670n	3.3u

a wider design space. This results in better-optimized solutions that enhance the circuit performance more effectively than traditional methods. The combination of parametric analysis and WaOA significantly improved the rectifier circuit's performance, achieving a higher PCE, particularly at low input power levels, and extending its dynamic range. These enhancements make the optimized design highly suitable for a wide range of applications, demonstrating the effectiveness of the optimization strategy in achieving efficient and compact circuit design.

Figure 27 provides a graphical comparison of the aspect ratios of the devices obtained using the WaOA and a traditional parametric analysis. Complementing the data in Table 3, this graph illustrates that WaOA typically achieves more optimal device sizing while also demonstrating that comparable performance can be achieved with various size configurations.

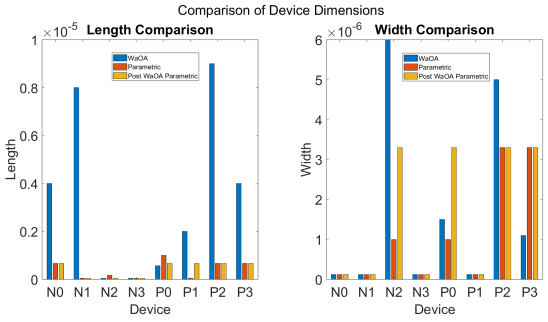

FIGURE 27. Graphical representation of the aspect ratio of devices obtained from parametric analysis.

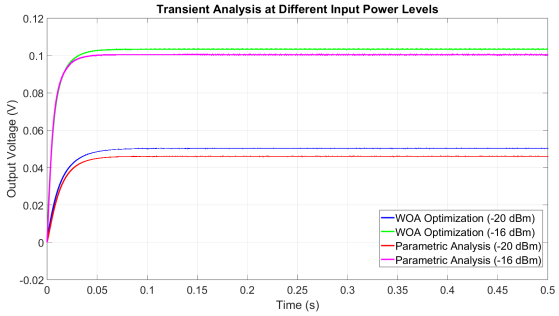

FIGURE 28. Transient analysis comparison between WaOA-optimized and parametrically optimized transistor aspect ratios.

Figure 28 compares the transient performance of circuits optimized with WaOA to those designed using parametric analysis. The waveform responses highlight the superior dynamic behavior of the WaOA-optimized circuits, underscoring the effectiveness of advanced optimization techniques for high-speed and efficient circuit applications.

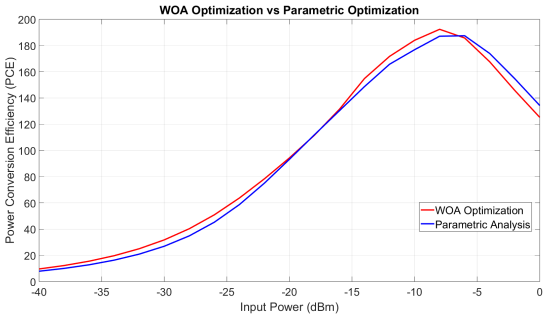

FIGURE 29. PCE comparison between WaOA-optimized and parametrically optimized transistor aspect ratios.

Figure 29 shows the PCE as a function of the input power for circuits optimized by WaOA and parametric methods. The consistent PCE across a range of input powers for the WaOA-optimized design indicates robust transistor sizing, showcasing the algorithm's ability to optimize multiple parameters simultaneously for enhanced efficiency.

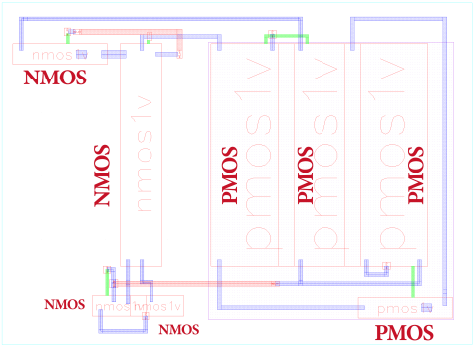

FIGURE 30. Top view of the physical layout of the modified circuit.

Figure 30 presents the top view of the physical layout of the circuit, which is essential to ensure that the optimized design is translated into a practical implementation that meets the manufacturing and performance constraints in the real world.

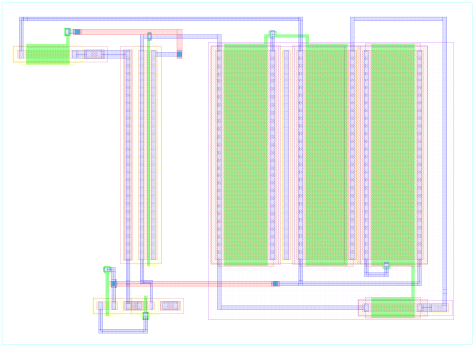

FIGURE 31. Layer view of the physical layout of the modified circuit.

Figure 31 illustrates the circuit layout layer view, detailing the arrangement of the components across multiple layers. This perspective is critical for verifying compliance with manufacturing standards and identifying potential parasitic effects that could affect circuit performance.

Figure 32 shows the extracted view of the layout, which incorporates real-world effects, such as parasitic capacitance and resistance. This view is vital for the final design validation, ensuring that the circuit is ready for fabrication by addressing potential performance issues.

Figure 33 shows the PCE of the circuit for input powers ranging from −40 to 0 dBm. This assessment validated the performance of the circuit under varying operating conditions, confirming the effectiveness of the optimized design.

It is important to clarify that this work is based on circuit design, layout, and post-layout simulation results only. The rectifier has not yet been fabricated, and therefore no physical prototype measurements are reported in this study. The physical layouts shown in Figures 30–32 correspond to a completed layout that has been verified using design

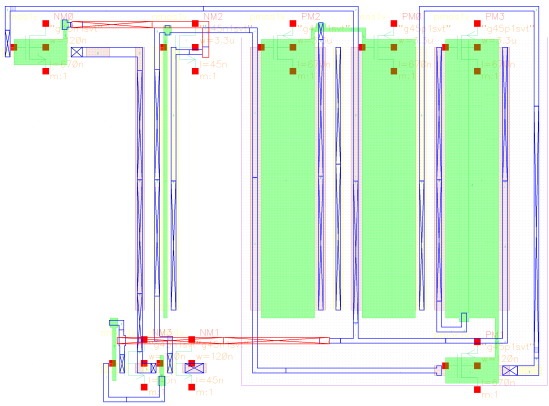

FIGURE 32. Extracted view of the physical layout of the modified circuit.

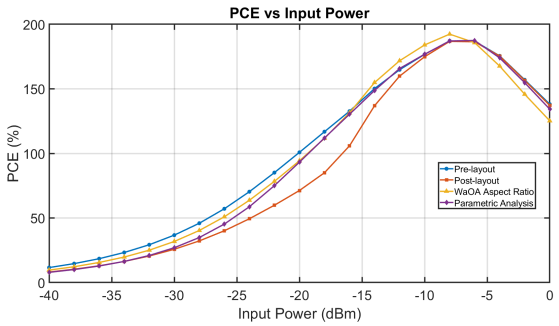

FIGURE 33. PCE comparison of the circuit at input powers from −40 to 0 dBm.

rule checking (DRC), layout-versus-schematic (LVS), and post-layout parasitic extraction (PEX). All performance results presented in this paper, including output voltage, output power, and PCE, are obtained from post-layout simulations that include extracted parasitic effects. Experimental fabrication and hardware measurements are planned as future work to validate the simulated results under real RF operating conditions.

All post-layout simulations were performed using Cadence Virtuoso Spectre with GPDK 45 nm CMOS technology. Simulation settings: RF input frequency = 900 MHz, source impedance = 50 Ω, output load capacitance Cout = 1 pF, no external resistive load connected for open-circuit output voltage measurement. Parasitic extraction was performed using Assura with RC reduction enabled. Simulation temperature = 27°C. Transient simulations were run for 500 ms to ensure steady-state convergence. PCE is calculated using Equation 48, where Pin is the maximum power deliverable from the source under conjugate matched condition. The reported PCE of 93.24% is the peak value obtained at Pin = −17.5 dBm under these simulation conditions.

Overall, the post-layout simulation results demonstrate that the proposed modified rectifier achieves improved output voltage, output power, and PCE over a wide input power range. The combined use of parametric analysis

TABLE 4. Comparison of the proposed rectifier with recent state-of-the-art designs.

Work	Technology	Stage	Freq (MHz)	Input Power (dBm)	Output Voltage (mV)	Max PCE (%)	Power Dynamic Range (dB)	Area (μm^2)	Type
[39], Electronics'24	180 nm	2	900	-11	N/A	69	17	N/A	Sim
[40], TCAS-II'24	130 nm	6	915	-9.6	800 @-28dBm	72.9	17.3	N/A	Meas
[41], Sensors'22	65 nm	1	900	-18.8	1000	73	17.3	9300	Sim
[42], TCAS-I'25	55 nm	3	915	-25	1000	31.3	14	27000	Meas
[14],IEEE Access'21	180 nm	5	953	-16.1	N/A	73.8	N/A	400	Sim
[43], VLSID'25	65 nm	1	953	-8.8	N/A	60	14	3619	Sim
[44], TCAS-I'22	130 nm	10	900	-16	2190	42.4	14	29000	Meas
[45],IEEE Access'25	180 nm	1	930	-18.9	1000	78.5	26.1	8058	Sim
This Work	45 nm	1	900	-17.5	40.7	93.24	25	35.22	Sim

and WaOA-based optimization enables effective transistor sizing, leading to reduced conduction loss and enhanced charge transfer efficiency. The verified layout and post-layout extracted simulations confirm the feasibility of the design. Experimental fabrication and hardware measurements are planned as future work to validate the simulated performance under real RF operating conditions.

V. SUMMARY AND CONCLUSION

In this study, we present a novel, modified CCDD rectifier for RFEH applications. By integrating MOSFET-modeled capacitors, the proposed design achieves a significant reduction in area consumption while maintaining a PCE. Through detailed mathematical modeling and simulation using the Cadence Virtuoso Analog Design Environment, we demonstrated that the modified rectifier outperforms both the conventional and dual configurations, particularly at low input power levels. The use of the WaOA further enhanced circuit performance by optimizing the aspect ratios of the transistors. Our results show that the modified rectifier achieves a maximum PCE of 93.24% at an input power of -17.5 dBm, with a notable improvement in efficiency even at ultralow input powers as low as -30 dBm. The proposed design achieves a wide power dynamic range of 25 dB and occupies an ultra-compact area of $35.22\mu m^2$, making it highly suitable for ambient RFEH applications. Furthermore, as shown in Table 4, our design compares favorably with recent state-of-the-art rectifiers, offering a higher PCE at comparable input power levels.

It is important to note that the works cited in Table 4 include both simulation-only studies and fabricated prototypes with measurement results. Our work currently reports post-layout simulation results only; fabrication and measurement are planned as future work. Simulation results typically show higher PCE compared to measurement due to idealized conditions, absence of process variation, and incomplete modeling of high-frequency parasitic effects. Therefore, the 93.24% PCE reported here should be interpreted as the simulated upper bound achievable with the proposed topology and optimization method. Experimental validation will provide realistic performance under actual fabrication and operating conditions.

The proposed design represents a significant advancement in RFEH technology, offering a more efficient and compact solution for powering low-energy devices such as IoT sensors and wearable electronics. Future work will focus on the experimental validation of the design and the exploration of its integration into multi-stage rectifiers to further enhance its performance and applicability.

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RUPAM BORA (Student Member, IEEE) received the B.E. degree in instrumentation engineering from Assam Engineering College, Guwahati, in 2020, and the M.Tech. degree in electronics and communication engineering from Gauhati University, Assam, India, in 2024, where he is currently pursuing the Ph.D. degree in electronics and communication engineering.

He completed the TEEP Internship with Chung Gung University, Taiwan, where he was with the CReST Laboratory, from July 2025 to October 2025. His research interests include RF energy harvesting, circuit design, 6G communication systems, and FPGA-based system design.

MANASH PRATIM SARMA (Member, IEEE) received the M.Sc. degree in electronics from Gauhati University and the M.Tech. degree in electronics design and technology from Tezpur University, Assam. He is currently an Assistant Professor with the Department of Electronics and Communication Engineering, Gauhati University, Assam, India. His research interests include VLSI, high speed VLSI design for communications, RF energy harvesting systems, and CMOS circuit design. He is a fellow of IETE.

LACHIT DUTTA (Senior Member, IEEE) received the Ph.D. degree in embedded systems and machine olfaction from Tezpur University, Tezpur, India, in 2019. He is currently an Assistant Professor with the Department of Electronics and Communication Engineering, Gauhati University, Guwahati, India. His research interests include sensor system design, biomedical signal processing, sensor fabrication, the IoT, renewable energy, and AI and its application in microcontroller.

PRANJAL BARMAN (Member, IEEE) received the M.Tech. and Ph.D. degrees from Tezpur University. He is currently an Assistant Professor with the Department of Electrical Engineering, Assam Skill University, specializing in electric vehicles and renewable energy. He has a strong background in teaching, hands-on prototyping, and the development of training modules in EVs and drone technology. His research interests include electric vehicle, traction control systems, power electronics, circuit and system design, and renewable energy.

BRIAN AZZOPARDI (Senior Member, IEEE) received the B.Eng. degree (Hons.) in electrical and electronics engineering from the University of Malta, in 2002, and the Ph.D. degree from The University of Manchester, U.K., in 2011. He is currently a Senior Lecturer II and the Founding Chair of Malta College of Arts, Science and Technology (MCAST) Energy Research Group, the Founding Chair of The Foundation for Innovation and Research-Malta (FiR.mt), and a Visiting Senior Lecturer with the University of Malta. Previously, he was an Associate Professor and a Senior Researcher with Kaunas University of Technology, Lithuania. He is the Coordinator of the H2020 and Horizon Europe Projects, JUMP2Excel.eu, NEEMO-Project.eu, PVPROMISE.eu, and TRANSITproject.eu. His research interests include clean energy technologies, renewable energy integration, sustainable power systems, and energy and environmental economics. He was the Chairperson of the Tertiary Education Scholarship Scheme (TESS), from 2017 to 2022, a Senior Member of the Chamber of Engineers, an Invited Member of the Royal Society of Chemistry, and the Chair of the ISOS-10 (2017) and MEDPOWER2022 conferences. Additionally, in 2008, he obtained the Certificate in Vocational Education from MCAST. In 2012, he earned the P.G.C.H.E. from Oxford Brookes University, U.K., specializing in higher education. In 2012., U.K. Engineering Council awarded him the C.Eng. and the EI Chartered Energy Engineer titles.