

# High Current Multi-Stage Gate Drive Unit to Control the Maximum $dv/dt$

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**Abstract**—This paper addresses the fast voltage changes in a hard-switching IGBT based two-level voltage-source inverter. It is well known that fast-switching devices generate high  $dv/dt$  values at the inverter output. This paper presents a solution to control the voltage slopes of IGBTs in a flexible manner. The proposed method utilizes a multi-stage architecture to control both the dynamic and static behavior of the IGBT. The control stage of the proposed method is simulated and verified in a test chamber. The measurement results underline the capability to control effectively the  $di/dt$  and  $dv/dt$  for IGBTs.

**Index Terms**—Igbt, gate drive unit,  $dv/dt$  control,  $di/dt$  control, variable gate voltage, switching transients

## I. INTRODUCTION

From July 1st 2021, efficiency class of IE2 is required by the Regulation (EU) 2019/1781 for drives up to 1000 kW, up to 1000 V, and up to 599 Hz. Active front end, low harmonic front end, single phase, and multi-drives are exempted. On the motor side, only induction motors are affected so far, but the regulation for drives covers all types of motors [1], [2].

The efficiency of the inverter could be increased by increasing the switching speed, thus lowering the switching losses, or bluntly by reducing the current densities and flux densities in various parts of the circuit. The first approach usually leads to more expensive semiconductors, while the other leads to increased weight and size, again increasing the cost. In addition, the impulse voltage insulation classes (IVIC) set forth in IEC 60034-18-41 practically eliminate the sole use of faster switching semiconductors [3].

The switching speeds have been steadily increasing from the advent of the IGBT in mid-80's to the present. Currently the introduction of wide band gap silicon carbide and gallium nitride semiconductors continue this trend. Short rise and fall

times of the currents and voltages during switching cause high frequency radiated electromagnetic emission, which must be kept below the allowed limits. The  $dv/dt$  itself stresses the first turns of the motor winding. Moreover, the voltage wave is reflected at the motor terminals depending on the cable length. The propagation speed of the wave is approximately 100 m/ $\mu$ s.

The reflection increases the peak voltage at the motor end from the initial peak voltage at the inverter source. The increase is due to the mismatch of the wave impedance of the cable (few tens of ohms) and the motor (a few hundred ohms). High  $dv/dt$  leads to the full reflection of the voltage even with relatively short motor cables (a few tens of meters). Reducing the  $dv/dt$  would be a straightforward way to reduce the insulation stress and emission levels. However, this will typically lead to higher switching losses in the power switches.

This paper considers a multi-stage gate drive unit to control the  $dv/dt$  of IGBTs to acceptable levels without extensively increasing the switching losses to improve the overall system performance.

## II. TURN-ON SWITCHING BEHAVIOR OF IGBTs

The turn-on switching behavior in a half-bridge configuration with an inductive load is shown in Fig. 1. The turn-on characteristic is divided into four distinct sections, as described in [4]. These sections are represented in Fig. 2 using different colors: cyan, green, gray and yellow.

- Before the IGBT  $T_2$  is turned on: The diode of  $T_1$  carries the current of  $I_L$  and IGBT  $T_2$  remains turned off.
- Section 0 (S0, cyan): The gate-emitter voltage  $v_{GE,2}$  rises until it reaches the threshold voltage  $V_{GE,th}$ . During this phase, the collector current remains zero because the IGBT is not yet in conduction mode. Consequently, there is no voltage drop across the stray inductance, and thus no voltage drop across the collector-emitter terminals of the IGBT  $T_2$ .
- Section 1 (S1, green): The gate voltage continues to rise, and the current starts to commutate. Consequently, a voltage drop occurs across the stray inductance, causing the collector-emitter voltage to decrease.
- Section 2 (S2, gray): The Miller plateau is reached, and the gate-emitter voltage ceases to rise as the gate

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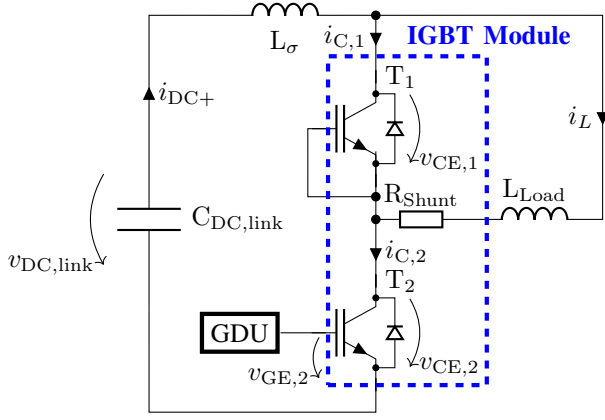


Fig. 1. Schematic of a half-bridge with an inductive load and the stray inductance

current flows through the Miller capacitance. The reverse-recovery current of the diode of  $T_1$  decreases until  $i_{C,2}$  equals the output load current  $i_L$ . The voltage commutes from the diode to the IGBT.

- Section 3 (S3, yellow): The Miller capacitance becomes fully charged, and the gate voltage rises to the driving voltage. The collector-emitter voltage continues to decrease until reaching saturation at  $v_{CE,sat}$ .

Only the first part of section 1 and the section 2 are important for controlling the maximum  $dv/dt$ .

- Section 1:  $dv/dt$  caused by  $d^2i_{C,2}/dt^2$   
Change of  $di/dt$ , which causes a  $dv/dt_{S1}$  across the stray inductance  $L_\sigma$ , as given by the following equation:

$$V_{DC,link} = L_\sigma \frac{di_{DC+}}{dt} + v_{CE,1} + v_{CE,2} \quad (1)$$

$$i_{DC+} = i_{C,1} + i_L \quad (2)$$

Differentiating of (2) under assumption of a constant  $i_L$  gives

$$\frac{di_{DC+}}{dt} = \frac{di_{C,1}}{dt} \quad (3)$$

Assuming that  $v_{CE,1} = 0$  because the diode still conducts and substituting (3) into (1) results in

$$V_{DC,link} = L_\sigma \frac{di_{C,1}}{dt} + v_{CE,2} \quad (4)$$

Under the assumption of a constant  $V_{DC,link}$ , differentiating (4) with respect to time gives

$$\frac{dv_{CE,2}}{dt} = -L_\sigma \frac{d^2i_{C,1}}{dt^2}. \quad (5)$$

- Section 2:  $dv/dt_{S2}$  caused by voltage commutation from diode to IGBT

This section can be controlled by adjusting the duration of the Miller plateau. The proposed method can adjust both  $di/dt$  and  $dv/dt_{S2}$  of the IGBT, making it possible to control the maximum  $dv/dt$ .

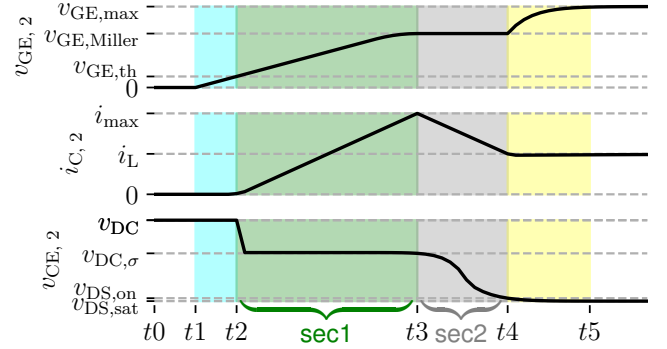


Fig. 2. Idealized turn-on behavior of the IGBT  $v_{GS}$ ,  $i_C$  and  $v_{CE}$  divided into four main sections according to [4]

### III. PROPOSED METHOD

#### A. Motivation and Requirements

For this application, the IGBT half-bridge module *IFF750B12ME7\_B11* in the EconoDUAL™ 3 package is used [11]. It consists of TrenchStop™ IGBT7 chips with an integrated shunt resistor. The internal gate resistance is  $0.5 \Omega$ .

This control method is also suitable for  $di/dt$  control and, therefore, for current balancing in IGBT modules connected in parallel. Due to the high importance of an IGBT parallel connection this feature is considered in the gate drive unit design. In addition, the gate drive unit should fulfill the following requirements:

- Balancing the current in a parallel connection of modules.
- Controlling the maximum  $dv/dt$  within a range of  $1 \text{ kV}/\mu\text{s}$ .

Thus, the gate drive unit should be able to:

- Deliver a peak current of  $I_{Peak} = 30 \text{ A}$ .
- Operate at a maximum DC-link voltage of  $v_{DC,link} = 800 \text{ V}$ .
- Generate different gate voltages during the switching period, which lasts a few  $100 \text{ ns}$ .
- Accurately adjust the on-state voltage during the on-state period.

This paper presents the results of controlling the maximum  $dv/dt$ . The other features of the gate unit will be elaborated at a later time.

According to [5], active gate drive units can be divided into different types, primarily the 1-step-, 2-step- and 4-step-control. The approach of using multiple voltage steps to drive the gate of an IGBT is shown in [6]. The authors modify the positive and negative supply voltage of the driving circuit to alter the behavior of the IGBT. Another technique to control the IGBT behavior is switching parallel resistors to increase the gate current [7]. In [8], a method with a 10 bit-DAC and a Class-B current amplifier stage is presented. The output current of the proposed method is realized with bipolar junction transistors (BJTs). Each transistor can drive a maximum current of  $3 \text{ A}$ , which is why a parallel configuration

of transistors was used. The technique presented in [9] controls the gate current by setting the  $V_{GS}$  of a MOSFET operating in saturation mode. A high precision DAC is connected to the gate and source terminals to control the saturation voltage, thereby adjusting the drain current used to drive the IGBT. In [10], an operational amplifier circuit composed of an adder and an amplifier is used to control the gate voltage. The output voltage is determined by control signals that modify the voltage divider ratio within the adder circuit, thereby adjusting the input to the voltage amplifier and hence the voltage applied to the IGBT gate.

The proposed method in this paper proposes a low-cost approach for varying the gate voltage using a flexible architecture with a low-voltage, low-cost, high dynamic range DAC and a powerful Class-B current amplifier to supply the required high gate current. As this method controls the gate voltage and, consequently, also the gate current, the external gate resistor is no longer needed, reducing the component count.

### B. Description of the Overall System

The schematic structure of the proposed gate drive unit, including feedback of the output current  $i_L$  and the maximum  $dv/dt$ , is depicted in Fig. 3. An FPGA controls the gate drive unit by switching the low-voltage MOSFETs (*RE1C001UN* [12]) in the DAC block. The *THS3491* voltage amplifier from TI [13] amplifies the resulting DAC voltage to the driving voltage level for the IGBT. The Class-B amplifier functions as a current amplifier, consisting of one n-channel MOSFET (*RD3H200S* [14]) and one p-channel MOSFET (*RD3H160SPTL1* [15]) from ROHM Semiconductor. This amplifier supplies the necessary gate current of at least 30 A to drive the IGBT.

The output current of the half-bridge IGBT module is sensed using an integrated shunt resistor. A  $\Delta\Sigma$ -ADC measures the voltage drop across this resistor and transmits the data back to the FPGA. The maximum  $dv/dt$  is determined using a peak detector [16], and its maximum voltage is measured by another  $\Delta\Sigma$ -ADC, whose bit stream is then fed back to the FPGA.

## IV. SIMULATION OF THE CONTROL STAGE

An LTspice simulation of the control stage for IGBT turn-on is shown in Fig. 4.

The simulation demonstrates how the  $dv/dt$  during the IGBT turn-on can be actively adjusted by varying the gate voltage. However, the effect of  $di/dt$ , which induces  $dv/dt$  across the stray inductance, is not considered in this simulation.

The figure presents two different scenarios, represented in blue and red, corresponding to pulse patterns P1 and P2. The upper figure shows the output voltage of the Class-B amplifier  $v_{out}$  (dotted line) and the internal gate-emitter voltage  $v_{GE,int}$  (solid line) behind the internal Gate resistor  $R_{int}$  at the gate connection, along with the corresponding Miller plateau duration. The lower Figure depicts the gate currents  $i_G$ .

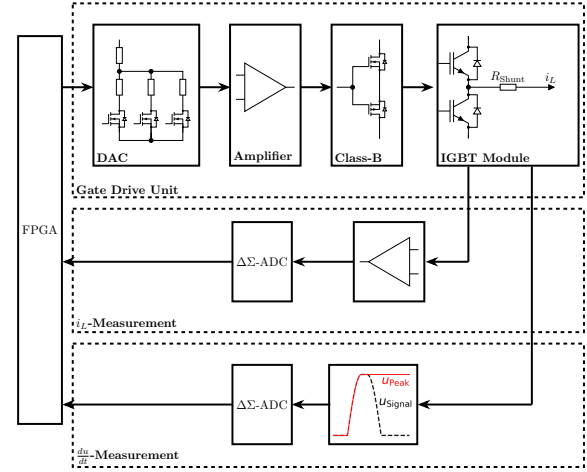


Fig. 3. Schematic structure of the gate unit with DAC, voltage amplifier, Class-B current amplifier, and feedback measurement of output current and maximum  $dv/dt$

TABLE I  
EQUIPMENT USED FOR TESTING THE PROTOTYPE

	Device	Description
Power supply	EA-PS 91500-30	$i_{max} = 30 \text{ A}$ , $v_{max} = 1.5 \text{ kV}$ , $p_{max} = 15 \text{ kW}$
Oscilloscope	Tektronix MSO46	$f_{BW} = 500 \text{ MHz}$ , $f_s = 5 \text{ GS/s}$
Rogowski Coil	CWT15B	$i_{max} = 3 \text{ kA}$
High voltage differential probe	BumbleBee	$f_{max} = 400 \text{ MHz}$ , $v_{max} = 1 \text{ kV}$
Low voltage differential probe	Saker	$v_{max} = \pm 25 \text{ V}$

The gate voltage level is varied using the DAC. The red curve represents the case where 17 V is applied earlier. As soon as the 17 V is applied to the gate, the voltage at the output of the Class-B amplifier rises, and the current  $i_G$  starts to increase according to

$$i_G = \frac{v_{out} - v_{GE,int}}{R_{ext} + R_{int}} \quad (6)$$

where  $R_{ext}$  is the external resistor, and  $R_{int}$  is the internal resistance of the IGBT module.

A higher gate current results in a faster switching transition, as the switching time is correlated with the gate charge  $Q_G$  according to

$$Q_G = \int i_G \cdot dt. \quad (7)$$

## V. VERIFICATION OF THE METHOD

### A. Test Setup

The prototype for the proposed method is tested in a double-pulse testbench. The measurement equipment and voltage source are listed in table I.

The IGBT module equipped with its gate drive unit is shown in Fig. 5. The proposed prototyped gate drive unit is positioned on top of the Infineon IGBT module. The output of the IGBT half-bridge is connected to an inductance of  $L_{Load} = 100 \mu\text{H}$

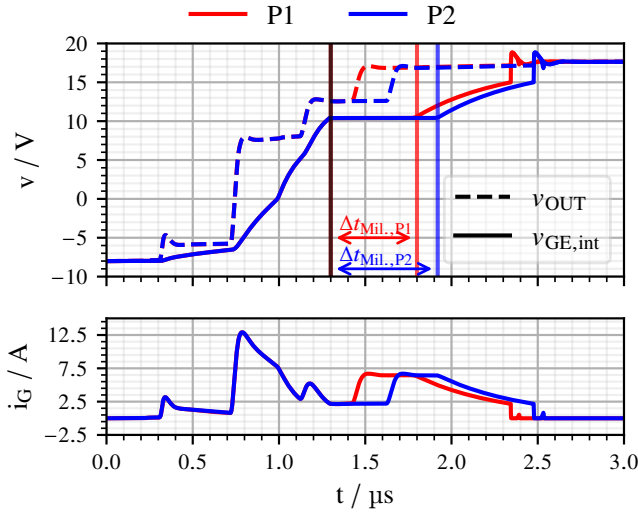


Fig. 4. Simulation results of the control stage using LTspice, where one of the small-signal MOSFETs in the DAC is switched at two different times to alter the duration of the Miller plateau

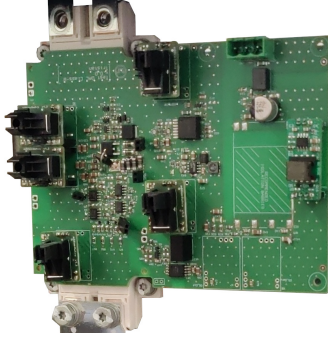


Fig. 5. Realized gate drive unit mounted on top of the IGBT

and to the positive rail of the DC-link, as can be seen in Fig. 1. To test the gate drive unit, a double-pulse test is conducted, characterizing the low-side switch.

The following results are conducted with an external resistor of  $R_{\text{ext}} = 0 \Omega$ , which results in a gate voltage  $v_{\text{GE}} = v_{\text{out}}$  and a maximum gate voltage of 17 V. Since the gate drive unit can precisely control the gate voltage, the need for an external gate resistor is eliminated. To achieve higher gate currents and to adjust the on-state-voltage in later test, a slightly increased gate voltage is used.

### B. Measurement Results of the Proposed Method with Time Control

In Fig. 6, a pulse pattern with four voltage steps is shown. The gate-emitter voltage  $v_{\text{GE}}$  transitions from the negative voltage to 6 V, 12.5 V and finally 17 V. The duration of the 12.5 V-level gate voltage level is varied systematically. The resulting maximum  $dv/dt$  and the maximum  $di/dt$  are shown in Fig. 7. If the driving voltage remains at 12.5 V for an extended period, the  $dv/dt$  is reduced, as the rise to the

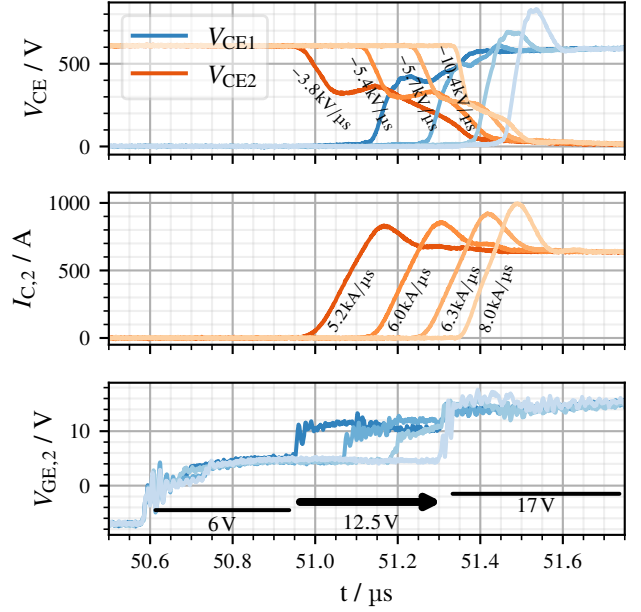


Fig. 6. Turn-on waveforms of the collector-emitter voltage, gate-emitter voltage, and collector current of transistor T2 for an example gate voltage pattern.

threshold voltage  $V_{\text{GE,th}}$  and the Miller plateau  $V_{\text{GE,Miller}}$  is reduced. The time interval between  $V_{\text{GE,th}}$  and  $V_{\text{GE,Miller}}$  determines the  $di/dt$ , while the duration of the Miller plateau determines the  $dv/dt$ , as illustrated in Fig. 2. In contrast, directly stepping the driving voltage from 6 V to 17 V, both the resulting  $di/dt$  and  $dv/dt$  reach higher values, as the  $V_{\text{GE,th}}$  and  $V_{\text{GE,Miller}}$  are attained in shorter time intervals.

In Fig. 7, the mean  $di/dt$  of IGBT T2 and the maximum  $dv/dt$  are plotted against the duration of the 12.5 V level applied to the gate of the IGBT. As the gate drive voltage remains at 12.5 V for a longer duration, the gate current is decreased, leading to a reduction in both  $di/dt$  and  $dv/dt$ . The  $di/dt$  of IGBT T2 is shown in gray, while the maximum  $dv/dt$  values for the two sections of IGBT T2 are shown in blue and orange. The  $|dv/dt|$  of the first section is significantly higher than that of the second section. Therefore the primary objective is to reduce the  $dv/dt$  of the first section.

- S1 (blue): The  $dv/dt$  of section 1 can be controlled within a range of approximately  $-10.5 \text{ kV}/\mu\text{s}$  to  $-3.5 \text{ kV}/\mu\text{s}$ .
- S2 (orange): The  $dv/dt$  of the second section remains relatively constant at around  $-3 \text{ kV}/\mu\text{s}$ . However, the results indicate that  $dv/dt$  in this section can also be controlled, with values dropping below  $-2 \text{ kV}/\mu\text{s}$ .

The  $dv/dt$  values for IGBT T1 are divided into two parts:

- First part: The period until the current reaches  $I_{\text{max}}$ . The corresponding rising  $dv_{\text{CE},1}/dt_{\text{r,max}}$  is positive (green). It is initially high but can be effectively controlled by reducing  $di/dt$ . The  $dv/dt$  decreases from approximately  $-16 \text{ kV}/\mu\text{s}$  to  $-8 \text{ kV}/\mu\text{s}$ .

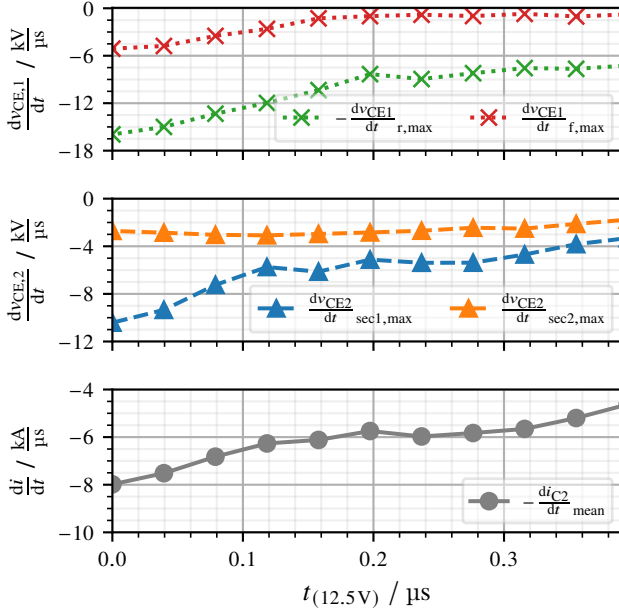


Fig. 7. Results of  $di/dt$  and  $dv/dt$  of the measurement over the length of the 12.5 V pulse

- Second part: The period in which the current  $i_{C,2}$  falls from  $I_{max}$  to  $I_L$ . The corresponding falling  $dv_{CE,1}/dt_{f,max}$  is negative (red) and can be controlled within a range of approximately  $-5 \text{ kV}/\mu\text{s}$  to  $-1 \text{ kV}/\mu\text{s}$ .

The result in Fig. 7 confirm the primary goal of controlling the global maximum  $dv/dt$  over a wide range.

The resulting losses for this pulse pattern are presented in Fig. 8. The solid lines represent the resulting energy losses of this configuration, while the dotted lines show the datasheet values at room temperature and an external gate resistor of  $R_{ext} = 0.5 \Omega$  and a gate voltage of  $V_{Gate} = 15 \text{ V}$ . The datasheet losses are higher when the duration of the 12.5 V voltage level is either zero or minimal, as the external gate resistor is zero and the driving voltage reaches fast 17 V. However, as the duration of the 12.5 V voltage level increases, the turn-on energy loss  $E_{on}$  and the total energy loss  $E_{total}$  increase, whereas the reverse recovery loss  $E_{rec}$  decreases.

### C. Measurement Results of the Proposed Method with Time and Voltage Level Control

To optimize the maximum  $dv/dt$  in a more loss-efficient manner, a more sophisticated puls pattern, as depicted in Fig. 9, is tested. The new pulse pattern consist of flexible voltage levels to precisely control  $dv/dt$  in both sections. Different gate voltages are applied in each section with the objective to optimize

- the delay time by applying a high voltage in section zero.
- the maximum  $dv/dt$  by reducing the  $di/dt$  in section 1.
- the losses. As the  $dv/dt$  in section 1 is low after the current rises and becomes linear, a higher voltage to

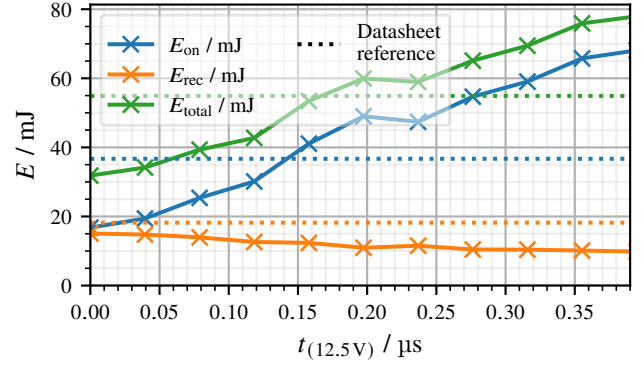


Fig. 8. Losses over the length of the 12.5 V pulse

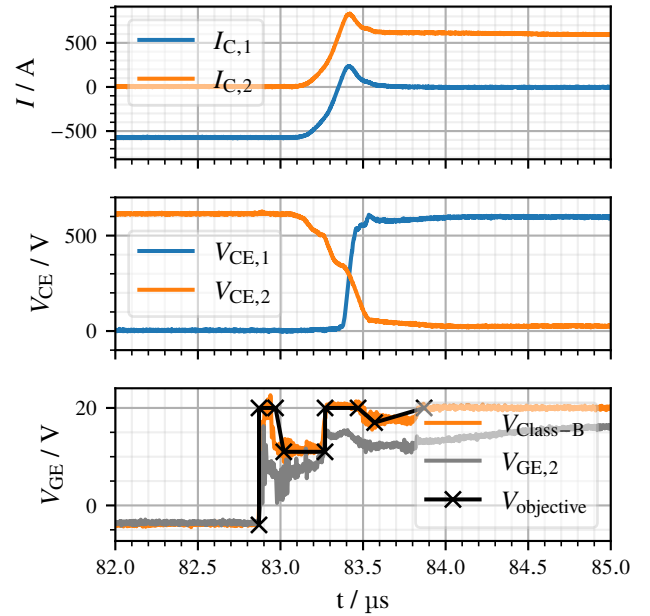


Fig. 9. IGBT turn-on transition with five voltage steps to control the  $dv/dt$  and its losses

the gate is applied to accelerate the commutation of the current which leads to a steeper current slope and a higher  $dv/dt$ .

- the maximum  $dv/dt$  by lowering the voltage commutation and thus the  $di/dt$  in section 2.
- the losses, by applying a higher gate driving voltage to increase the dynamic gate drive unit performance regarding changes of the gate current and to accelerate the drop of the drain-source voltage.

After the collector-emitter voltage drops to a low level, a gate voltage of 15 V is applied to limit the maximum current in the event of a short circuit.

The graphs in Fig. 10 show the maximum  $dv/dt$  and the corresponding losses compared to reference measurements using a state-of-the-art control with different gate resistors at a

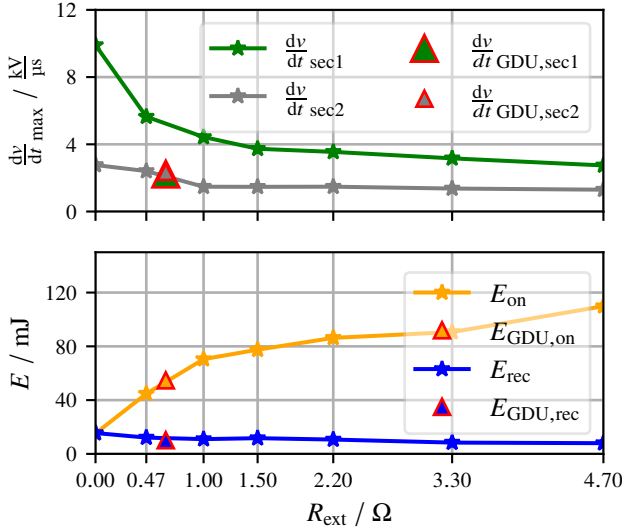


Fig. 10. Results of the optimized gate voltage applied to the gate and its maximum  $dv/dt$  and its losses compared to reference measurements with different gate resistors and a gate voltage of 15 V

fixed gate drive voltage of 15 V. The x-axis indicates the gate resistor values, while the y-axis represents the measured maximum  $dv/dt$  and switching losses. The results obtained using the optimized pulse pattern are marked with triangles in both plots. The  $dv/dt$  values in both sections are nearly identical, demonstrating the goal of reducing  $dv/dt$  while maintaining low losses. The resulting losses correspond approximately to those observed with a gate resistor of about 0.5  $\Omega$ . The loss of  $E_{GDU,rec}$  is lower than in the reference measurement as the current commutation is accelerated by the increased gate voltage. This also induces a stronger reverse recovery current spike which leads to a higher voltage drop across the stray inductance  $L_\sigma$ . In this test setup, the IGBT's maximum voltage rating is not exceeded and therefore, the losses associated with the commutation can be reduced.

## VI. CONCLUSION

This paper presents the realization of a gate drive unit capable of flexibly adjusting the gate voltage to control the maximum  $dv/dt$  during the turn-on switching transition. The primary objective of controlling and reducing the maximum  $dv/dt$  is to reduce the  $dv/dt$  at the converter output and the insulation stress on the motor windings. The proposed method achieves this by controlling

- the  $di/dt$  in the first section and
- the  $dv/dt$  in the second section

of an IGBT switching transient. The effectiveness of this approach is demonstrated through both LTspice simulations and experimental results. The  $dv/dt$  and  $di/dt$  plots validate the proposed method, showing that adjusting intermediate gate voltage levels significantly impacts the switching transients.

Additionally, the energy loss analysis reveals a trade-off between  $dv/dt$  and efficiency. The experimental results con-

firm that the maximum  $dv/dt$  can be controlled within a wide range.

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