

INPUT REFERRED NOISE REDUCTION TECHNIQUE FOR TRANSCONDUCTANCE AMPLIFIERS

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ABSTRACT

In this paper, a useful procedure to design folded cascode (FC) and recycling folded cascode (RFC) OTAs is presented. The proposed procedure is based on a simplified equation of input voltage noise in strong and weak inversion regions. The presented method considerably decreases the input referred noise of amplifiers in weak, moderate and strong inversion. The proposed amplifiers were simulated in 0.18 μ m CMOS technology, achieving 36% and 25% reduction of input voltage noise @ 1Hz in strong and weak inversion, respectively, compared to the conventional FC, without increasing power consumption and silicon area.

KEYWORDS

Flicker noise, Weak inversion, Folded cascode, CMOS amplifier, G_m/I_d methodology

1. INTRODUCTION

The operational transconductance amplifier (OTA) is an important block used as analogue-to-digital (A/D) converters and switched-capacitor filters. Newly, the folded cascode (FC) structure is preferred over the telescopic configuration due to the low voltage characteristics, despite the higher power budget [1, 2]. Moreover, to enhance performance of the FC amplifier, the recycling folded cascode structure (RFC) has been presented. The RFC structure has better DC gain, gain bandwidth and slew rate compared to the FC [3-5]. The weak inversion operation is a common approach when considering the market trend towards low-voltage and ultra-low-power applications [6, 7]. Also, the frequency response, power supply voltage, and power consumption are key design parameters. Therefore, there is a trade-off between signal swing and frequency response [1, 6]. MOS transistors biased at higher current densities are faster, but require larger drain-source voltage. The required drain-source voltage for saturation of transistor in weak inversion is smaller than strong and moderate inversion, thus the signal swing in weak inversion is larger than the other regions. However, frequency response will be degraded because of extremely low currents. In MOSFETs, the flicker noise is the dominant noise at the low frequency range [2, 7]. In addition, extra energy states in SiO₂ and Si boundaries generate further flicker noise. Therefore, the flicker noise is a key parameter for considering in weak inversion circuit design [8-10].

Some techniques for flicker noise reduction have been recently presented in [11, 12] and some strategies to reduce the DC offset in multipliers have been proposed in [13, 14] by chopper technique. Nonetheless, these methods lead to enhance power budget and area. Also in [3, 15, 16], the input referred flicker noise is reduced due to improved transconductance in RFC amplifier without enhancing power consumption. On the other hand, larger active loads and dimension of transistors significantly enhance the silicon area as well as the parasitic capacitance.

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Therefore, to move the parasitic poles to higher frequencies more power consumption will be needed [4, 5]. Thus, enhancing noise performance without increasing power budget and silicon area is recently an open challenge for analogue circuit designers.

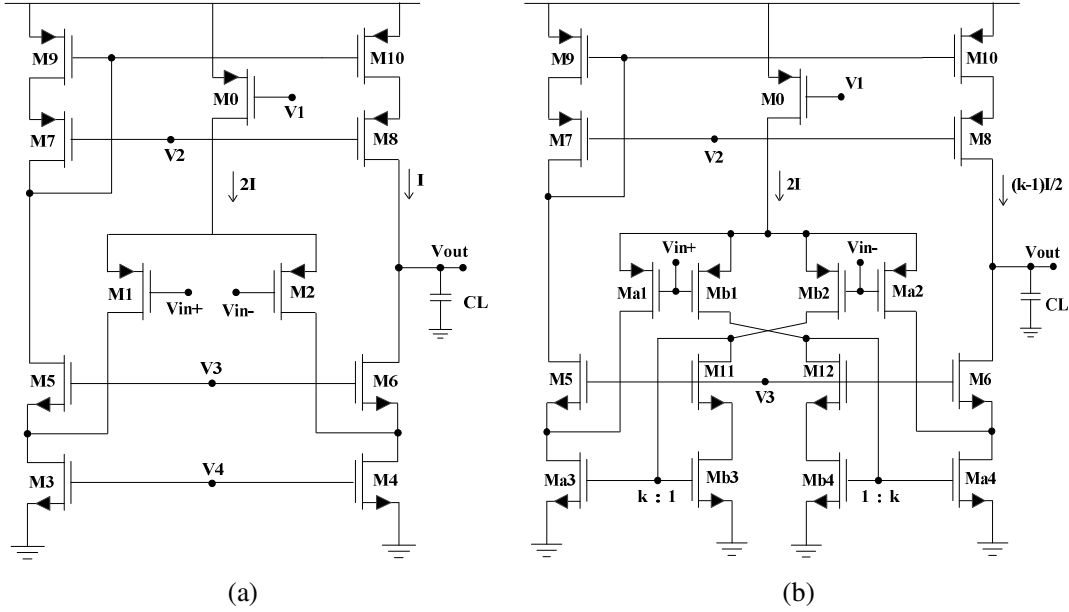


Figure 1. Folded cascode amplifiers: (a) FC amplifier and (b) RFC amplifier.

In this paper, a new formulation for input referred flicker noise in weak and strong inversion regions amplifier configurations is presented, that introduces a design technique for flicker noise reduction based on increasing length of some transistors. The presented design methodology is used to design the FC and RFC amplifiers with decreased input voltage noise, without increasing the power budget and phase margin degeneration. The rest of the paper is organized as follows. Section 2 describes the RFC configuration. The reduction noise method is described in Section 3 based on Gm/I_d characteristic. The simulation results of the proposed technique are discussed in Section 4 followed by a conclusion in Section 5.

2. RFC STRUCTURE

The FC amplifier is shown in Fig. 1a. In this figure, transistors M3 and M4 have usually the largest drain current and accordingly the largest transconductance. To address this inefficiency, an alternative configuration, the RFC architecture [3-5] has been proposed (Fig. 2b). The transconductance of the FC structure is $Gm_{FC} = gm_1$, which is referred to the input transistors. It is well-known to have better DC gain, gain bandwidth and slew rate the transconductance of the proposed structure should be enhanced. Also increasing transconductance leads to the lower input referred noise because the current noise of transistors M3, M4, M9 and M10 are referred to the input by the transconductance [3-5]. In the RFC amplifier, Ma3 and Ma4 are used to increase the transconductance without enhancing power consumption ($k=3$) by a factor of two compared to the FC amplifier [3-5].

$$Gm_{RFC} = gm_{a1}(k+1) = 2gm_1 \quad (1)$$

This modification improves DC gain, gain-bandwidth, slew rate and noise performance. However; adding the recycling part may limit the phase margin by adding a pole expressed as (2) [3].

$$\omega_{RFC}^{p2} = -\frac{gm_{b3}}{(k+1)(C_{GB} + C_{GS})_{b3}} \quad (2)$$

For suitable phase margin, we should have $\omega_{p2} \geq 3\omega_u$ thus having the parameter k satisfying the following inequality (3) [4].

$$k_{RFC} \leq \sqrt{\frac{gm_{b3}C_L}{3gm_{a1}(C_{GB} + C_{GS})_{b3}}} - 1 \quad (3)$$

3. PROPOSED NOISE REDUCTION METHOD

To reduce the input referred flicker noise in weak, moderate and strong inversion the length of effective MOS transistors can be increased but at the cost of lower current. To overcome this matter, some compensation parameters such as the gate-source voltage and the transistor width W are considerable. Therefore in the moderate inversion, a trade-off between the drain-source voltage swing and the silicon area is usually performed. In this region, V_{GS} and W are both varied to compensate the length increasing. Due to low frequency operation in weak, moderate and strong inversion, flicker noise is the most important noise source in this circuit. The maximum current noise at the drain-source of a MOSFET is described by (4) [8-10].

$$\overline{i_o^2} = \left[4k_B T \gamma gm + \frac{K_F gm^2}{C_{ox} LWf} \right] \quad (4)$$

The second term of equation (4) shows flicker noise contribution and it can be seen that increasing the transistor dimensions will considerably decrease the flicker noise. By considering (5), the input referred flicker noise of the RFC amplifier is calculated by (6).

$$\begin{aligned} Gm_{RFC} &= (k+1)gm_{a1}, gm_{a1} = gm_{b1}, (WL)_{a3} = k(WL)_{b3}, \\ k gm_{b3} &= gm_{a3}, (WL)_{a1} = (WL)_{b1}, L_{a3} = L_{b3} \end{aligned} \quad (5)$$

$$\overline{V_{RFC}^2} = 2 \frac{K_{fp}}{C_{ox} f (k+1)} \cdot \left[\frac{1+k^2}{(WL)_{a1} (k+1)} + \frac{K_{fn}}{K_{fp}} \cdot \frac{gm_{a3}^2}{(WL)_{a3} gm_{a1}^2} + \frac{gm_9^2}{(WL)_9 (k+1) gm_{a1}^2} \right] \quad (6)$$

3.1. Strong Inversion

To consider the flicker noise reduction method, it is assumed that all devices operate in the strong inversion region with a simplified DC transconductance model given by

$$gm^2 = 2\mu C_{ox} \frac{W}{L} Id \quad (7)$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the transistor dimensions and Id is the drain current. The input referred flicker noise of the RFC amplifier can be found by replacing (7) in (6).

$$\overline{V_{RFC}^2} = 2 \frac{K_{fp}}{C_{ox} f (k+1)} \cdot \left[\frac{1+k^2}{(WL)_{a1} (k+1)} + \left(\frac{K_{fn} C_{ox}^2 \mu_n^2}{K_{fp} gm_{a1}^2} \right) \frac{W_{a3}}{(L_{a3})^3} V_{eff,a3}^2 \right. \\ \left. + \left(\frac{C_{ox}^2 \mu_p^2}{(k+1) gm_{a1}^2} \right) \frac{W_9}{(L_9)^3} V_{eff,9}^2 \right] \quad (8)$$

$$\overline{V_{if}^2}_{Cascade,Recycle} \propto \left[\frac{W}{(L)^3} V_{eff}^2 \right] \quad (9)$$

where V_{eff} is the effective voltage in strong inversion region. It can be concluded from equation (9), which increasing the MOSFET length (L) leads to the lower input referred flicker noise of cascade and recycling part transistors. It will also decrease the drain current of transistors and subsequently, their transconductance. In order to compensate of such current reduction, width of transistor or gate-source voltage as two compensation parameters can be increased. Increasing the transistor width leads to the phase margin degradation. So increasing the gate-source voltage can be the best approach to reduce the input referred flicker noise without current attenuation of the cascade and recycling part transistors in the strong inversion. It can be concluded from (9), increasing the gate-source voltage generates more input referred flicker noise but since length increment has much more impact on noise than gate-source voltage. However, there is a trade-off between silicon area and voltage swing, because increasing transistor gate-source voltage leads to the larger effective voltage and accordingly reduces the drain-source voltage swing. As illustration for strong inversion, by assuming $L_{new}=xL_{old}$, $W_{new}=(1/x)W_{old}$ and $(V_{eff, new})=x(V_{eff, old})$, the silicon area and drain current will remain constant while the input referred flicker noise from cascode and recycling part transistors will be reduced by a factor of x^2 , such as

$$\overline{V_{if}^2}_{Cascade,Recycle} \propto \left[\frac{W_{new}}{(L_{new})^3} (V_{eff, new})^2 \right] = \frac{1}{x^2} \left[\frac{W_{old}}{(L_{old})^3} (V_{eff, old})^2 \right] \quad (10)$$

In this condition, drain-source voltage will be reduced by value of x Volt. To determine the maximum length value of Mb3 and Ma3, the gate-source capacitor in strong inversion was replaced with $2C_{ox}WL/3$ in (3) while neglecting the gate-bulk capacitor.

$$L_{a3,b3} \leq \frac{gm_{a3}}{gm_{a1}} \cdot \frac{C_L}{2C_{ox}W_{b3}(k+1)^2} = \frac{Id_{b3}}{Id_{a1}} \cdot \frac{V_{eff,a1}}{V_{eff,b3}} \cdot \frac{C_L}{2C_{ox}W_{b3}(k+1)^2} \quad (11)$$

Compared to the conventional FC, we considered $k=3$ and $Id_{b3}=Id_{a1}$ for the RFC amplifier to remain power dissipation constant, thus

$$L_{a3,b3}^{max} = \frac{V_{eff,a1}}{V_{eff,b3}} \cdot \frac{C_L}{32C_{ox}W_{b3}} \quad (12)$$

3.2. Weak inversion

In this work, we were interested in the weak inversion region for ultra-low-power operation. In this region, MOSFETs are in weak inversion with an extremely low drain current expressed as (13) [1, 7].

$$I_d = I_S \frac{W}{L} e^{\left(\frac{V_{GS}-V_{TH}}{nU_t} \right)} \left(1 - e^{\frac{-V_{DS}}{U_t}} \right) \xrightarrow{V_{DS} \geq 3U_t} I_d = I_S \frac{W}{L} e^{\left(\frac{V_{GS}-V_{TH}}{nU_t} \right)} \quad (13)$$

where V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, V_{TH} is the threshold voltage, n is the slope factor, $U_t=26mV$ in room temperature and I_S is the characteristic current in weak inversion that is given by (14) [2, 7].

$$I_S = 2nU_t^2 \mu C_{ox} \quad (14)$$

Therefore, the transconductance of a MOS transistor in the weak inversion region can be given by (15), that is a function of current and temperature [6, 7].

$$gm = \frac{\partial I_d}{\partial V_{GS}} = \frac{I_d}{nU_t} \quad (15)$$

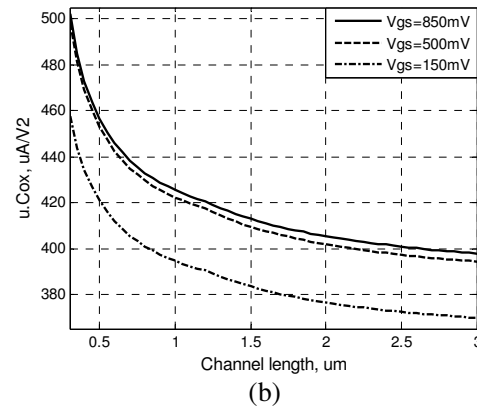
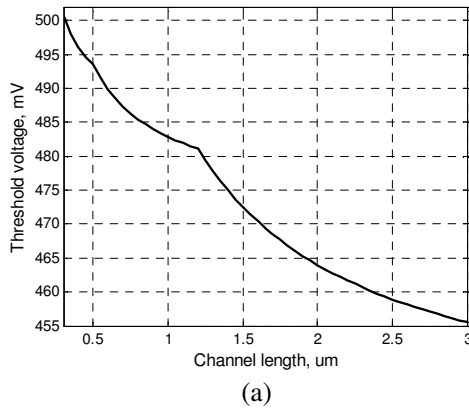
Therefore, the input referred flicker noise of the RFC amplifier in weak inversion can be found by replacing (15) in (6).

$$\overline{V_{if}^2}_{RFC} = 2 \frac{K_{fp}}{C_{ox} \cdot f(k+1)} \cdot \left[\frac{1+k^2}{(WL)_{a1}(k+1)} + \left(\frac{4K_{fN}U_t^2 C_{ox}^2}{K_{fp}gm_{a1}^2} \right) \mu_n^2 \frac{W_{a3}}{(L_{a3})^3} e^{2\left(\frac{V_{GS,a3}-V_{TH}}{n_{a3}U_t}\right)} \right. \\ \left. + \left(\frac{4U_t^2 C_{ox}^2}{(k+1)gm_{a1}^2} \right) \mu_p^2 \frac{W_9}{(L_9)^3} e^{2\left(\frac{V_{GS,9}-V_{TH}}{n_9U_t}\right)} \right] \quad (16)$$

So,

$$\overline{V_{if}^2}_{Cascode, Recycle} \propto \left[\mu^2 \frac{W}{(L)^3} e^{2\left(\frac{V_{GS}-V_{TH}}{nU_t}\right)} \right] \quad (17)$$

Similar to strong inversion, to reduce the input referred flicker noise the length of effective MOS transistors can be increased but at the cost of lower current. Therefore, the one approach to reduce the input referred flicker noise in weak inversion without current attenuation is increasing the transistor length and gate-source voltage of the cascode and recycling part transistors. However, increasing the gate-source voltage generates more input referred flicker noise. Note that according to (17), As illustration for weak inversion, by assuming $(V_{GS, new}) - (V_{GS, old}) = 2nU_t[\ln(x)]$, $L_{new} = xL_{old}$, $W_{new} = (1/x)W_{old}$ and neglecting the effect of other parameters, the current and input referred flicker noise from cascode and recycling part transistors will remain constant. Namely, the flicker noise reduction effect of length increment is equal to the flicker noise increment effect of increasing the gate-source voltage. With these qualities, simulation results have shown that increasing the MOSFET length and gate-source voltage can be used as the flicker noise reduction parameter and current compensation parameter in weak inversion region, respectively. Because value of parameters such as slope factor (n), career mobility (μ) and threshold voltage (V_{TH}) will change with increasing the MOSFET length and gate-source voltage. Increasing the MOSFET length and gate-source voltage lead to increase slope factor and decrease threshold voltage and carrier mobility, that are shown in Figs. 2a-c.



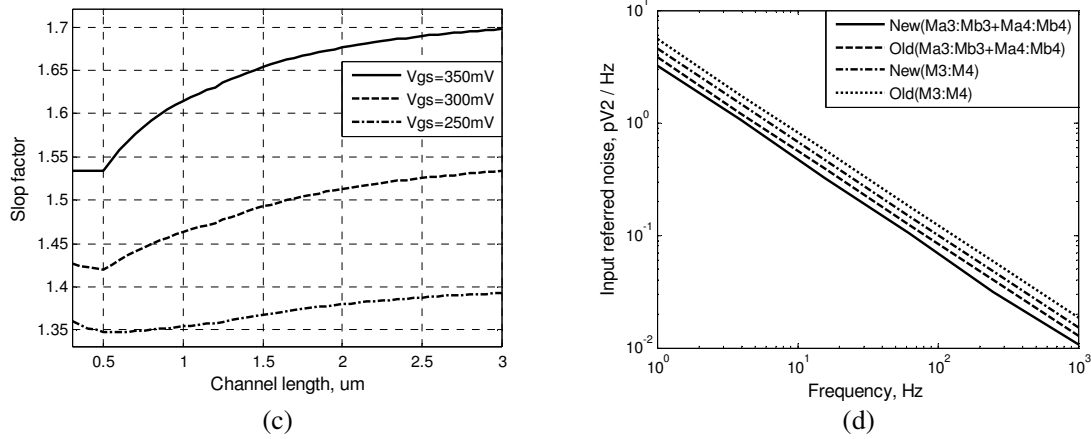


Figure 2. (a) Threshold voltage, (b) transconductance parameter ($C_{ox}\mu$), (c) slop factor versus MOSFET channel length and (d) total input referred flicker noise of the cascode and recycling part transistors in weak inversion for amplifiers.

By considering $L_{new}=xL_{old}$, $W_{new}=(1/x)W_{old}$ and illustration for weak inversion region, $n_{new} \geq n_{old}$, $V_{TH,new} \leq V_{TH,old}$, $\mu_{new} \leq \mu_{old}$ can be found from Fig. 2 to remain the silicon area constant. A complex equation will be achieved by replacing new parameters in drain current (13) to obtain value of $V_{GS, new}$ as the current compensation parameter. Nevertheless, placement of numerical values for the new and old parameters can show decreasing the input referred flicker noise without current attenuation. To confirm the accurately of this method, the low frequency total input referred flicker noise of the cascode and recycling part transistors in Fig. 1 (M3 with M4 and Ma3:Mb3 with Ma4:Mb4) have been shown in Fig. 2d.

Therefore, to further reduce the input referred flicker noise without current attenuation in weak inversion we can increase the MOSFET width that leads to larger die area. Consequently, the best approach to reduce the input referred flicker noise with current compensation due to larger length is increasing the gate-source voltage and MOSFET width in strong and weak inversion regions, respectively. Also, in accordance with the EKV model of MOSFETs operation in moderate inversion [17], increasing length can reduce the input referred flicker noise power. However, there is a trade-off between voltage swing and silicon area in this region, too. To determine the maximum length for Mb3 and Ma3, we replaced the gate-bulk capacitor in weak inversion with $C_{ox}WL$ in (3) while neglecting the gate-source capacitor.

$$L_{a3,b3} \leq \frac{gm_{b3}}{gm_{a1}} \cdot \frac{C_L}{3C_{ox}W_{b3}(k+1)^2} = \frac{n_{a1}Id_{b3}}{n_{b3}Id_{a1}} \cdot \frac{C_L}{3C_{ox}W_{b3}(k+1)^2} \quad (18)$$

In FC and RFC circuits with equal power dissipation, we considered $k=3$ and $Id_{b3}=Id_{a1}$. Also, to achieve minimum input referred flicker noise and obtain suitable phase margin, the maximum possible length for transistors Mb3 and Ma3 is given by (19).

$$L_{a3,b3}^{max} = \frac{n_{a1}}{n_{b3}} \cdot \frac{C_L}{48C_{ox}W_{b3}} \quad (19)$$

Since flicker noise of P-channel is less than N-channel, this process is not used for the current mirror transistors (M9 and M10).

3.3. Design methodology

In the Gm/Id design methodology, the relationship between the transconductance (Gm) over DC drain current Id and the normalized drain current $In = Id/(W/L)$ is considered as a design tool, because both the normalized current In and the Gm/Id ratio are independent of transistor dimensions [18, 19]. Therefore, the Gm/Id methodology can be introduced as a relative method to design the RFC amplifier. Hence, the equation (6) can be re-written based on Gm/Id and In as follows:

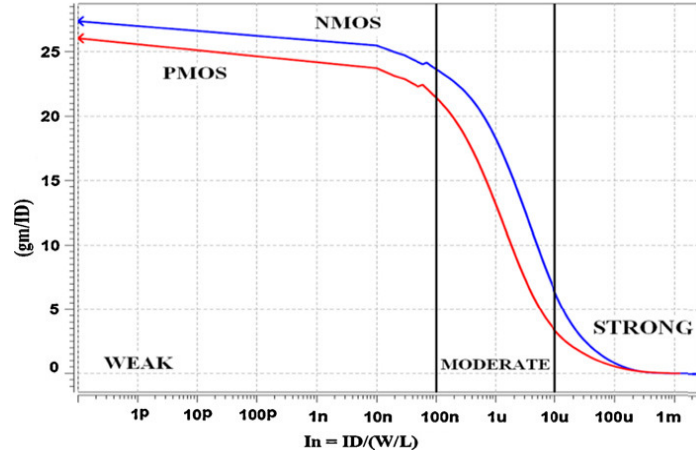
$$\overline{V_{RFC}^2} = 2 \frac{K_{JP} \left(\frac{gm_{a1}}{Id_{a1}} \right)^{-2}}{C_{oxf} (k+1)^2 Id_{a1}} \left[\frac{(1+k^2) \left(\frac{gm_{a1}}{Id_{a1}} \right)^2 \left(\frac{Id_{a1}}{W_{a1}/L_{a1}} \right)}{L_{a1}^2} + \frac{\frac{K_{fN}}{K_{fP}} \frac{k(k+1) \left(\frac{gm_{a3}}{Id_{a3}} \right)^2 \left(\frac{Id_{a3}}{W_{a3}/L_{a3}} \right)}{L_{a3}^2} + \frac{(k-1) \left(\frac{gm_9}{Id_9} \right)^2 \left(\frac{Id_9}{W_9/L_9} \right)}{L_9^2} \right] \quad (20)$$

Similar to equations (8) and (16), it can be seen from equation (20) that increasing the MOSFET length and decreasing the MOSFET width lead to reduce the input referred flicker noise of effective transistors but at the cost of lower current. In order to compensate this current reduction, the gate-source voltage can be increased [18]. The proposed methodology is illustrated using Gm/Id characteristic based on equation (20) as follows:

1. The simulated Gm/Id characteristic curve for both NMOS and PMOS type transistors in 0.18 μm CMOS technology is shown in Fig. 3 [19].
2. The (gm_{a1}/Id_{a1}) ratio should be increased to have a larger DC gain and unity gain bandwidth, and the smaller input referred flicker noise.
3. According to Fig. 3, increasing the (gm_{a1}/Id_{a1}) ratio leads to smaller In and V_{GS} (normalized drain current is a function of V_{GS}), and larger W in order to compensate the current reduction of the input transistors (Ma1, Mb1, Ma2 and Mb2) [18].
4. Therefore, increasing the W and decreasing the L and V_{GS} (larger Gm/Id) can be done as a useful approach to reduce the input referred flicker noise of the input transistors without current reduction.
5. To reduce the input referred flicker noise of the cascode and recycling transistors the (gm_{a3}/Id_{a3}) and (gm_9/Id_9) can be decreased.
6. According to Fig. 3, decreasing the (gm_{a3}/Id_{a3}) and (gm_9/Id_9) lead to larger In , V_{GS} and low frequency output impedance (larger DC gain), and smaller W to degenerate of such current enhancement of the transistors Ma3:Mb3, Ma4:Mb4, M9 and M10 [18].
7. Therefore, decreasing the W and increasing the L and V_{GS} (smaller Gm/Id) can be done as a useful approach to reduce the input referred flicker noise of the cascode and recycling part transistors without current reduction.
8. The dimension of the effective transistors can be easily calculated using Fig. 3, when the best values for Gm/Id and Id are chosen.
9. The maximum length of the cascode and recycling part transistors can be found by (12) and (19) in strong and weak inversion regions, respectively.
10. Upper boundary of current gain k can be obtained by (21) to achieve proper phase margin.
- 11.

$$k_{RFC}^{Strong \& Weak} \leq \sqrt{\frac{\left(\frac{gm_{b3}}{Id_{b3}} \right) \left(\frac{gm_{a1}}{Id_{a1}} \right)^{-1} \left(\frac{Id_{b3}}{W_{b3}/L_{b3}} \right) C_L}{[2 \& 3] C_{ox} L_{b3}^2 Id_{a1}}} - 1 \quad (21)$$

12. To reduce the input referred noise the (gm_{a3}/Id_{a3}) can be decreased and the (gm_{a1}/Id_{a1}) , In_{b3} and L_{b3} can be increased. These solutions lead to have lower k and the phase margin degeneration [20].
13. The slew rate of amplifier can be determined by power consumption limitation.


 Figure 3. Simulated Gm/Id characteristic in 0.18 μm CMOS technology [19]

4. SIMULATION RESULTS

The FC amplifier (Fig. 1a) and the RFC amplifier (Fig. 1b) were simulated in weak and strong inversion, first without using the proposed approach (thus denoted as FC and RFC, respectively) and then, while utilizing the proposed technique (thus denoted as PFC and PRFC, respectively). Table 1 shows the transistor sizes and component values that are used in the FC, PFC, RFC and PRFC amplifiers which operate in weak and strong inversion. It can be seen that transistors M3 and M4 in PFC and Ma3:Mb3, Ma4:Mb4 in PRFC have more value of length ($L_{\text{new}}=5L_{\text{min}}$, $L_{\text{old}}=2L_{\text{min}}$ and $WL_{\text{old}}=WL_{\text{new}}$) and less value of width compared to the conventional amplifiers. Therefore, current reduction is compensated by 50mV-150mV gate-source voltage enhancement.

The circuits were simulated using the 0.18 μm CMOS process. Supply voltage was chosen as 0.6 V for weak inversion and 1.8 V for strong inversion. Fig. 4 shows the DC Gain, the gain-bandwidth and the phase-margin of the four simulated amplifiers. Note that the proposed technique has negligible effect on the frequency response and the DC gain improvement, for both FC and RFC amplifiers. It is essential to note that the four amplifiers have the same die area and power consumption.

 Table 1. Amplifier device sizes (μm), bias voltages (V) and Gm/Id characteristics.

Components	Weak Inversion				Strong Inversion			
	FC	PFC	RFC	PRFC	FC	PFC	RFC	PRFC
M0	67/0.18	67/0.18	67/0.18	67/0.18	60/0.54	60/0.54	60/0.54	60/0.54
M1, M2	246/2	246/2	-	-	92/0.54	92/0.54	-	-
Ma1, Ma2	-	-	123/2	123/2	-	-	46/0.54	46/0.54
Mb1, Mb2	-	-	124/2	124/2	-	-	47/0.54	47/0.54
M3, M4	63/0.36	25/0.9	-	-	42/0.36	17.5/0.9	-	-
Ma3, Ma4	-	-	47/0.36	19/0.9	-	-	32/0.36	13.5/0.9
Mb3, Mb4	-	-	16/0.36	6/0.9	-	-	10.6/0.36	4.5/0.9
M5, M6	108/0.36	108/0.36	108/0.36	108/0.36	4/0.54	4.6/0.54	4/0.54	4.6/0.54

M7, M8	513/0.36	513/0.36	513/0.36	513/0.36	24/0.54	24/0.54	24/0.54	24/0.54
M9, M10	105/2	105/2	105/2	105/2	30/0.54	30/0.54	30/0.54	30/0.54
M11, M12	-	-	55/0.36	54/0.36	-	-	2/0.54	2.3/0.54
$(Gm/Id)_{3,4}$	28.41	26.36	-	-	14.85	7.13	-	-
$(Gm/Id)_{a3,a4}$	-	-	28.41	26.36			14.83	7.15
$(Gm/Id)_{b3,b4}$	-	-	28.41	26.36			14.83	7.15
V1	0.3	0.3	0.3	0.3	1.1	1.1	1.1	1.1
V2	0.3	0.3	0.3	0.3	0.75	0.75	0.75	0.75
V3	0.3	0.3	0.3	0.3	0.95	1.05	0.95	1.05
V4	0.25	0.3	-	-	0.55	0.7	-	-
$V_{in_{cm}}$	0.3	0.3	0.3	0.3	0.9	0.9	0.9	0.9

In addition, Fig. 5 shows the input referred noise of the designed amplifiers versus frequency in weak and strong inversion. It is obvious from Fig. 5 that the presented technique significantly reduces the noise power for both RFC and FC amplifiers in weak and strong inversion. The input referred noise of the FC, PFC, RFC and PRFC @ 1Hz is $3.88\mu V/\sqrt{Hz}$, $3.59\mu V/\sqrt{Hz}$, $3.13\mu V/\sqrt{Hz}$ and $2.89\mu V/\sqrt{Hz}$ in weak inversion and $7.21\mu V/\sqrt{Hz}$, $5.59\mu V/\sqrt{Hz}$, $5.71\mu V/\sqrt{Hz}$ and $4.57\mu V/\sqrt{Hz}$ in strong inversion, respectively. While, the maximum phase-margin degeneration is 3.98° for the PRFC amplifier compared to the RFC amplifier in strong inversion. Note that the silicon area and bias current remain constant, slew rate of the four amplifiers have not degeneration.

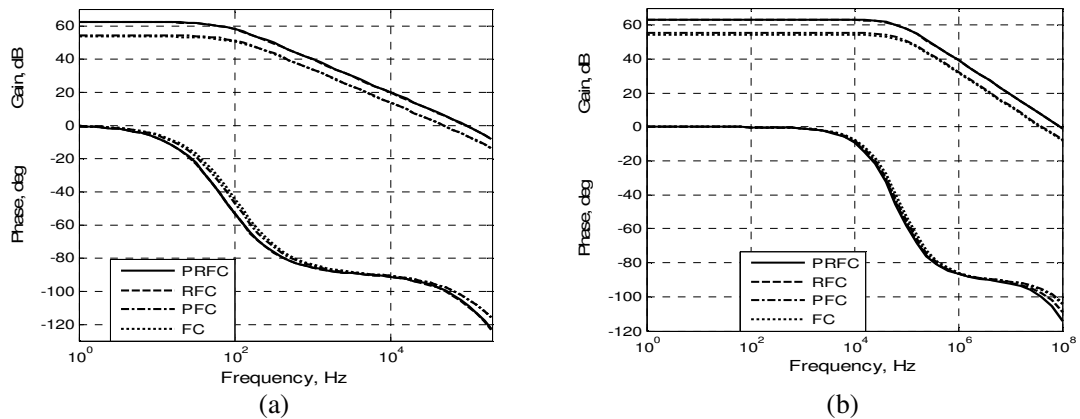


Figure 4. Frequency response of simulated amplifiers (a) in weak inversion region and (b) in strong inversion region.

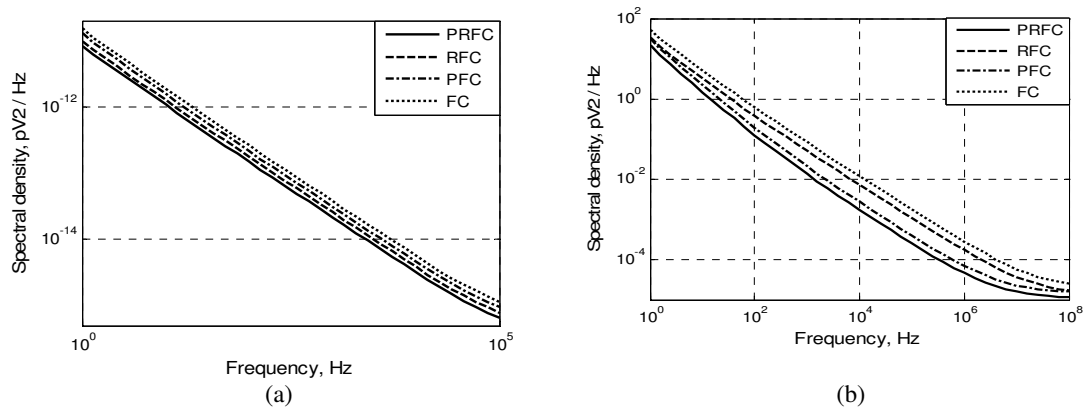


Figure 5. Total input referred noise for designed amplifiers (a) in weak inversion region and (b) in strong inversion region.

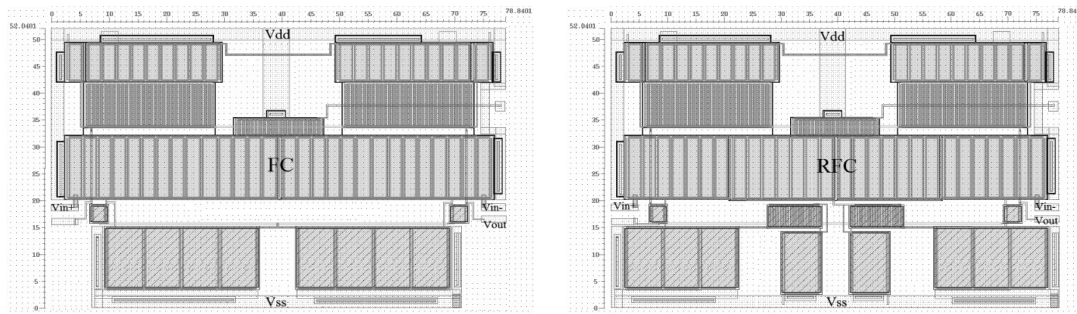


Figure 6. Layout of the proposed amplifiers in weak inversion region.

Process corners (TT, SS, FF, SF and FS) and temperature variation (from -10°C to $+90^{\circ}\text{C}$) are reported to demonstrate the global variation of the flicker noise reduction method. The important specifications of the PRFC in the temperature variation and process corners are reported in Table 2. So that in process corners and temperature variation of the four amplifiers that operate in weak and strong inversion, the most variations of the input referred flicker noise is $0.25\mu\text{V}/\sqrt{\text{Hz}}$ @ 1Hz. In addition, the input referred flicker noise of the PRFC and PFC compared to the RFC and FC amplifiers respectively is lower in the five corners analysis. Moreover, to confirm the presented arguments in the weak inversion, the layout of the proposed amplifiers in weak inversion is shown in Fig. 6. According to this figure, the active area of PFC and PRFC amplifiers is $4056\mu\text{m}^2$. Finally, the output common mode voltage of designed amplifiers is set at $V_{DD}/2$ for maximize swing. In Table 3, the key parameters of the four amplifiers that operate in weak and strong inversion are compared.

Table 2. Important specifications of PRFC in the process corners and temperature variation.

PARAMETER	Corner analysis				Temperature dependent			
	Weak		Strong		Weak		Strong	
	SS	FF	SS	FF	-10°C	$+90^{\circ}\text{C}$	-10°C	$+90^{\circ}\text{C}$
Unit gain-bandwidth (MHz)	0.092	0.0103	83.5	95.6	0.09	0.0106	82.2	97.1
Phase margin ($^{\circ}$)	76.9	74.1	69.7	66.9	77.8	73.1	70.3	65.4
DC gain (dB)	64.9	60.3	65.7	60.8	60.1	64.9	60.9	66.5
Average slew-rate (V/ μs)	0.0582	0.0599	89.1	91.4	0.0577	0.0598	88.1	91.2
Input voltage noise @ 1Hz ($\mu\text{V}/\sqrt{\text{Hz}}$)	2.94	2.85	4.69	4.48	2.96	2.82	4.65	4.53

Table 3. Specifications of the simulated amplifiers in weak and strong inversion.

PARAMETER	Weak Inversion				Strong Inversion			
	FC	PFC	RFC	PRFC	FC	PFC	RFC	PRFC
Supply voltage (V)	0.6	0.6	0.6	0.6	1.8	1.8	1.8	1.8
Power dissipation (μW)	0.36	0.36	0.36	0.36	720	720	720	720
Capacitive load (pF)	12	12	12	12	4	4	4	4
GBW (MHz)	0.047	0.048	0.099	0.0995	39.15	42.12	90.62	89.01
Phase-margin (degree)	84.43	84.44	75.23	75.62	84.41	84.39	72.57	68.59
Output voltage swing (V)	0.4	0.4	0.4	0.4	1	0.9	1	0.9
DC gain (dB)	53.24	54.15	61.69	62.42	54.18	55.63	63.02	63.45
Input referred noise [1 Hz–100 kHz]	21.1	19.12	17.6	15.86	72.37	47.2	57.56	39.56

& 1Hz- 100MHz] (μVrms)								
Input voltage noise @ 1Hz ($\mu\text{V}/\sqrt{\text{Hz}}$)	3.88	3.59	3.13	2.89	7.21	5.59	5.71	4.57
Average slew rate ($\text{V}/\mu\text{s}$)	0.0224	0.0223	0.0591	0.0591	31.23	31.16	90.3	90.31
Area (μm^2)	4060	4060	4060	4060	2000	2000	2000	2000

5. CONCLUSION

A new procedure to design CMOS OTAs with enhanced noise performance in weak, moderate and strong inversion was presented. Based on this approach, the proposed RFC amplifier was simulated in $0.18\ \mu\text{m}$ CMOS technology, highlighting an input voltage noise @ 1Hz decrement of $31.1\ \text{pV}^2/\text{Hz}$ and $6.7\ \text{pV}^2/\text{Hz}$ compared to the conventional FC, without increasing the power consumption and silicon area in strong and weak inversion, respectively.

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