

# Plasma Behavior of SiC MOSFETs with Engineered Substrates during Reverse Recovery

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**Abstract**—The plasma density and distribution are crucial factors in optimizing the reverse recovery behavior of power semiconductor devices, particularly under conditions of high temperature and current density. This paper investigates the impact of hydrogen ion implantation during the manufacturing process of SiC engineered substrates on the reverse recovery performance of MOSFETs, comparing them to devices based on monocrystalline substrates. The results indicate a lower reverse recovery charge, faster plasma formation, and a reduced charge carrier lifetime in the engineered substrates. Electro-thermal simulations further support these findings by demonstrating a lower carrier density.

**Index Terms**—SiC MOSFET, SiC engineered substrate, body diode, reverse recovery, carrier lifetime, TCAD

## I. INTRODUCTION

The reverse recovery characteristics of silicon carbide (SiC) MOSFETs are critical for optimizing performance, particularly in achieving fast, efficient switching with minimal losses. During the reverse recovery phase, the depletion of stored charge accumulated during the dead time introduces additional losses, affecting both the active and complementary switches.

Various factors influence the reverse recovery charge, including minority carrier lifetime, operating temperature, and load current. As temperature increases, the ionization of p-doped regions and the prolonged carrier lifetime lead to higher plasma density. These effects negatively impact reverse recovery performance, resulting in increased switching losses, pronounced snappiness, and higher induced voltages.

Optimizing plasma behavior is essential to minimize losses and enhance efficiency and robustness. A proven method for

silicon PIN diodes involves local lifetime control through the introduction of recombination centers, which optimize plasma distribution. Recent studies suggest that this approach is also applicable to silicon carbide devices [1] [2], resulting in improved plasma distribution and a corresponding reduction in reverse recovery charge. However, this reduction is accompanied by an increase in the on-state voltage drop.

A recent study demonstrated a reduction in reverse recovery charge without impacting on-state voltage drop by using SiC engineered substrates based on SmartCut™ technology [3]. The implantation of hydrogen ions during the manufacturing process of bonded substrates, which is used to split the donor wafer, leads to the formation of point defects that reduce the effective carrier lifetime [5].

This study investigates plasma behavior as a function of current density, temperature, and dead time. A novel method for more accurate determination of carrier lifetime is proposed. Furthermore, electro-thermal simulations provide additional insights into the plasma behavior.

## II. DEVICE STRUCTURE AND METHODOLOGY

SiC MOSFETs with a voltage class of 1200 V and a trench structure were fabricated using a SiC engineered substrate based on SmartCut™ technology. This technology combines a thin, high-quality monocrystalline SiC layer with a thick, low-resistivity polycrystalline SiC carrier [4]. For comparison, reference SiC MOSFETs were fabricated on a monocrystalline substrate. Both types of SiC MOSFETs were processed under the same conditions, ensuring the same cell design, n-base region, and buffer layer. This enables the investigation of the substrate's impact on plasma behavior during reverse recovery.

The measured static C-V characteristics of the parasitic capacitances in the devices are shown in Fig.1. The capacitances

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demonstrate similar trends with respect to the applied drain-source voltage ( $V_{DS}$ ), indicating that the capacitive switching behavior remains comparable under similar conditions for both technologies.

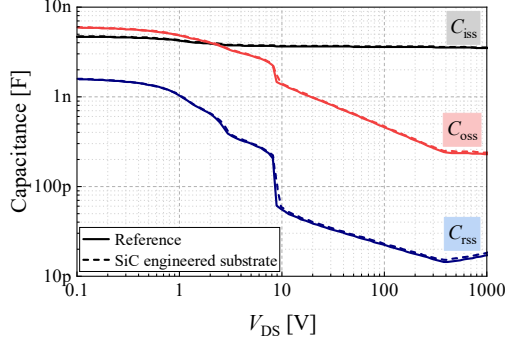


Fig. 1. Comparison of the measured C-V characteristic for both technologies.

The reverse recovery behavior of the body diode in the SiC MOSFET was investigated using a double-pulse setup. Both the high-side and low-side switches utilized the same type of MOSFET. The DC-link voltage ( $V_{DC}$ ) was adjusted to 800 V, and the gate-source voltage ( $V_{GS}$ ) was set to  $-10$  V to eliminate the influence of the n-channel during the dead time ( $t_{dead}$ ). A dead time of  $1 \mu s$  was selected to ensure complete plasma formation.

Measurements were conducted at current densities reaching up to three times the nominal value and temperatures up to  $200^\circ\text{C}$ . A coaxial shunt was used for current measurement, while voltage was measured using a passive probe connected to a separate oscilloscope. Fig. 2 shows the results obtained at maximum current density for both technologies.

The reverse recovery charge ( $Q_{RR}$ ) was determined according to JEDEC JEP201 standards (see Fig. 2). The determined  $Q_{RR}$  consists of capacitive stored charge ( $Q_C$ ) and stored charge from charge carriers ( $Q_{Plasma}$ ). The capacitive charge is derived from the device's output capacitance  $Q_{OSS}$ , determined by the  $C_{OSS}(V)$  curve (Fig. 1) and the applied  $V_{DC}$ . Additionally, the parasitic capacitance of the load inductance

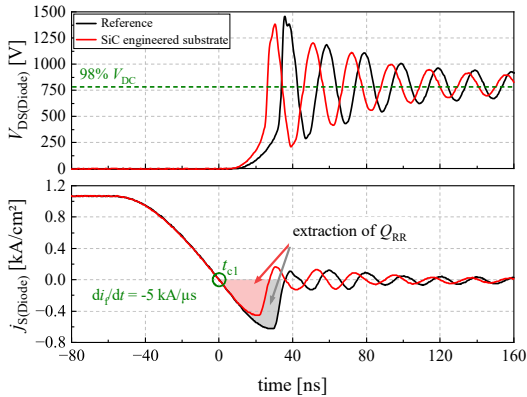


Fig. 2. Comparison of the reverse recovery behavior at  $V_{DS} = 800$  V,  $j_s = 1$  kA/cm<sup>2</sup>,  $V_{GS} = -10$  V,  $t_{dead} = 1 \mu s$ , and  $T_{vj} = 200^\circ\text{C}$ .

and the test circuit contributes further to  $Q_C$ . To accurately quantify  $Q_C$ , measurements were conducted during the initial pulse of the double-pulse test according to JEDEC JEP201 [6], ensuring no bipolar charge component in the absence of current. A  $Q_C$  of  $325$  nC was determined for the reference device and  $328$  nC for the SiC engineered substrate based device.

### III. EXPERIMENTAL RESULTS AND DISCUSSION

#### A. Plasma Stored Charge

The plasma stored charge was initially analyzed as a function of current density and temperature for both technologies. Fig. 3 illustrates the temperature dependence of  $Q_{Plasma}$ , corrected by the previously mentioned  $Q_C$ , at nominal and three times the nominal current density.

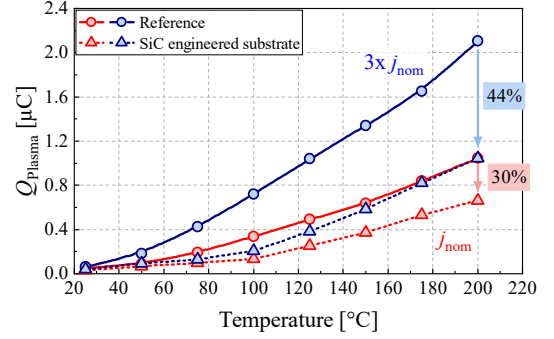


Fig. 3. Plasma stored charge ( $Q_{Plasma}$ ) as a function of temperature ( $T$ ) for different current densities ( $j$ ) at  $V_{DS} = 800$  V,  $V_{GS} = -10$  V, and  $t_{dead} = 1 \mu s$ .

In general,  $Q_{Plasma}$  increases with temperature due to the higher ionization degree of the p-doped regions and the enhanced effective carrier lifetime ( $\tau_{eff}$ ). However, the increase observed in the device based on the SiC engineered substrate is smaller, resulting in a lower  $Q_{Plasma}$  compared to the reference. This difference becomes more pronounced with increasing temperature and current density. Moreover, a significant increase in  $Q_{Plasma}$  for the SiC engineered substrate based device is only observed at temperatures above  $100^\circ\text{C}$ .

Since  $Q_{Plasma}$  is directly proportional to both current and effective carrier lifetime, the observed reduction in  $Q_{Plasma}$  for the SiC engineered substrate based device under identical test conditions can be attributed to a lower effective carrier lifetime.

#### B. Dead Time Dependency

A deeper understanding of the plasma formation process during forward recovery in both technologies can be gained by analyzing the relationship between the reverse recovery charge and the dead time. Fig. 4 shows the ratio of  $Q_{RR}$  to  $Q_C$  as a function of dead time at the nominal current density and at three times the nominal value, measured at a  $T_{vj}$  of  $200^\circ\text{C}$ .

Plasma formation occurs with a lower time constant for the SiC engineered substrate, referred to as the forward recovery time constant ( $\tau_{FR}$ ), compared to the reference device. At three times the nominal current,  $\tau_{FR}$  is reduced by 33% for the

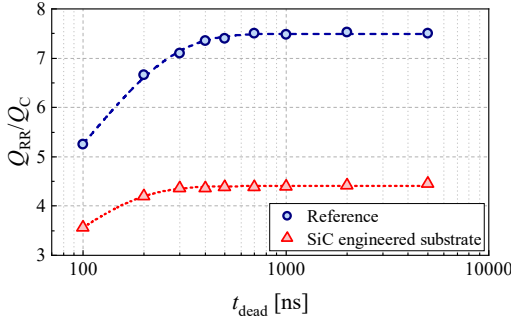


Fig. 4. Ratio of  $Q_{RR}$  to  $Q_C$  as a function of dead time ( $t_{dead}$ ) for different current densities at  $T_{vj} = 200^\circ\text{C}$ .

SiC engineered substrate based device, resulting in plasma saturation at shorter dead times. At nominal current density, the difference is less pronounced.

Plasma saturation during forward recovery is achieved only when an equilibrium between charge carrier generation and recombination is reached. This process is influenced by the carrier lifetime and emitter efficiency, with a shorter carrier lifetime leading to faster plasma saturation.

Hence, the faster plasma saturation observed in the SiC engineered substrate based device is primarily attributed to a lower carrier lifetime.

### C. Carrier Lifetime

The observed reduction in  $Q_{Plasma}$  and the faster plasma formation in the SiC engineered substrate based device compared to the reference device indicate a strong dependence on carrier lifetime. The effective carrier lifetime  $\tau_{eff}$ , determined from the relationship between  $Q_{Plasma}$  and load current, ranges from 10–15 ns for the reference device and 5–10 ns for the SiC engineered substrate based device, based on the measurements in Fig. 3. Thus,  $\tau_{eff}$  is lower for the SiC engineered substrate based device. However, this value is underestimated compared to the expected carrier lifetime in conduction mode due to surface recombination effects. Moreover,  $\tau_{eff}$  primarily reflects the carrier lifetime in the heavily doped emitter region, making it significantly shorter than the bulk carrier lifetime in the lightly doped region [7].

To propose an additional approach for evaluating the carrier lifetime, similar to the open-circuit voltage decay (OCVD) method, the behavior of  $V_{SD}$  is analyzed during the transition from bipolar to unipolar current conduction in the third quadrant, i.e., during plasma depletion. For this purpose, the device is continuously operated under a constant current (also to avoid di/dt effects influencing the measurement), while the gate voltage is switched between  $V_{GS} = 18\text{ V}$  (channel open - unipolar mode) and  $-10\text{ V}$  (channel closed - bipolar mode).

Fig. 5 shows the behavior of  $V_{SD}$  during the transition from bipolar to unipolar operation for both technologies at a temperature of  $150^\circ\text{C}$  and approximately the nominal current density. For the reference device, a slightly higher current density was required to achieve the same device temperature.

An exponential function was fitted to the voltage waveform to extract the charge decay time constant ( $\tau_{CD}$ ).

The SiC engineered substrate based device exhibits a faster charge decay, as indicated by a faster voltage rise, with  $\tau_{CD}$  being 40% smaller than that of the reference device. This aligns with a 37% decrease in  $Q_{Plasma}$  under comparable conditions (see Fig. 3). The reduced voltage drop in unipolar mode is attributed to the lower resistance of the highly doped poly-SiC layer [3].

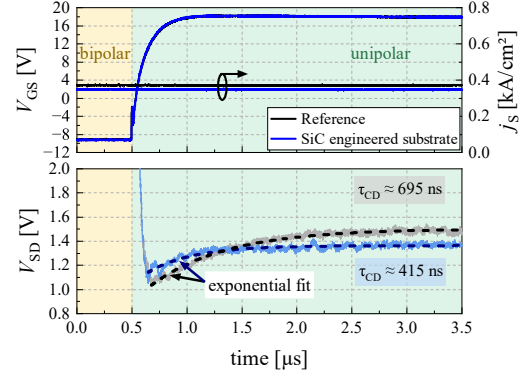


Fig. 5. Forward voltage drop during the transition from bipolar to unipolar third quadrant DC current conduction for both technologies at approx. nominal current density, with  $T_{vj} = 150^\circ\text{C}$ , and  $V_{GS} = +18\text{ V} / -10\text{ V}$ .

### D. Electro-Thermal Simulation Results

To analyze the plasma distribution within the device based on substrate technology and its impact on reverse recovery charge reduction, electro-thermal simulations were performed using *Synopsys TCAD* [8]. A half-cell 1200 V SiC MOSFET with a trench cell structure was utilized to reproduce the fundamental behavior. The substrate-specific characteristics were incorporated by introducing lifetime-killing traps in the bonded mono SiC layer and adjusting the doping density for the poly SiC layer as described in [3].

The reverse recovery behavior of both technologies was initially simulated at three times the nominal current density and a temperature of  $200^\circ\text{C}$ , using dead times of 100 ns and 1000 ns. As shown in Fig. 6, longer dead times result in higher reverse recovery current peaks and longer recovery times for both substrates, consistent with measurements. However, the total charge is lower in the SiC engineered substrate based device compared to the reference device, which aligns with experimental measurements (see Fig. 4).

Plasma formation in both substrate technologies was examined by analyzing electron and hole distribution at various time points within a  $1\text{ }\mu\text{s}$  dead time. As shown in Fig. 7, time point  $t_1$  marks the onset of bipolar current conduction.

At  $t_1$ , the SiC engineered substrate device exhibits a slightly higher electron density in the drift region compared to the reference, which is attributed to increased doping from the poly-SiC layer. This enhances electron injection and increases the initial hole density. After 50 ns ( $t_2$ ), the carrier density near the p-region become similar for both substrates. However, the

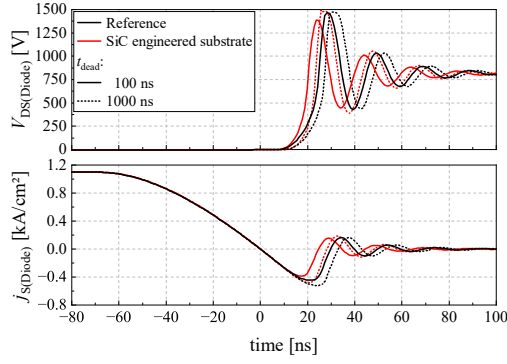


Fig. 6. Comparison of the simulated reverse recovery behavior at three times the nominal current density for different dead times at  $V_{DS} = 800$  V,  $V_{GS} = -10$  V, and  $T_j = 200^\circ\text{C}$ .

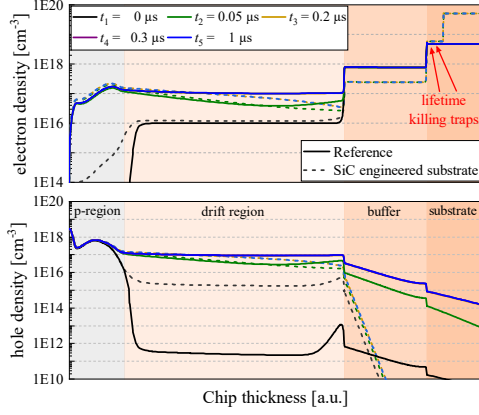


Fig. 7. Comparison of the electron and hole density for different time points at three times the nominal current density, with  $V_{GS} = -10$  V,  $T_j = 200^\circ\text{C}$ , and  $t_{dead} = 1 \mu\text{s}$ .

SiC engineered substrate device shows a lower carrier density toward the buffer due to the lifetime-killing effect, resulting in a reduced penetration depth. Hydrogen ion implantation into the mono-SiC layer, followed by annealing, increases the concentration of  $Z_{1/2}$  and other recombination centers, which reduce electron lifetime and limit carrier injection [5]. Consequently, the hole density decreases, particularly at the drift/buffer interface. During forward recovery, the electron and hole densities in the drift region continue to increase. Fig. 8 shows the hole distribution in the drift region at different time points for both technologies to improve visibility.

The hole concentration saturates earlier in the SiC engineered substrate based device compared to the reference. In the reference device, saturation occurs after 350 ns, whereas in the SiC engineered substrate based device, it occurs after 250 ns. This earlier saturation is attributed to the lower effective carrier lifetime and the lower emitter efficiency. These findings align well with the measurements shown in Fig. 4.

According to the trade-off between plasma density and voltage drop in bipolar devices, MOSFETs based on SiC engineered substrates are expected to exhibit a higher voltage drop in the third quadrant during bipolar operation due to the

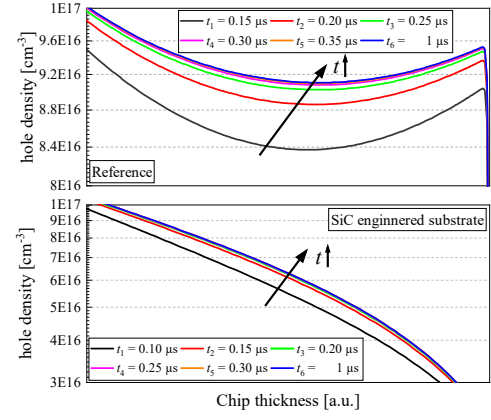


Fig. 8. Comparison of hole density in the drift region at three times the nominal current, with  $V_{GS} = -10$  V,  $T_j = 200^\circ\text{C}$ , and  $t_{dead} = 1 \mu\text{s}$ .

lower plasma density. Electrostatic potential analysis in Fig. 9 confirms this expectation in the drift region, buffer, and the initial micrometers of the substrate. However, the presence of a highly doped poly-SiC substrate compensates for the increased voltage drop in these regions. Consequently, the overall voltage drop  $V_{SD}$  is reduced from 3.55 V to 3.3 V at given conditions.

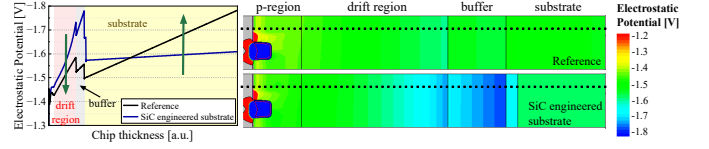


Fig. 9. Comparison of electrostatic potential at three times the nominal current, with  $T_j = 200^\circ\text{C}$ ,  $V_{GS} = -10$  V, and  $t_{dead} = 1 \mu\text{s}$ .

#### IV. CONCLUSION

The reverse recovery behavior and plasma formation of SiC MOSFETs fabricated on engineered substrates were investigated through measurements and electro-thermal TCAD simulations. Compared to SiC MOSFETs on monocrystalline substrates, these devices exhibit a significant reduction in plasma charge, which becomes more pronounced with increasing temperature and current density. Furthermore, the charge measurements as a function of dead time indicate a faster plasma formation behavior. The extracted carrier lifetime is lower and identified as one of the primary causes of this behavior. Electro-thermal simulations reveal a reduced carrier density, particularly at the interface between the drift region and the buffer.

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