

GA 21NRM02 - Digital-IT

D4 - Good practice guide for the calibration of digital substation instrumentation using PTPv2 timing

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List of Abbreviations

1PPS	One Pulse Per Second - A timing signal that marks each second for synchronization
4B/5B	4-Bit/5-Bit Encoding - Converts 4-bit data into 5-bit symbols for reliable transmission
API	Application Programming Interface - Enables software systems to communicate and share functions
BC	Boundary Clock – A networking switch which operates as a PTP master port for downstream devices
COTS	Commercial off the Shelf – easily available and replaceable hardware
DUC	Device Under Calibration - Equipment being tested for accuracy
EURAMET	European Association of National Metrology Institutes – Organization that develops and disseminates a measurement infrastructure for Europe
GM	Grandmaster - The primary time source in a PTP network
GPS	Global Positioning System - Satellite-based system for distributing location and precise time
IEC	International Electrotechnical Commission – A commission that develops global standards for electrical technologies
IEEE	Institute of Electrical and Electronics Engineers – An institute that sets standards and advances technology innovation
IT	Instrument Transformer – Converts high voltage and high current signals in the electricity grid to measurable values
LPIT	Low-Power Instrument Transformer - Measures electrical signals, either small-signal voltage output or digital SV stream output
MAC	Media Access Control - The layer of protocols and methods that manages how devices access a shared network medium, preventing data collisions and ensuring orderly communication
MII	Media Independent Interface – Interface that connects MAC interface chip and its host processor
MLT-3	Multi-Level Transmit-3 - Signal encoding using three voltage levels to reduce bandwidth
NRZI	Non-Return-to-Zero Inverted - Data encoding using signal transitions to represent bits
NTP	Network Time Protocol - Synchronizes clocks across computer networks
P2P	Peer-to-Peer – PTP delay method, where both link partners measure the link delay
PC	Personal Computer - General-purpose computing device for individual use
PHC	PTP Hardware Clock - Physical clock used for precise time sync in PTP systems
PTP	Precision Time Protocol - Synchronizes clocks in networks with high accuracy
PTPv2	Precision Time Protocol Version 2 - Enhanced version of PTP with better scalability and precision
REF	Reference device - Provides a stable standard for time or measurement calibration
RJ45	Registered Jack 45 - Standard connector for Ethernet cables
Rx	Receive - Process of accepting data or signals
SAMU	Stand-Alone Merging Unit - Digitizes signals from electrical equipment in substations
SFP	Small Form-factor Pluggable - Compact module for physical layer network interfaces
SOF	Start of Frame - Indicates the beginning of a data packet in communication protocols
SV	Sampled Value - Digitized measurements transmitted in real-time in electrical systems
TAP	Traffic Access Point - Allows monitoring or testing of network traffic

TC	Transparent Clock – A networking switch which forwards PTP messages while correcting for internal delay
TIC	Time Interval Counter - Measures time between two events with high precision
Tx	Transmit - Process of sending data or signals
UCA IUG	Utility Communications Architecture International Users Group - Promotes standards in utility communications
UTC	Coordinated Universal Time - Global time standard used for synchronization
UTP	Unshielded Twisted Pair - Common network cable type without shielding to reduce interference

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1 Summary

The EURAMET Digital-IT project set out to develop a traceable method for calibrating stand-alone merging units and digital output LPITs under IEEE 1588 Precision Time Protocol synchronicity. No such service was to date available from any national metrology institute globally. The problem has so far been the somewhat cross-disciplinary nature of the problem, the electricity grid metrologists are not timing experts, and time and frequency researchers mostly focus on time scales and frequency transfer. The grey area between the disciplines had so far been unexplored. But timing is becoming increasingly important in operating electricity grids and the need for calibrating PTP timing in the context of digital substations has become important

Three complementary methods were developed within the project duration. Two methods rely on determining the PTP clock time based on the traffic it sends and receives. A third method relies on a pair of similar clocks being used back-to-back, where either clock can operate as a master for its pair. The latter method was compared against one of the traffic monitoring methods and it was found that they agree within the uncertainty budgets. A goal for uncertainty was set to be in the 100-nanosecond range and all three methods succeeded in this. The goal was set an order of magnitude lower than what was foreseen as the absolute maximum tolerable uncertainty according to the requirements set in IEC 61869-13 standard. Besides calibration of master clocks, methodology for determining timing errors for other relevant equipment is presented based on one of the traffic monitoring methods.

As a “prenormative” project in the 2021 EURAMET project call, one of the outputs of Digital-IT is to develop best practices for industry and input to future amendment of relevant standards. This guide thus ends with a conclusions section including suggestions for developing standardization in testing equipment under PTP synchronicity. The findings indicated that a necessary step in traceable calibration is to isolate the test setup timing errors from the result. This can be achieved by a traceable calibration of the master clock and by ensuring a sufficiently low asymmetry in the physical transfer medium between the master clock and device under calibration.

2 Introduction

The digital substation environment in accordance with IEC 61850 family of standards is rapidly gaining in popularity in substations connecting parts of the transmission and distribution grids. Within a substation, the process bus is transmitting data to communicate specific events as Sampled Values (SV) streams of time domain measurements of grid signals in accordance with IEC 61850-9-2 [1]. Phase of the signals encoded into the SV streams is related to a local time source, often aligned with the coordinated universal time (UTC). A preferred time source in the IEC 61850-9-2 implementation guideline [2] for IEC 61850-9-2, the first, and widely accepted, document to suggest a conformal set of SV transmission parameters, is the one-pulse-per-second signal (1PPS) delivered via means of a dedicated optical or electrical connection.

The original standard IEC 61850-9-2 was first released in 2004 (superseded by the 2011 release and 2020 amendment), with the implementation guideline published in the same year. Since then, the IEEE 1588-2008 Precision Time Protocol (PTPv2) [3] has gradually been adopted as the preferred method for time synchronization. Originally an industry preference over 1PPS, PTPv2 is now considered as the primary means of time synchronization in IEC standard for digital interface for instrument transformers IEC 61869-9 [4]. The practical reasons for adopting PTPv2 are clear. It requires no additional cabling, since the already present process bus can be used for delivering the synchronization. And some applications, such as synchrophasors require absolute UTC time, which cannot be delivered using 1PPS.

While PTPv2 may have desirable properties for many applications on a digital substation, its use also significantly complicates the verification of the phase displacement performance of measurement instruments. While many national metrology institutes in the EU and worldwide have developed methods for calibrating merging units and other devices, which adopt 1PPS as a means of synchronicity, traceable methods for calibrating PTPv2 synchronized devices have not been proposed yet. Two major complications for calibrating a PTPv2 device clock can be readily identified. First, the timing information is embedded into a reasonably complicated exchange of messages between a master clock and a slave clock. And second, a slave clock's timing is unique, meaning that no two devices can be expected to have the same concept of time even if they receive their synchronicity from the same master clock. The latter property means that the classical approach of a reference measurement is not valid anymore.

One of the goals of the EURAMET 21NRM02 project "Metrology for digital substation instrumentation" was to develop methodology for calibration of merging unit phase displacement under PTPv2 synchronicity. The consortium consists of experts from both smart grids and time and frequency communities as an answer to the cross-disciplinary nature of the problem. The planned output from the project in this regard was to communicate the findings and developed methods to relevant standardization bodies, especially but not limited to IEC TC 38. This good practice guide serves as the means to this end.

3 Requirements for synchronicity

The most stringent timing requirements for a phase measurement referred to an absolute time source come from the measurement class stand-alone merging unit (SAMU) specifications, which are defined in the IEC 61869-13 standard. To support connecting the most accurate class 0.1 and 0.2S instrument transformers and LPITs to the process bus, an accuracy class 0.05 for SAMU is introduced. A maximum tolerated phase error for the class for both current and voltage is 2.5 minutes, which corresponds to a timing error of 2.3 microseconds if no other error sources exist.

When calibrating devices, it is often desirable for the reference setup to have an uncertainty an order of magnitude smaller than what is the desired final uncertainty of calibration. This means that the requirement for timing accuracy provided for the calibrated device should be as low as 230 nanoseconds or even lower if the uncertainty budget contains other sources with significant magnitude. Furthermore, devices (often test bridges) for calibrating SAMUs and instrument transformers under 1PPS synchronicity are already on the market and it is expected that such devices will soon support also PTP synchronicity. This introduces even more stringent requirements for synchronicity. Since the traceability chain is an additional step longer, the uncertainty in a test bridge calibration should be low enough to enable its use for calibrating class 0.05 SAMUs. For these reasons, *the goal for uncertainty in PTP time synchronicity calibration was set as low as 100 nanoseconds in the Digital-IT project.*

4 Traceability for PTPv2 on a digital substation

A drawing illustrating the principle of traceable phase displacement calibration is shown in Figure 1. A time source is introduced, which provides both 1PPS and PTP timing referenced to its timing plane. A physical link is established between the time source and both the device under calibration (DUC) and the reference measurement setup. The link may introduce errors if not implemented and calibrated correctly.

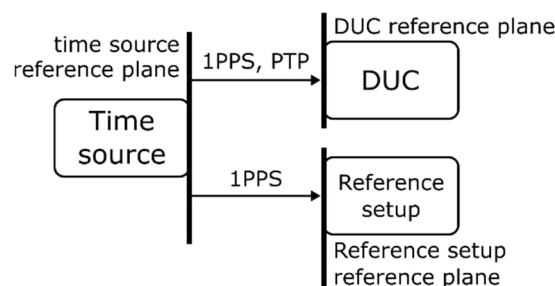


Figure 1. Principle of time synchronicity when using 1PPS and PTP in a calibration setup

In the case of 1PPS synchronicity, the time source reference plane may be considered common for both the device under calibration and the reference setup. In this case, the timing difference introduced by different lengths of 1PPS signal should be accounted for if different length cables are used. In a correctly working PTP master-to-slave link, the delay is compensated by the delay mechanism. Therefore, it is important that the time source, i.e. the master clock delay mechanism is implemented correctly, and the physical link introduces no additional error. The former can be guaranteed by calibrating the master clock with any preferred method and the latter by guaranteeing sufficient symmetry in the PTP transport path. If both requirements are satisfied, any error introduced between the master and slave clocks is due to the slave clock, the DUC in this case. Additionally, the master clock's internal time may be different from a 1PPS rising edge, even if supplied by the master itself. Thus, the internal time must be known with respect to any preferred timing reference plane. When the master clock's delay mechanism and internal time are calibrated, and the PTP transport path has no appreciable symmetry, timing related error to DUC SV data phase displacement is due to the DUC only and may be calibrated.

To address master clock calibration, three complementary methods have been developed within the Digital-IT project. VTT have developed a method, which can be used for determining the error of the time stamps generated by a PTP clock and deriving clock inaccuracies from the results. The method is based on probing on-the-wire Layer 1 signals between two clocks in a master to slave communication link. The method

presented in detail in section 0 is called the *absolute calibration method*. RISE have developed a similar approach, relying on Linux APIs, which support PTP hardware clocks (PHC) on Ethernet interfaces, and both allow time stamping of Ethernet frames as well as external events of 1PPS representations of a traceable timescale. RISE's method is described in detail in section 0. In VSL's method two PTP clocks in the master-slave hierarchy are taken as a pair of PTP clocks for calibration, and the calibration is done by setting up a PTP communication path between the PTP clocks pair accordingly. By assessing relevant PTP parameters in the link as well as the phase comparison on the 1PPS signals, total internal latencies and relative PTP time offset of the two PTP clocks in pair are calibrated. VSL's approach is called the *relative calibration method* and is described in section 7. A comparison of the absolute and relative methods is presented in section 0.

5 Relevant aspects of PTPv2

Shortly after the release of the 2008 version of the precision time protocol, IEEE Power and Energy Society released a standardized set of rules in IEEE C37.238-2011 [5] for using PTPv2 for synchronizing devices. This document is commonly known as the "Power profile" for PTPv2. A common set of rules for implementing PTPv2 and the mandatory requirement for its support in IEC TC 38 release of IEC 61869-9 [4], which standardized the sampled values output of IEDs for various applications meant that the precision time protocol became the primary means for time synchronization. The IEEE Power Profile further evolved into a dual logo release of the IEC/IEEE 61850-9-3:2016 known as the "Utility Profile" and to specific requirements for the North American market defined in IEEE C37.238-2017 [6], [7], [8].

What is most important in the standard profiles for this work are the definitions of some key aspects of using PTPv2 on a substation. While the method developed at VSL is not dependent on the specifics of a PTP setup, certain aspects are leveraged in other solutions developed in the Digital-IT project. Most importantly, the following specifications are of significance:

1. **Switches are allowed to be configured as either transparent or boundary clocks.** While both types have their pros and cons, a boundary clock is preferred in a calibration setup. Using a boundary clock greatly simplifies the Sync mechanism messages delivered to a slave-only device, since no residence time correction is required and a high level of Rx/Tx path symmetry between the slave and master ports can be guaranteed.
2. **One-step and two-step devices are allowed.** Two-step clocks are often preferred, since its use simplifies the process updating relevant fields in the PTP messages used in sync and delay mechanisms.
3. **Peer delay mechanism for path delay measurement is the only allowed method.** The associated *Pdelay_Req*, *Pdelay_Resp*, and *Pdelay_Resp_Follow_Up* messages available from both link partners carry all the necessary information to assess all critical parameters of the PTP ports. Furthermore, when using two-step devices, the rules state that *requestReceiptTimestamp* and *responseOriginTimestamp* fields should be populated in the respective response messages. This makes calculating the ingress and egress timestamp errors straightforward.
4. **Layer 2 transport with a predefined Ethertype field.** Locating and decoding PTP traffic on the wire is simpler, when the messages can be identified as PTPv2 traffic based on the *EtherType* field in the Layer 2 frame. In Layer 3 traffic the *EtherType* field would be used for indicating transmission of IPv4 packets.

6 Absolute calibration method

6.1 Setup and rationale

VTT's setup for calibrating devices, which produce sampled values data and rely in PTPv2 for time synchronicity is shown in Figure 2. The figure shows relevant devices, which deliver synchronicity between the devices. The Grandmaster (GM) clock is synchronized using GPS and along with PTPv2 sync, has also an output for a 1PPS signal used by the reference device (REF). The boundary clock, which is synchronized by the Grandmaster in turn synchronizes its downstream slave clock, the device under calibration (DUC). The GM and the boundary clock switch are set up in accordance with the Utility Profile. The SV data produced by the devices is transferred to a PC (not drawn) through the same switch. Voltage and current test signal connections are omitted in the figure for simplicity. In this regard, the setup works as any other setup for comparing readings from a device under calibration to a calibrated reference device: the same signals are measured by both devices.

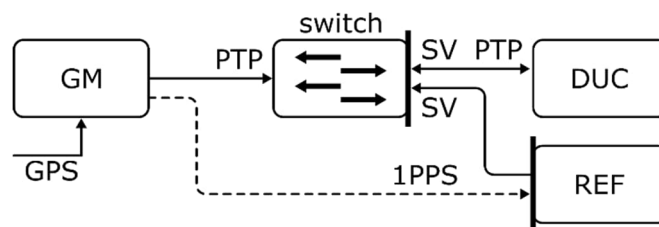


Figure 2. Timing and data connections of the measurement setup for calibrating devices that produce SV data.

In Figure 2 the thick lines show the definition of timing reference planes of the relevant devices in the setup. For the device under calibration, this is the boundary between the upstream master clock and the network, i.e. the physical network connector. For the reference device, the timing reference plane is the 1PPS input connector, against which its phase displacement is calibrated. To calibrate the phase displacement of the device under calibration, one needs to know what the difference in the synchronicity received by both devices is. The rationale for defining this is that the error of the DUC upstream master clock (the boundary clock switch) must be known so that it can be accounted for. This includes determining the internal time of the master clock as well as its ingress/egress asymmetry. Additionally, the network cabling between the switch and the DUC must not introduce additional asymmetry. Any phase displacement in slave device SV stream can then be attributed to the slave only, while the upstream master port error can be accounted for in the result.

6.2 PTP event message timing and clock models

The error of a PTP clock can be quantified by determining how its internal time stamping is performing with respect to the delays it needs to compensate for. Looking into the original PTPv2 standard IEEE 1588-2008 [3], three clauses are of significance:

Clause 6.6.5 Generation of message timestamps: *A timestamp event is generated at the time of transmission and reception of any event message. The timestamp event occurs when the message's timestamp point crosses the boundary between the node and the network.*

Therefore, determining the time of transmission or reception of messages with respect to an external time reference plane and the time the PTPv2 instance claims as the transmission or reception time, enables determining the time stamping error¹ with respect to the timing reference plane.

Clause 7.3.4.1 Event message timestamp point: *Unless otherwise specified in a transport-specific annex to this standard, the message timestamp point for an event message shall be the beginning of the first symbol after the Start of Frame (SOF) delimiter.*

This means that the timestamp point in the PTPv2 messages is the first bit of the destination MAC address at the beginning of a Layer 2 frame. Figure 3 illustrates this location in a 100Base-X ethernet connection, where

¹ Since the reference plane is somewhat arbitrarily defined as the reference device 1PPS input, the use of “difference” instead of “error” of any PTPv2 time stamp would be more appropriate.

the frame is shown in detail for the relevant part. The timestamp location Δt_{TS} is at all times determined with respect to the 1PPS signal at a suitable time reference plane. The last two 4B/5B symbols “AA” of the preamble are followed by the SOF delimiter “AB”, which is then followed by the timestamp point at the beginning of the frame. The NRZI line coding of the symbols is shown for the sake of detail. The 5-bit symbols are defined by either a transition (one) or no transition (zero). It is possible that the NRZI code has no transition at the timestamp location, which means that the exact symbol time must be determined based on the preceding “B” symbol in the SOF delimiter.

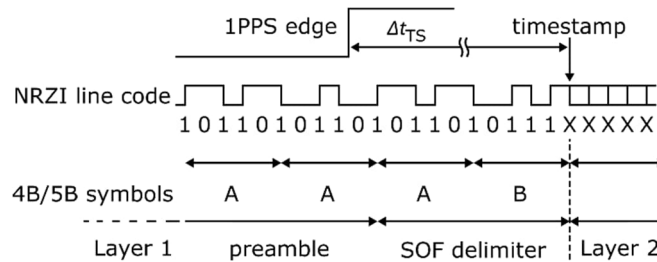


Figure 3. Timestamp point at the beginning of a Layer 2 frame in a 100Base-X ethernet connection

Finally, regarding the generation of timestamps, the standard defines the time instance when this needs to be performed by a clock:

Clause 7.3.4.2 Event timestamp generation: *All PTP event messages are timestamped on egress and ingress. The timestamp shall be the time at which the event message timestamp point passes the reference plane marking the boundary between the PTP node and the network.*

The clause is followed by a note further specifying that a clock should compensate for any time difference between the event message timestamp point passing the reference plane and the time the clock measures and claims to represent said time:

NOTE 1— *If an implementation generates event message timestamps using a point other than the message timestamp point, then the generated timestamps should be appropriately corrected by the time interval between the actual time of detection and the time the message timestamp point passed the reference plane. Failure to make these corrections results in a time offset between the slave and master clocks.*

It is therefore necessary for a device to compensate for this error by adjusting the event message timing according to any delay present in the ingress and egress paths in the implementation. This is illustrated in detail in Figure 4. A clock model is drawn with ingress and egress path delays, with event messages passing the timing reference plane at instances t_i (ingress) and t_e (egress). The clock measures the values t'_i and t'_e at the internal timestamping point. The difference between t_i and t'_i , and t_e and t'_e are respectively called ingress and egress latencies, and are likely to be different, as drawn in the figure. According to the IEEE 1588 standard, the latencies need to be corrected for by using the following formulas.

$$t_e = t'_e + \text{egress latency}$$

$$t_i = t'_i - \text{ingress latency}$$

Any error in compensating for the ingress and egress path errors correctly in either the master or slave clock results in offset error and link asymmetry and will lead to a time difference between the two clocks, and consequently in a time shift of the slave clock with respect to any external timing reference plane.

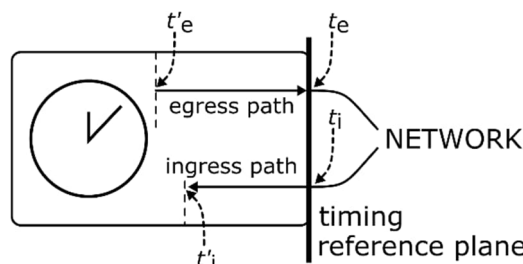


Figure 4. A PTP clock model including ingress and egress paths.

For the setup drawn into Figure 2, one needs to know the boundary clock properties to account for them in determining the time t_m available to the slave device (DUC). This includes determining the internal time of the clock master port, as it may be affected by its own upstream master clock, i.e. the Grandmaster clock in the setup. And additionally, its residual asymmetry, the part of ingress and egress delay asymmetry, which has not been compensated for is required. To quantify the master port for these properties, a more detailed model is drawn in Figure 5.

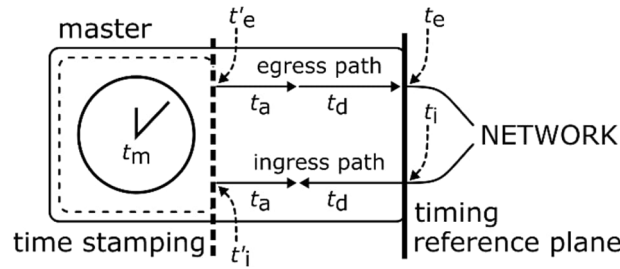


Figure 5. A PTP clock model with ingress and egress paths defined by constant and asymmetry parts.

The ingress and egress latencies are now given by a constant part t_d , which is equal but with opposing signs, and the asymmetry part t_a . The asymmetry is defined as positive w.r.t. the master egress path and negative w.r.t. the master ingress path as in clause 7.4.2 of IEEE 1588-2008 for the link transmission path. Master clock internal time t_m affects internal time stamping values t_i' and t_e' . Time at the timing reference plane is given by

$$\begin{cases} t_e = t_e' + t_a + t_d \\ t_i = t_i' + t_a - t_d \end{cases}$$

Solving for constant and asymmetry parts t_d and t_a yields

$$t_d = \frac{(t_e - t_e') + (t_i - t_i')}{2} \quad \text{and} \quad t_a = \frac{(t_e - t_e') - (t_i - t_i')}{2}$$

The constant part t_d ($=t_m$, since any additional error will be accounted for in t_a), as defined in Figure 5 and calculated above, is influenced by several delays in the timing chain. First, the upstream Grandmaster clock may have an error of its own, and the quality of the link to the boundary clock will cause an additional error. And second, the boundary clock master port may add to the error. From the measurement, it is impossible to distinguish between these error sources. The data in section 6.5 shows that a Grandmaster, which also provides the 1PPS signal may in fact have the largest effect on the error. The asymmetry part t_a is not influenced by an arbitrary choice of timing reference, such as the reference device 1PPS input, since any additional delay in t_i and t_e will simply cancel out. It is therefore a property of the clock under calibration only.

Only the sum of various error sources in t_d together with the residual asymmetry t_a is needed to calibrate the boundary clock master port time with respect to 1PPS. Following the signs in Figure 5 and in clause 7.4.2 of IEEE 1588-2008, the time delivered to a downstream slave clock by the master port in the boundary clock is given by

$$t_m' = t_m + t_a,$$

implying that a positive residual asymmetry will add to the constant part t_d , while a negative one will reduce it. The effect of master port time can then be removed from the phase displacement measurement $\varepsilon'_{\varphi, DUC}$ at a test signal frequency f , resulting in a calibrated value of

$$\varepsilon_{\varphi, DUC} = \varepsilon'_{\varphi, DUC} - 2\pi f t_m'.$$

Example: A PTP master port in a boundary clock providing reference time to a SAMU is offset by $t_m' = +100$ ns. This means that the SAMU (excluding any error of its own) will time tag samples 100 ns too early, causing a leading (positive) phase in its SV stream. Assuming a system frequency of 50 Hz, the phase lead due to the master port may be removed by subtracting the corresponding value of 31.4 μ rad (1.8 mdeg) from the measured phase displacement.

6.3 Leveraging the Peer Delay mechanism

The IEC 61850-9-3 utility profile uses only the peer delay mechanism delay measurement as stated in part 6 of the standard. The peer delay mechanism measures link delays between link partners only, as opposed to the end-to-end mechanism, which measures delays from slaves clocks all the way to master clocks. A sufficient amount of information is available from the message transfer between a slave clock and its upstream boundary clock master port. Figure 6 shows the slave-initiated peer delay measurement.

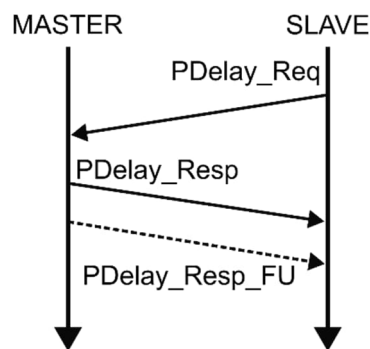


Figure 6. Transfer of messages in a peer delay measurement

The slave device first sends a *PDelay_Req* message, which is time-tagged by it and the master clock respectively at egress and ingress. The message enters the master port at ingress time t_i , and the master reports its ingress time measurement t'_i in the *PDelay_Resp* message. Thus, all information for calculating the ingress time error of the master port is available. The master also measures the egress time t'_e for the *PDelay_Resp* message, which is then communicated in the *PDelay_Resp_Follow_Up*. Since now both t_e and t'_e are known, the egress time error can be determined. All information for calculating master clock time and asymmetry is therefore available. Determining slave clock time for the link is also possible, since the peer delay mechanism explicitly defines that both link partners should do the measurement and keep a record of the result. In this case, the master-initiated message transfer is used.

6.4 Hardware and software

Timestamps are encoded into the payload data of the messages or defined as the time instance a single bit crosses the timing reference plane. In order to get all the required information, a method to simultaneously determine the internal time stamp values t_i and t_e , and time instances t'_i and t'_e when the messages pass the reference plane is developed. This is done by capturing both the Rx and Tx path Layer 1 signals together with 1PPS using a digitizer.

Measuring the physical layer signals is done by inserting a traffic access point (TAP) in the link between the two clocks. Separate TAPs are designed for 100Base-RX (copper, twisted pair) and 100Base-FX (fiber) links. The signals are output through coaxial connectors into the digitizer, which captures a sufficiently long record of the physical layer signals. Photographs of the capture devices are shown in Figure 7 (a) and (b). The copper tap consists of two RJ45 connectors at the back. The Rx and Tx signals are tapped in between the connectors and routed to the output BNCs through a signal transformer to maintain a galvanically isolated transmission path. The optical tap uses separate SFP modules for tapping Rx and Tx signal paths. The SFP modules are connected in a loopback setup, where the receiver electrical output is connected to the transmitter input. The loopback point is also connected to output SMAs through an attenuator and a limiting amplifier.



Figure 7. Traffic access points for 100Base-TX (a) and 100Base-FX (b) links.

The calibration setup consists of several cables or optical fibers, which either connect the clocks together or the physical layer signals to the digitizer. All connections introduce delays, which need to be determined and accounted for in order to measure message ingress and egress times correctly. Figure 8 shows the same setup as in Figure 2 including the TAP and the digitizer, and with all relevant cable and fiber delays given. The digitizer is locked to an external 10 MHz frequency standard and is triggered by the rising edge of the 1PPS signal in one of the input channels. The Grandmaster clock supplying the 1PPS signal is not drawn. Some assumptions are required to be made concerning the asymmetries and a simplified model for the TAPs is used. A separate device is used for driving fast 1PPS edges into the digitizer and reference device. TAP device internal delays are drawn in more detail in Figure 9 (a) and (b). Both devices are dual channel, so they connect Rx and Tx signals to the output coaxial connectors. Only a single channel is drawn.

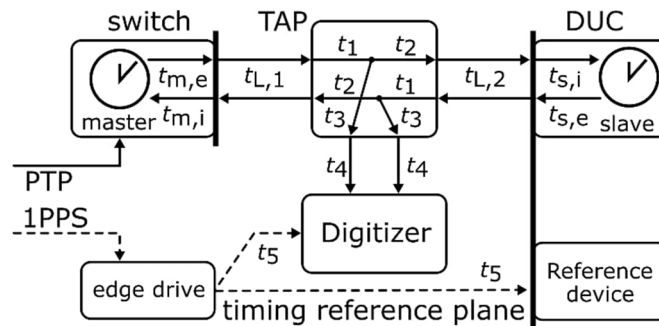


Figure 8. Measurement setup for determining the clock errors including relevant delays introduced by cables and fibers.

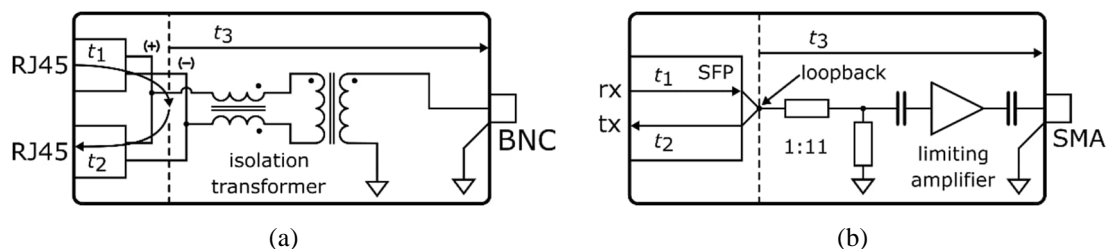


Figure 9. Traffic access point schematics and internal delays for 100Base-TX (a) and 100Base-FX (b) links.

The sources of various delays are given in. The links between the clocks are assumed to have no asymmetry due to the use of very short physical media connections in the order of some meters. The reference device 1PPS timing is assumed to be the same as the time of 1PPS measured by the digitizer due to use of equal length cables. The digitizer is verified to add no significant error through timing difference between the channels.

Table 1. Source of delays introduced by cables in the calibration setup.

Property	Source of delay
$t_{L,1}$	Link delay from master port to TAP, no asymmetry
$t_{L,2}$	Link delay from TAP to slave clock, no asymmetry
t_1	TAP delay from network connector input to tapping point
t_2	TAP delay from tapping point to network connection output
t_3	TAP delay from tapping point to output coaxial connector
t_4	cable or probe delay from TAP coaxial output to digitizer
t_5	delay from 1PPS drive to digitizer and reference device 1PPS input

After determining the delays, time instances t_i and t_e with respect to the 1PPS at the reference device input for the master port can be calculated based on the following formulas:

$$t_i = t_{i,d} + t_{L,1} + t_1 - t_3 - t_4$$

and

$$t_e = t_{e,d} - t_{L,1} - t_1 - t_3 - t_4,$$

where $t_{i,d}$ and $t_{e,d}$ are the SOF delimiter delays of suitable PTP messages from the 1PPS edge in data captured by the digitizer. 1PPS cable delays (t_5) cancel out, since equal length cables can be used.

The 125 Mbit/s NRZI/MLT-3 data in the 100Base-X connection is captured using an oversampling rate of 10, resulting in a sample rate of 625 MHz. Layer 1 signals in a 100Base-X link are generated by running MII data from a host processor through several different layers of encoding. This is mostly done for adding sufficient transitions into the NRZI signal to ensure a reliable clock recovery at the receiving end and in the case of 100Base-TX to also improve electromagnetic compatibility. In order to access the SOF timing and the message payload, the signals need to go through decoding. The flowchart for decoding is shown in Figure 10.

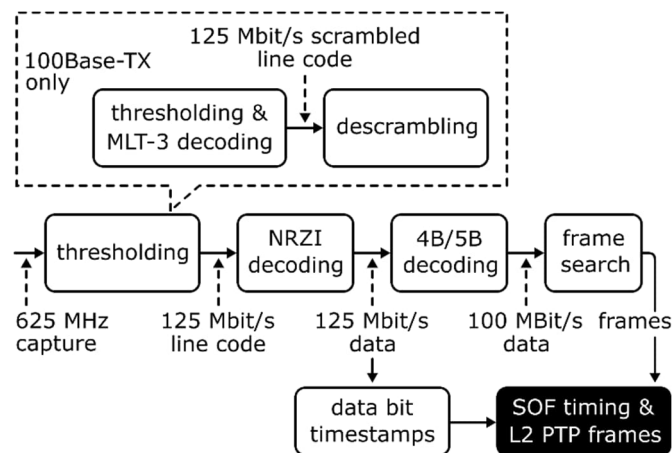


Figure 10. Decoding flowchart for 100Base-X physical layer signals.

The 625 MHz capture is first thresholded and downsampled to a 125 Mbit/s NRZI line code. A 100Base-TX signal needs MLT-3 decoding together with the thresholding, after which the NRZI line code goes through descrambling. The (descrambled) NRZI line code is decoded into 125 Mbit/s bits of 4B/5B encoded data and time stamps are generated for the bits in the encoded data. After 4B/5B decoding, Layer 2 frames are found based on locating the message preambles in the Layer 1 signal, and timestamp timing for all frames is calculated based on SOF delimiter locations. The payload of Layer 2 data is identified as a PTP message when the *EtherType* field carries the value 0x88F7. All decoding is done in python. A python package called *scapy* [9] is used for parsing the binary representation of decoded frames as various PTP messages with all fields decoded as appropriate data types.

6.5 Measurement results from VTT's digital substation calibration setup

The absolute calibration method was used for testing and calibrating various components in VTT's digital substation calibration setup. While calibration of the switch in Figure 11 is certainly the most important task, other interesting tests are also possible. A list of conducted calibrations and tests and their relevance is as follows.

1. **Calibration of the boundary clock switch master port internal time and residual asymmetry.** Calibrating the upstream master port is necessary to isolate the master's effect on the slave clock's timing error, and therefore on its phase displacement. A perfectly symmetrical link between master and slave is assumed.
2. **Test of DUC internal time.** The peer delay mechanism message transfer, when initiated by the master, may be used for determining the internal time of the PTPv2 slave clock instance running inside the DUC.
3. **Grandmaster error vs. its own 1PPS output.** Since the switch internal time is affected by its upstream master, it's interesting to quantify also the error of the Grandmaster clock.
4. **DUC phase displacement calibration under PTPv2 synchronicity.** With traceability for PTP time established, it's possible to calibrate a SAMU for its phase displacement.
5. **Introduction of errors in PTPv2 synchronicity.** Artificial errors in PTPv2 synchronicity should result in predetermined errors in DUC synchronicity. This may be tested by concurrently reading the DUC internal time and observing the phase displacement in its SV data output.

Calibration of the boundary clock switch master port and reading DUC internal time

Figure 11 shows the setup for determining master and slave clock time and residual asymmetry. Master port time in the switch is compared to reference device 1PPS input. Additional edge drive for 1PPS is used for generating fast edges to reduce timing uncertainty. Both the switch synchronicity and 1PPS is sourced from an external Grandmaster, which is not drawn. A 100Base-FX fiber link together with the probe in Figure 7 (b) is used for accessing traffic between the two clocks.

Table 2 shows the ingress and egress path errors for both clocks as well as the internal time and residual asymmetry calculated from the timing errors. The standard deviation of the measurement data is given as positive/negative tolerance for the measured timing errors.

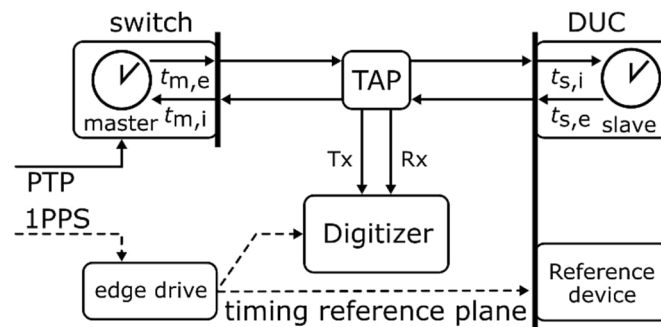


Figure 11. Measurement setup for calibrating a boundary clock's master port and slave clock's internal time and residual asymmetry.

Table 2. Clock egress and ingress errors, internal times, and residual asymmetries.

Property	Master (switch)	Slave (DUC)
Egress error	$(96.2 \pm 1.7) \text{ ns}$	$(-11.5 \pm 0.1) \mu\text{s}$
Ingress error	$(97.7 \pm 3.8) \text{ ns}$	$(11.6 \pm 0.2) \mu\text{s}$
Internal time vs. 1PPS	$(97.0 \pm 4.2) \text{ ns}$	$(48 \pm 228) \text{ ns}$
Residual asymmetry	$(-0.7 \pm 4.2) \text{ ns}$	$(-11.5 \pm 0.2) \mu\text{s}$

The data in Table 2 shows that the switch master port internal error is quite high, although it's only one hop away from the grandmaster, which supplies also the 1PPS signal. Slave clock time reflects this, although uncertainty is quite high due to large deviation² between individual measurements.

Grandmaster error vs. its own 1PPS output

Master port error may be further investigated by measuring the time inside its upstream master. The setup to do this is shown in Figure 12. The switch slave port is synchronized by the Grandmaster clock in the setup. The clocks are connected using a 100Base-TX link. A passive probe in Figure 7 (a) is connected between the devices and data is analyzed. Unfortunately, the Rx traffic into the Grandmaster is impossible to decode from the digitizer capture due to excessive ringing and the MLT-3 encoded signal settling at constantly varying levels between 1's in the data. Thus, Grandmaster internal time and asymmetry are not possible to be measured. However, egress error of the Grandmaster is available and can be determined from the *Sync* and *Follow_Up* message pair. Time instance t_e is the *Sync* message SOF delimiter egress time and t_e' is the *preciseOriginTimestamp* in the *Follow_Up* message. Figure 13 shows the egress error data collected in the measurement. Interestingly, a quantization of 10 ns for *Sync* message egress time can be observed in the data. The 1.6 ns quantization in error values is due to sampling frequency of 625 MHz in the digitizer used for capturing the physical layer signals. While not exactly comparable to the previous measurement of the switch master port internal time, the Grandmaster egress error of $(97.9 \pm 0.8) \text{ ns}$ appears to account for most of the time error in the upstream devices.

² The likely cause for this is a software-only implementation of PTP in the slave, with no hardware-assisted timestamping. In this case, any variable delay in servicing interrupts will cause jitter in time stamping PTP event message egress and ingress times.

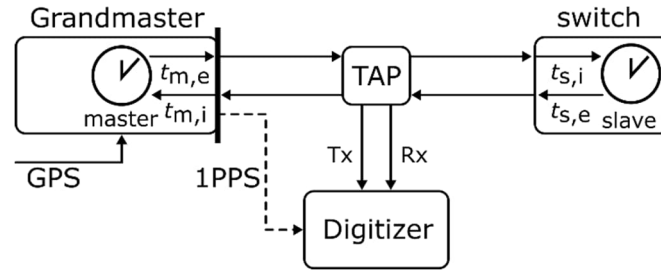


Figure 12. Measurement setup for testing grandmaster's timing error against its own 1PPS output.

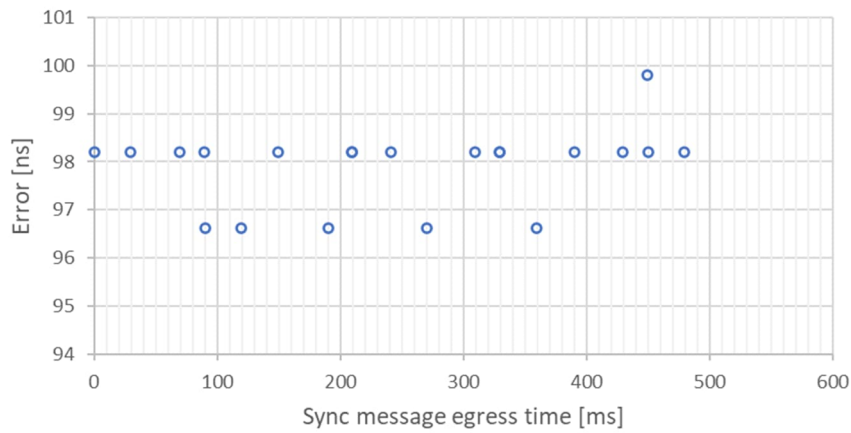


Figure 13. Grandmaster egress error vs. 1PPS against Sync message egress time.

DUC phase displacement calibration under PTPv2 synchronicity

After calibrating the upstream master port in Figure 12, it's error may be subtracted from the calibration result. The DUC was calibrated using an SV data rate of 4000 Hz using the setup in Figure 2. As per the example in section 6.2 on page 9, the master clock error t_m is compensated by subtracting its influence from the reading $\varepsilon'_{\phi, DUC}$ using the formula

$$\varepsilon_{\phi, DUC} = \varepsilon'_{\phi, DUC} - 2\pi f t_m$$

where $\varepsilon_{\phi, DUC}$ is the corrected calibration result and f is the calibration frequency.

The phase calibration results, including various uncertainty contributions are given in Table 3. It can be seen that for the smallest uncertainties, the PTP vs. 1PPS calibration uncertainty becomes a clear contributor to the overall calibration uncertainty. The roughly 100 ns error in switch master port time in VTT's setup becomes a relevant factor when trying to achieve the best possible uncertainty. An error of 100 ns would result in an error of 1.8 mdeg, which is almost the same as the lowest achieved uncertainty, when using input values of 1 A, 5 V, and 100 V. *This underlines the need for calibrating the timing network prior to calibrating merging units or other SV enabled equipment.*

Table 3. Calibration result of a Stand-alone merging unit using VTT's calibration setup.

Test conditions	Error of input [mdeg]				Uncertainty contributors [mdeg]			Uncertainty
Current inputs	IA	IB	IC	IN	Deviation	PTP v. 1PPS	Setup	[mdeg] $k = 2$
1 A, 50 Hz	70	73	45	62	1.1	0.3	0.3	2
0.05 A, 50 Hz	73	71	49	95	10	0.3	0.3	21
0.025 A, 50 Hz	88	137	99	-4	36	0.3	0.3	72
Voltage inputs	VA	VB	VC	VN				
100 V, 50 Hz	10.9	17.7	21.9	20.1	0.3	0.3	0.2	1.0
5 V, 50 Hz	8	15	19	17	0.9	0.3	0.2	2

The timing network influence may be further investigated by introducing an artificial error to the time the DUC receives. One way to achieve this is to add asymmetry in the link between the upstream PTP master clock and the DUC. This is shown in Figure 14, where additional fiber is added either in the master clock egress or ingress path. Using the definitions in Figure 5, the sign of the resulting asymmetry is positive when the extra fiber is added to the master egress (Tx) port. A positive asymmetry is drawn as a red fiber spool in the Figure 14 and a negative one as a blue spool. The SV stream of the DUC is recorded and phase displacement of one of the current signals is calculated for each asymmetry configuration. The measured input signal in the test is phase locked to 1PPS and no reference measurement is performed. Thus, the phase displacement result is the observed difference from the no-asymmetry condition. The measurement results are given in Table 4. The uncertainties are mostly dominated by deviation of readings.

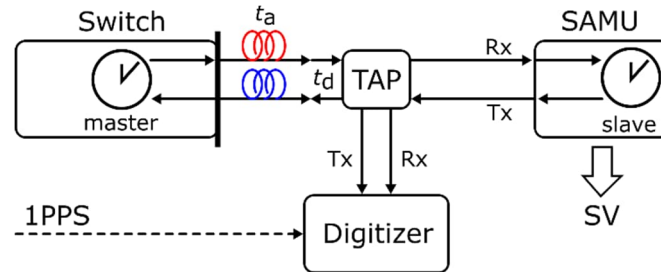


Figure 14. Introducing errors by adding asymmetries in the timing network

Table 4. Measured values of DUC slave clock time and relative phase displacement vs. link asymmetry.

Asymmetry [ns]	DUC slave clock time [ns]		DUC SV stream phase displacement			
	value [ns]	uncertainty [ns] $k = 2$	value [mdeg]	uncertainty [mdeg] $k = 2$	value [ns]	uncertainty [ns] $k = 2$
315	-373	320	4.83	1.21	268	67
215	-185	130	4.70	3.54	261	197
100	-204	646	3.77	3.56	210	163
0	42	335	0	2.76	0	153
-100	49	370	-1.96	3.56	-109	198
-215	311	128	-6.36	3.35	-353	186
-315	295	126	-6.71	1.48	-373	82

Figure 15 shows plots of DUC internal time and SV stream phase displacement vs. link asymmetry. In each case a first order polynomial fitted to the measurement data using weighted fitting, where weights are the reciprocals of squared measurement uncertainties. Unsurprisingly, a positive asymmetry causes a negative time error of the same magnitude in the slave clock, which in turn causes the slave device to timestamp SV data too early, causing a positive (leading) phase error. The slope of the phase error vs. asymmetry plot is $0.0188 \text{ m}^\circ/\text{ns}$, reasonably close to a theoretical ratio of

$$2\pi * 50\text{Hz} * \frac{180^\circ}{\pi} = 0.018 \frac{\text{m}^\circ}{\text{ns}}.$$

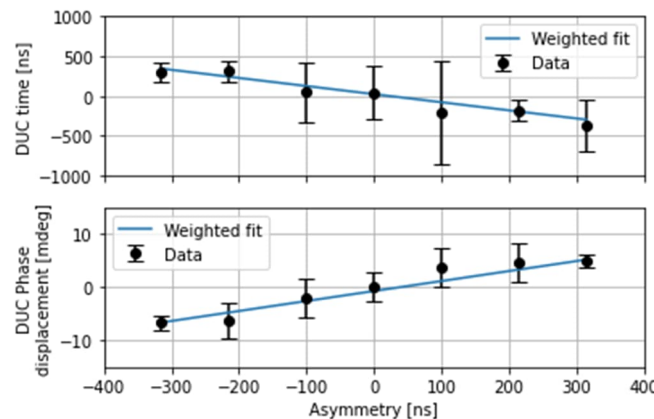


Figure 15. DUC internal time and phase displacement measurement results vs. link asymmetry.

6.6 Measurement results of various non-PTP network components

Other networking components, which are not used in VTT's calibration setup were tested in the project for their residence time. The tests include PTP and non-PTP compliant devices:

1. **Transparent clock residence time calibration.** Using the absolute probing method, it is possible to calibrate a transparent clock for the error it introduces due to miscalculating the data in the *correction* field associated with PTPv2 event messages passing through it. Another switch is added to the measurement setup to facilitate the test due to lack of TC support in the original switch.
2. **Non-PTP compliant networking components' residence time.** It may be desirable to know the residence time of PTP or any other message in networking equipment. Such devices include active network taps and media converters, which were tested using the probing setup.

Transparent clock residence time calibration

The setup can be used for determining an error introduced by a transparent clock miscalculating the residence time, which it is supposed to report as an updated value of the *correction* field in an event message, or in a follow-up message if a two-step mechanism for relaying event data is used. In this case the *Sync* and *Follow_Up* message pair is used. A second switch configured as a transparent clock is inserted in between the Grandmaster and boundary clocks and 100Base-TX TAPs are installed in both connections as in Figure 16 below. 1PPS signal is used for triggering the measurement but is not necessary for determining errors in the data due to the differential nature of the test.

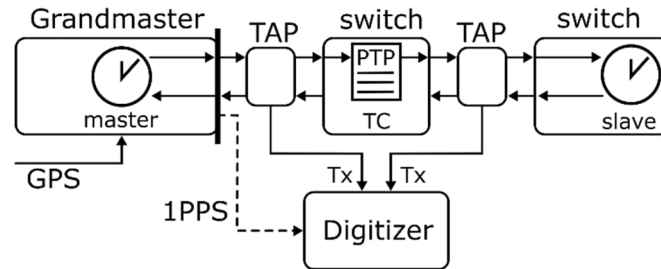


Figure 16. Measurement setup for testing a transparent clock for its residence time correction.

The ingress and egress time of a Sync message to and from the transparent clock is read using the digitizer and the corresponding *Follow_Up* message at the ingress and egress ports is decoded to read the change in *correction* field value. The residence time correction error Δt_{TC} is then calculated from

$$\Delta t_{TC} = t_{corr} - (t_{TC,e} - t_{TC,i}),$$

where t_{corr} is the updated correction field value read from the *Follow_Up* message, and $t_{TC,e}$ and $t_{TC,i}$ are respectively the Sync message egress and ingress times. The measured error is (-11.8 ± 2.4) ns as shown in Figure 17, where the measured average residence time of (1.05 ± 0.04) ms is subtracted from individual measured residence times, thus producing a plot centered around zero on the horizontal axis. The measurement is done using one concurrent SV stream in the switch. The switch seems to perform well considering that IEC 61850-9-3 allows for a transparent clock to introduce a maximum error of 100 ns. A higher traffic load may still have an impact on the time stamping quality.

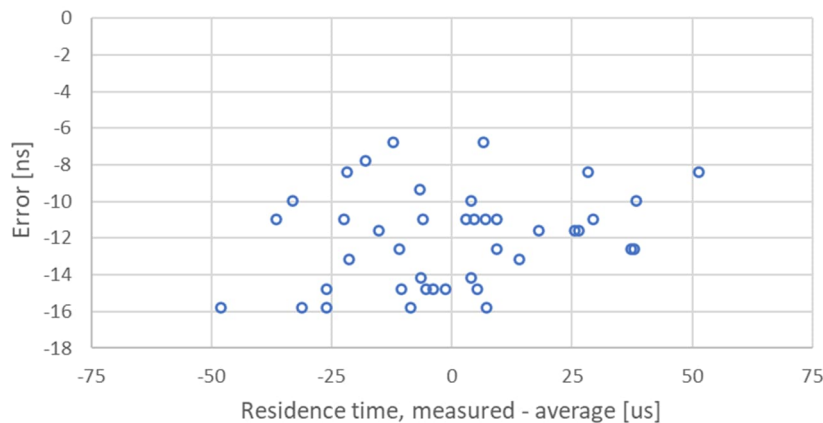


Figure 17. Transparent clock residence time correction error.

Non-PTP compliant networking components' residence time

Similarly to transparent clocks, residence time of various other network components may be determined. With non-PTP compliant devices that do not update the *correction* field in relevant PTP messages, the desirable function is to have as little of delay jitter as possible and no appreciable asymmetry. This way, the delay may be subtracted from any tests done using a probing method and the PTP delay mechanism has a chance to compensate for network latency correctly.

Any packet may be used for this purpose, but since VTT's ethernet probe is sensitive to PTP messages only, filtering out the rest, a stream of *Sync* and *Follow_Up* messages from a master to slave is used with the tested component inserted in between. An active traffic access point in non-aggregate mode and a 100Base-TX/100Base-FX media converter were tested for all relevant delays. The measurement setup is shown in Figure 18 with the DUT inserted in between the two clocks. The results are shown respectively for the TAP and media converter in Table 5 and Table 6. Uncertainty numbers include both the type B uncertainty

of the measurement setup and the standard deviation of the measurement data. Neither tested device introduces appreciable asymmetry into the link. The active network TAP has a reasonably high residence time and some deviation, but no asymmetry can be seen in the data.

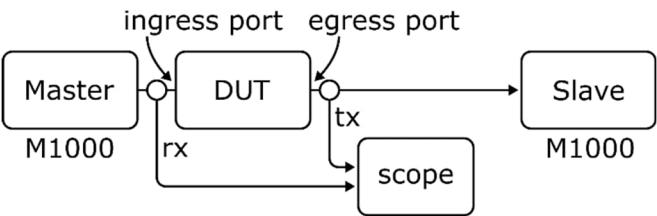


Figure 18. Test setup of non-PTP compliant networking devices

Table 5. Residence time of an active network traffic access point from port to port

Ingress port	Egress port	Residence time [ns]
Port A	Port B	7954 ± 35
Port B	Port A	7959 ± 34
PortA	Monitor Port 1	7955 ± 31
Port B	Monitor Port 2	7951 ± 34

Table 6. Residence time of a media converter

Ingress port	Egress port	Residence time [ns]
100Base-TX	100Base-FX	42 ± 1
100Base-FX	100Base-TX	57 ± 1

6.7 Digitizer triggering using PTP messages

The method of acquiring data contained in Ethernet frames of the PTP protocol and determining the timestamp for the SOF bit, described in section 7.4, is based on the use of a high-frequency (625 MHz) sampling device. For the typical PTP time update interval of 1 second, a one-second data buffer must also be maintained in the digitizer to ensure full capture of the PTP frame exchange transaction. If this is not possible due to hardware limitations of the digitizer, the method can be extended by using a trigger device to activate the digitizer at the moment PTP frames appear on the Ethernet link. This minimizes the number of samples that need to be recorded. Additionally, an extra time interval counter (TIC) is required to calculate the time of the SOF bit occurrence relative to the 1PPS signal. An example setup is shown in Figure 19. The trigger device may monitor network traffic via an additional TAP or via a mirror port on a switch.

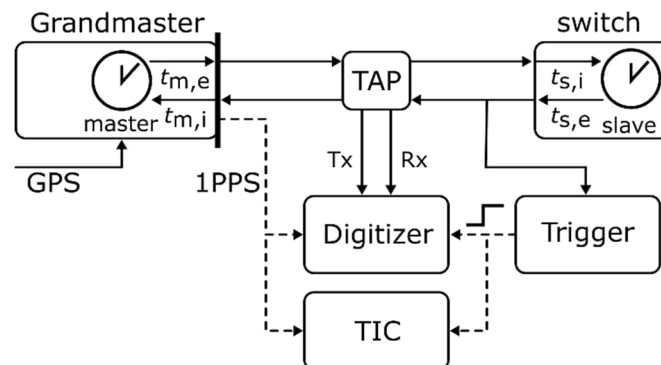


Figure 19. Example of setup with additional triggering device.

The trigger device can be built using e.g. the DP83640 Ethernet PHY integrated circuit and a host processor. This device can generate a signal on its output when an incoming PTP Ethernet frame is detected. The delay of this signal relative to the SOF bit is $7.5 \mu\text{s}$ with a standard deviation of 50 ns. Interrupt clearing by the host processor is performed via software by writing to a register in the chip and takes a maximum of 40 ms. The chip also supports hardware generation of a pulse precisely when the SOF bit appears. This allows for measuring the time difference between the trigger signal (indicating receipt of the PTP frame) and the SOF bit signal.

7 Golden calibrator pair approach

7.1 Extended PTP time synchronization model

The PTP synchronization model shown in [3] only concludes the ideal scenario in time synchronization, where the delays in the bi-directional link are symmetric and the clocks in master-slave hierarchy are synchronized. However, link asymmetry and clock offset are almost inevitable in realization. Therefore, the ideal time synchronization model needs to be extended to a general model which includes the real scenario of link asymmetry and clock offset.

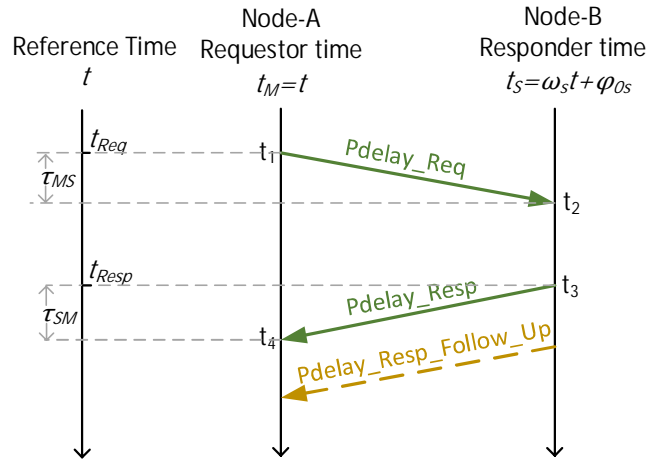


Figure 20. P2P time synchronization model

Figure 20 describes the extended timing exchange mechanism based on Peer-to-Peer (P2P) delay mechanism, which is used by Power Utility Profile IEC 61850-9-3. In this time synchronization model, Node-A and Node-B are synchronized via P2P mechanism, where Node-A serves as the master clock and Node-B is the slave clock. A reference time is used as the common reference of Node-A and Node-B clock. Assume Node-A clock follows the reference time, marked as $t_M = t$, and Node-B clock has a frequency and phase offset compared to Node-A, marked as $t_S = \omega_s t + \varphi_{0s}$. The moment that t_1 is sent is labelled as t_{Req} in the reference time, and the moment that t_3 is sent is labelled as t_{Resp} in the reference time. The propagation time of the timing message from Node-A to Node-B is τ_{MS} measured by the reference time, and the propagation time from Node-B to Node-A is τ_{SM} when measured by the reference time. Then we can deduced the relation between the local time of Node-A and Node-B and the reference time as:

$$\begin{cases} t_1 = t_{Req} \\ t_2 = \omega_s(t_{Req} + \tau_{MS}) + \varphi_{0s} \end{cases} \quad (1)$$

$$\begin{cases} t_3 = \omega_s t_{Resp} + \varphi_{0s} \\ t_4 = t_{Resp} + \tau_{SM} \end{cases} \quad (2)$$

Accordingly, in the syntonization case where $\omega_s \cong 1$, the message transmission time interval object $\langle meanPathDelay \rangle$ and the clock time error object $\langle offsetFromMaster \rangle$ can be derived as:

$$\begin{aligned} (t_2 - t_1) &= (\omega_s - 1)t_{Req} + \omega_s \tau_{MS} + \varphi_{0s} \\ &= \tau_{MS} + \varphi_{0s} \quad (\text{Let } \omega_s \cong 1) \end{aligned} \quad (3)$$

$$\begin{aligned} (t_4 - t_3) &= -(\omega_s - 1)t_{Resp} + \tau_{SM} - \varphi_{0s} \\ &= \tau_{SM} - \varphi_{0s} \quad (\text{Let } \omega_s \cong 1) \end{aligned} \quad (4)$$

$$\langle meanPathDelay \rangle = \frac{(t_2 - t_1) + (t_4 - t_3)}{2}$$

$$\begin{aligned}
 &= \frac{(\omega_s - 1)(t_{Req} - t_{Resp}) + (\omega_s \tau_{MS} + \varphi_{0s}) + (\tau_{SM} - \varphi_{0s})}{2} \\
 &\cong \frac{(\tau_{MS} + \varphi_{0s}) + (\tau_{SM} - \varphi_{0s})}{2} \quad (\text{Let } \omega_s = 1)
 \end{aligned} \tag{5}$$

$$\begin{aligned}
 \langle offsetFromMaster \rangle &= \frac{(t_2 - t_1) - (t_4 - t_3)}{2} \\
 &= \varphi_{0s} + \frac{(\omega_s - 1)(t_{Req} + t_{Resp}) + (\omega_s \tau_{MS} + \varphi_{0s}) - (\tau_{SM} - \varphi_{0s})}{2} \\
 &\cong \frac{(\tau_{MS} + \varphi_{0s}) - (\tau_{SM} - \varphi_{0s})}{2} \quad (\text{Let } \omega_s = 1)
 \end{aligned} \tag{6}$$

According to PTPv2 protocol [3], Node B will be synchronized to Node A by forcing $\langle offsetFromMaster \rangle = 0$ with the assumption of $\tau_{MS} = \tau_{SM}$. In an ideal symmetric link where $\tau_{MS} = \tau_{SM}$, $\varphi_{0s} = 0$ when forcing $\langle offsetFromMaster \rangle = 0$. While in an asymmetric link where $\tau_{MS} \neq \tau_{SM}$, forcing $\langle offsetFromMaster \rangle = 0$ leads to $\varphi_{0s} = -\frac{\tau_{MS} - \tau_{SM}}{2} \neq 0$. In summary, link asymmetry will cause an extra phase offset between a master clock and a slave clock under PTPv2 protocol.

7.2 PTP device time synchronization calibration model

The calibration model for PTP devices is shown in Figure 21. PTP devices are calibrated in pairs, where the pair of PTP devices is in master-slave hierarchy.

Taken the internal structure and function of a PTP device into consideration, a PTP device is divided into two units: Timing-message unit and Clock-servo unit. The timing-message unit implements the ingress and egress of PTP messages between the PTP port to the internal time-stamp clock, and the clock-servo unit corresponds to the RF signal conversion from the time-stamp clock to the pulse port. Here the time-stamp clock is defined as the internal clock of a PTP device which marks timestamps for PTP timing packets. Its clock time is referred to the moment when a timestamp is generated.

Furthermore, ingress and egress latencies in Timing-message unit as well as the electrical latencies in Clock-servo unit are defined specifically as follows:

$\Delta TXM_{PTP}, \Delta TXS_{PTP}$: PTP timing packet propagation delay from the moment when it is timestamped to the moment when the transmitted packet reaches to the PTP port in a master or slave device, respectively.

$\Delta RXM_{PTP}, \Delta RXS_{PTP}$: PTP timing packet propagation delay from the moment when it reaches the PTP port to the moment it is timestamped in the clock-servo unit in a master or slave device, respectively.

$\Delta PULSEM_{PTP2OUT}, \Delta PULSES_{PTP2OUT}$: electrical delay between the output of the time-stamp clock and the pulse output port in a master or slave device, respectively.

$\Delta PULSEM_{IN2OUT}$: electrical delay from reference PPS input port to the output of the time-stamp clock in a master device.

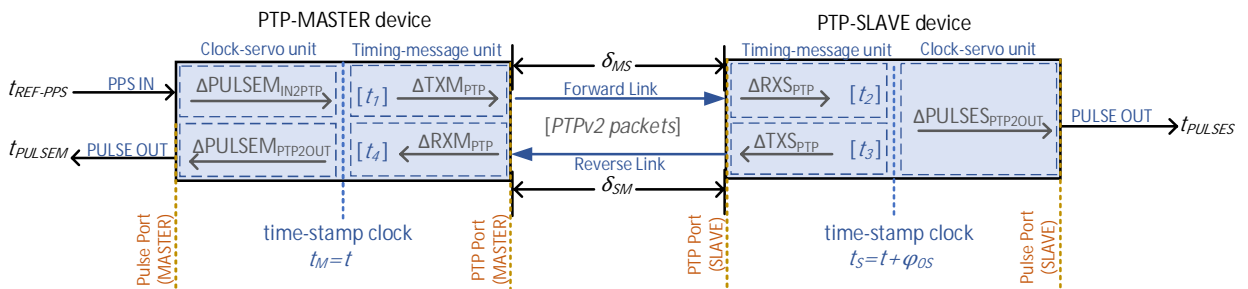


Figure 21. PTP devices calibration model

In the calibration model of Figure 21, the syntonization case is assumed, that the slave clock is syntonized with the master clock, leaving a constant phase offset of φ_{0s} with respect to the master clock.

Apply the calibration model to the extended PTP synchronization model described by equation (5) and (6), the relation among each items can be deduced as follows:

In a direct PTP link between a master PTP device and a slave PTP device, define the total PTP device latencies in forward link and reverse link as $\Delta XMS_{PTP} \stackrel{\text{def}}{=} \Delta TXM_{PTP} + \Delta RXS_{PTP}$, $\Delta XSM_{PTP} \stackrel{\text{def}}{=} \Delta TXS_{PTP} + \Delta RXM_{PTP}$, respectively. And the total PTP link latencies in bi-direction are defined as $\tau_{MS} = \Delta XMS_{PTP} + \delta_{MS}$, $\tau_{SM} = \Delta XSM_{PTP} + \delta_{SM}$, where δ_{MS} and δ_{SM} are the latencies from the transmission medium of the PTP link, for example, optical fibres or UTP cables, via forward and reverse links respectively. Accordingly, in the case of a direct connection between a pair of PTP devices, equation (3) and (4) can be explained as:

$$\begin{cases} (t_2 - t_1) = \Delta XMS_{PTP} + \delta_{MS} + \varphi_{0s} \\ (t_4 - t_3) = \Delta XSM_{PTP} + \delta_{SM} - \varphi_{0s} \end{cases} \quad (7)$$

Similarly, equation (5) and (6) can be elaborated in this scenario as:

$$\begin{aligned} \langle \text{meanPathDelay} \rangle_{meas} &= \frac{(t_2 - t_1) + (t_4 - t_3)}{2} \\ &= \frac{(\Delta XMS_{PTP} + \varphi_{0s}) + (\Delta XSM_{PTP} - \varphi_{0s})}{2} + \frac{\delta_{MS} + \delta_{SM}}{2} \end{aligned} \quad (8)$$

$$\begin{aligned} \langle \text{offsetFromMaster} \rangle_{meas} &= \frac{(t_2 - t_1) - (t_4 - t_3)}{2} \\ &= \frac{(\Delta XMS_{PTP} + \varphi_{0s}) - (\Delta XSM_{PTP} - \varphi_{0s})}{2} + \frac{\delta_{MS} - \delta_{SM}}{2} \end{aligned} \quad (9)$$

where the subscript $\langle \cdot \rangle_{meas}$ labels the measurement results.

Therefore, the time synchronization criteria of PTPv2 protocol can be elaborated in the proposed PTP calibration model as: let $\langle \text{offsetFromMaster} \rangle_{meas} = 0$ by assuming $\Delta XMS_{PTP} + \delta_{MS} = \Delta XSM_{PTP} + \delta_{SM}$. On the other hand, the asymmetry in the PTP link leads to an extra phase offset of the slave clock.

To investigate the source of the phase offset, φ_{0s} can be further categorized into two parts: ΔX_φ , the offset due to the asymmetry from PTP device and $\Delta \varphi_{link}$, the offset results from the asymmetry from PTP transmission link. Define $\varphi_{0s} \triangleq \Delta X_\varphi + \Delta \varphi_{link}$, and then equation (9) can be decomposed into:

$$\begin{cases} \Delta X_\varphi = \langle \text{offsetFromMaster} \rangle_{meas} - \frac{\Delta XMS_{PTP} - \Delta XSM_{PTP}}{2} \\ \Delta \varphi_{link} = -\frac{\delta_{MS} - \delta_{SM}}{2} \end{cases} \quad (10)$$

where $\Delta \varphi_{link}$ is the link-dependent phase offset of the slave clock, and ΔX_φ is device-dependent phase offset of the slave clock.

In addition to PTP messages, pulse signal measurements has the relation of:

$$\begin{aligned} t_{PULSEM} &= t + \Delta PULSEM_{PTP2OUT} \\ t_{PULSES} &= t + \varphi_{0s} + \Delta PULSES_{PTP2OUT} \\ t_{REF-PPS} &= t - \Delta PULSEM_{IN2PTP} \end{aligned} \quad (11)$$

Then the phase difference between two pulse signals, which could be measured by a Time Interval Counter (TIC), for example, can be expressed as:

$$\begin{aligned} \langle \Delta TIC_{MS} \rangle_{meas} &= t_{PULSEM} - t_{PULSES} \\ &= (\Delta PULSEM_{PTP2OUT} - \Delta PULSES_{PTP2OUT}) - \varphi_{0s} \\ &\stackrel{\text{def}}{=} \Delta PULSEMS_{PTP2OUT} - \varphi_{0s} \end{aligned} \quad (12)$$

$$\begin{aligned} \langle \Delta TIC_{REF2M} \rangle_{meas} &= t_{REF-PPS} - t_{PULSEM} \\ &= -\Delta PULSEM_{IN2PTP} - \Delta PULSEM_{PTP2OUT} \\ &\stackrel{\text{def}}{=} \Delta PULSEM_{IN2OUT} \end{aligned} \quad (13)$$

Combining equation (8), equation (9) and equation (12), an equation set can be summarized to describe the relation between the measurements and the unknown variables in a PTP link:

$$\left\{ \begin{array}{l} \frac{(\Delta XMS_{PTP} + \Delta X_{\varphi}) + (\Delta XSM_{PTP} - \Delta X_{\varphi})}{2} = \langle meanPathDelay \rangle_{meas} - \frac{\delta_{MS} + \delta_{SM}}{2} \\ \frac{(\Delta XMS_{PTP} + \Delta X_{\varphi}) - (\Delta XSM_{PTP} - \Delta X_{\varphi})}{2} = \langle offsetFromMaster \rangle_{meas} \\ \varphi_{0s} = \Delta X_{\varphi} + \Delta \varphi_{link}, \text{ where } \Delta \varphi_{link} = -\frac{\delta_{MS} - \delta_{SM}}{2} \\ (\Delta PULSEMS_{PTP2OUT} - \varphi_{0s}) = \langle \Delta TIC_{MS} \rangle_{meas} \\ \Delta PULSEM_{IN2OUT} = \langle \Delta TIC_{REF2M} \rangle_{meas} \end{array} \right. \quad (14)$$

where the unknown variants are all on the left side of the equations, and they are ΔXMS_{PTP} , ΔXSM_{PTP} , $\Delta PULSEMS_{PTP2OUT}$, and φ_{0s} (including ΔX_{φ} and $\Delta \varphi_{link}$), and the measurements are on the right side of the equations.

7.3 PTP device calibration principle

The proposed PTP device calibration is based on a pair of PTP devices in master-slave hierarchy. The ingress and egress latencies of the PTP device pair are calculated based on the measurements of timing messages as well as pulse phase offset, referring to equation (14). Since the device latency calibration results are only valid on a pair of devices, the calibration results will be passed down through a reference PTP pair. The reference PTP pair can be called “Golden Calibrator”, that the master device and slave device in the “Golden Calibrator” can be named as “Golden Master” and “Golden Slave” respectively. The “Golden Calibrator” will be used as the common reference for the other PTP Devices Under Calibration (DUCs). And all the other PTP DUCs can be traceable to “Golden Calibrator” by connecting either “Golden Master” or “Golden Slave” with the DUC as a new PTP link for calibration.

The calibration of “Golden Calibrator” follows the PTP link mathematical model described in equation (14). Specifically, let $\Delta X_{\varphi} = 0$ by selecting a virtual time-stamp clock reference plane, then the asymmetry due to the devices is attributed to the offset in $\langle offsetFromMaster \rangle$. Then it could get:

$$\left\{ \begin{array}{l} [\Delta XMS_{PTP}]_{cal} = \langle meanPathDelay \rangle_{meas} - \frac{\delta_{MS} + \delta_{SM}}{2} + \langle offsetFromMaster \rangle_{meas} \\ [\Delta XSM_{PTP}]_{cal} = \langle meanPathDelay \rangle_{meas} - \frac{\delta_{MS} + \delta_{SM}}{2} - \langle offsetFromMaster \rangle_{meas} \\ [\Delta PULSEMS_{PTP2OUT}]_{cal} = \langle \Delta TIC_{MS} \rangle_{meas} - \frac{\delta_{MS} - \delta_{SM}}{2} \\ [\Delta PULSEM_{IN2OUT}]_{cal} = \langle \Delta TIC_{REF2M} \rangle_{meas} \end{array} \right. \quad (15)$$

where $[\cdot]_{cal}$ indicates the calibration result of the variable. Equation (15) is the calibration model of PTP “Golden Calibrator” pair.

7.4 New tools for transmission medium latency calibration

The calibration of the PTP bi-directional link delay δ_{MS} and δ_{SM} is the prerequisite of the PTP device calibration. For majority of the PTP devices, the transmission medium of a direct PTP link is either a UTP cable with RJ45 connectors on two sides, or an optical fiber with SFP connectors on two sides. One method to calibrate δ_{MS} and δ_{SM} is to use a pair of PTP devices. δ_{MS} and δ_{SM} can be measured by the internal time interval counter object $\langle meanPathDelay \rangle$ of the PTP device. Firstly setup a direct PTP link between two PTP devices, and measure the $\langle meanPathDelay \rangle$ object to get the direct PTP link delay. And then cascade the UTP cable or optical fibre under calibration to the direct link and measure $\langle meanPathDelay \rangle$ again. The subtraction of the two measurements is the averaged one-way delay of the cable/fibre under calibration. However, this method is limited by the accuracy and precision of the PTP device internal counter, normally the limitation is up to several ns level. And the verification of the measurement accuracy is another issue to be solved.

Here we propose an independent measurement method to measure the time delay of UTP cables and optical fibres with the measurement uncertainty of sub-ns level. The calibration kit of CalKitRJ45 is designed to

calibrate the UTP cable delay, and the calibration kit of CalKitSFP is to calibrate the optical fibre delay. Figure 22 and Figure 23 show the block diagram of the two calibration kits. The idea of the proposed calibration kit is to convert a pulse signal with a single-end co-axial RF port to a differential-end pulse signal with RJ45/SFP connector, and therefore the delay calibration of UTP cable/optical fibre is transferred to the delay calibration of a co-axial RF cable, which is a proven calibration method in metrology.

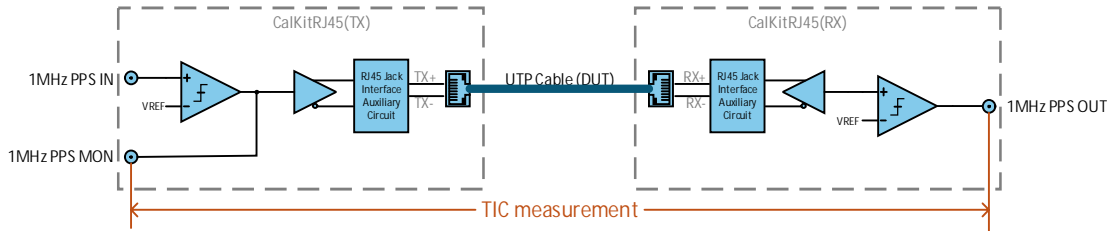


Figure 22 Simplified block diagram of CalKitRJ45 latency measurement setup

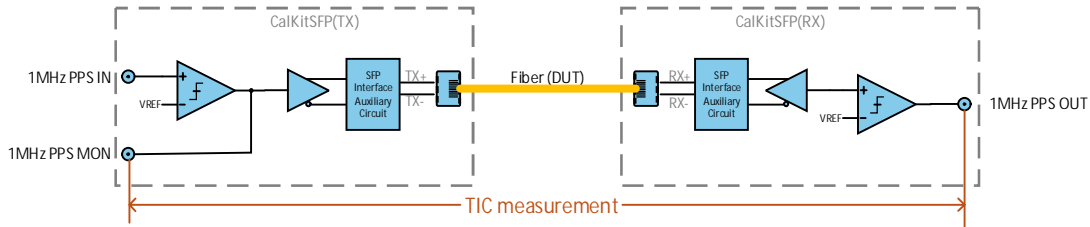


Figure 23. Simplified block diagram of CalKitSFP latency measurement setup

7.5 PTP “Golden Calibrator” calibration results

The calibration procedure of the “Golden Calibrator” can be concluded as:

Step 1: build the PTP “Golden Calibrator” setup, where a direct PTP link is setup between the “Golden Master” device and the “Golden Slave” device. Besides, the setups of timing message measurements and pulse phase offset measurements are ready.

Step 2: measure δ_{MS} and δ_{SM} , and collect the raw data measurements of $\langle meanPathDelay \rangle_{meas}$, $\langle offsetFromMaster \rangle_{meas}$, and $\langle \Delta TIC_{MS} \rangle_{meas}$.

Step 3: calibrate $[\Delta XMS_{PTP}]_{cal}$, $[\Delta XSM_{PTP}]_{cal}$, and $[\Delta PULSEMS_{PTP2OUT}]_{cal}$ according to equation (15).

The calibration setup of the “Golden Calibrator” is demonstrated in Figure 24. Two PTP devices are connected via two cascaded UTP cables and a direct tap. A PTP link is running by applying Power Utility Profile IEC 61850-9-3. Two setups are built for calibration:

- (1) Configure one PTP device as Grandmaster and the other as Slave. The collected raw data and statistics are shown in Figure 25 and Table 7.
- (2) Swap “Golden Master” and “Golden Slave” to build another setup. The raw data and statistics are listed in Figure 26 and Table 8.

Besides of the uncertainties in the measurements, the main systematic uncertainties come from the reboot of the PTP devices. Figure 27 show the offset of the measurements when rebooting the PTP devices for multiple times. In addition, the measurement uncertainty from the TIC is also added to the systematic uncertainty.

Categorize the standard deviation of the measurements as Type A uncertainty σ_A , and the systematic uncertainty as Type B uncertainty σ_B , then the total uncertainty of the measurements is $\sigma_T = \sqrt{\sigma_A^2 + \sigma_B^2}$, and choose $k=2$ expanded uncertainty as the final uncertainty budget. Final calibration results of the two setups are listed in Table 8 and Table 10.



Raw data item	mean, ns	std, ns
$\langle meanPathDelay \rangle_{meas}$	1.6	1.7
δ_{MS}	10.85	0.03
δ_{SM}	10.85	0.03
$\langle offsetFromMaster \rangle_{meas}$	-7.5	5.1
$\langle \Delta TIC_{MS} \rangle_{meas}$	-6.2	5.0

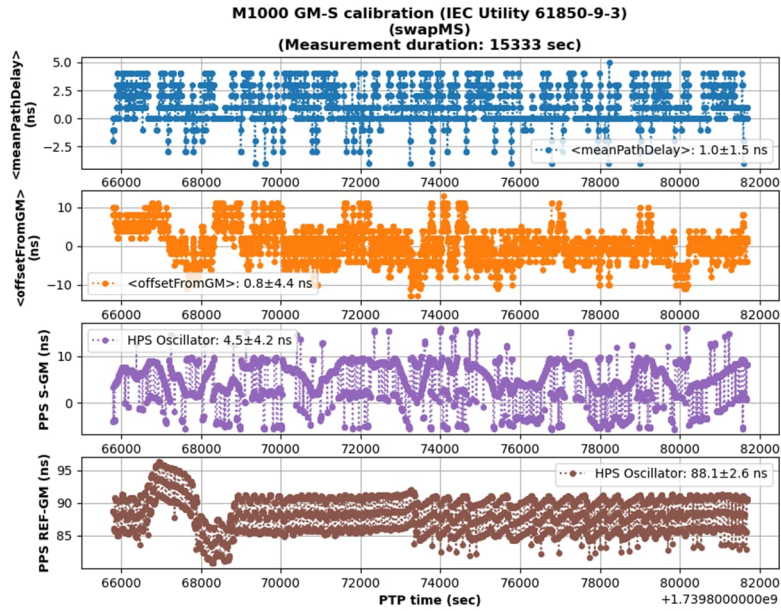


Figure 26. Raw data of "Golden Calibrator" calibration (swap Master-Slave)

Table 8. "Golden Calibrator" (swap Master-Slave) raw data statistics

Raw data item	mean [ns]	std [ns]
$\langle \text{meanPathDelay} \rangle_{\text{meas}}$	1.0	1.5
δ_{MS}	10.85	0.03
δ_{SM}	10.85	0.03
$\langle \text{offsetFromMaster} \rangle_{\text{meas}}$	0.8	4.4
$\langle \Delta TIC_{MS} \rangle_{\text{meas}}$	-4.5	4.2

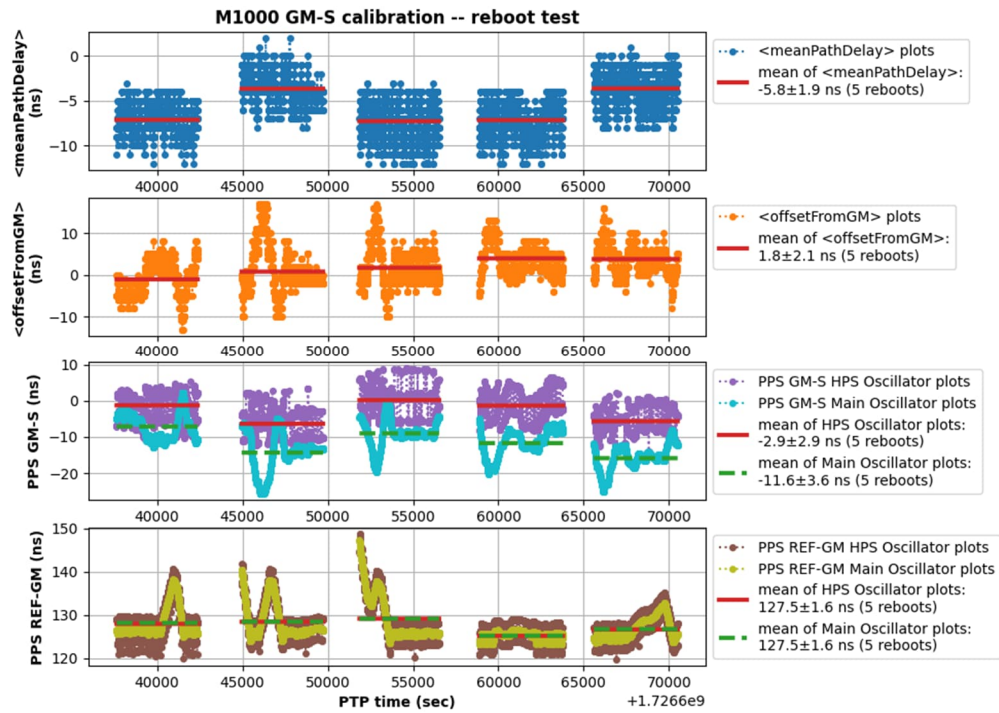


Figure 27. Reboot uncertainty of "Golden Calibrator" pair

Table 9. "Golden Calibrator" calibration results

Calibration item	mean, ns	σ_A , ns	σ_B , ns	σ_T , ns	$\kappa\sigma_T(\kappa = 2)$, ns
$[\Delta XMS_{PTP}]_{cal}$	-16.8	5.4	2.8	6.1	12.2
$[\Delta XSM_{PTP}]_{cal}$	-1.8	5.4	2.8	6.1	12.2
$[\Delta PULSEMS_{PTP2OUT}]_{cal}$	-6.2	5.0	2.9	5.8	11.6

Table 10 "Golden Calibrator" (swap Master-Slave) calibration results

Calibration item	mean, ns	σ_A , ns	σ_B , ns	σ_T , ns	$\kappa\sigma_T(\kappa = 2)$, ns
$[\Delta XMS_{PTP}]_{cal}$	-9.1	4.6	2.8	5.4	10.9
$[\Delta XSM_{PTP}]_{cal}$	-10.7	4.6	2.8	5.4	10.9
$[\Delta PULSEMS_{PTP2OUT}]_{cal}$	-4.5	4.2	2.9	5.1	10.2

8 Alternate method using time tagging at PHC, RISE

The absolute calibration method requires special purpose hardware and is, even though universally designed, quite specific in its implementation for 100BASE layers. The required computational effort is challenging, but results in best possible performance regarding traceable timing. Capturing PTP events is however tedious and time consuming.

Considering Figure 8, the main digitizer and its necessary post processed decoding logic can be replaced by a modern network interface and a network stack. Figure 28, depicts a generic setup for capturing Ethernet traffic using external equipment to provide time traceability. The approach makes use of widely available COTS hardware, is simple to use, and has the flexibility to interface any physical layer and speed available on Ethernet interface hardware supported by the Linux³ kernel. Linux timing APIs expose the clock work present on those network interfaces and offer all necessary functionality to replicate the absolute method that uses an oscilloscope as digitizer.

Linux timing infrastructure offers access to physical hardware clocks (PHC) on Ethernet interfaces and allows time stamping of Ethernet frames as well as external events in the form of 1PPS representations of a traceable timescale. Together with an active or passive TAP device the Ethernet frame data is collected using for instance a PCAP [8] based application that integrates timing management, traffic capture and extracts Ethernet frame time stamping and the content of the relevant PTP messages. Ingress/egress delay determination is the same as in the discrete capture of data traffic described above.

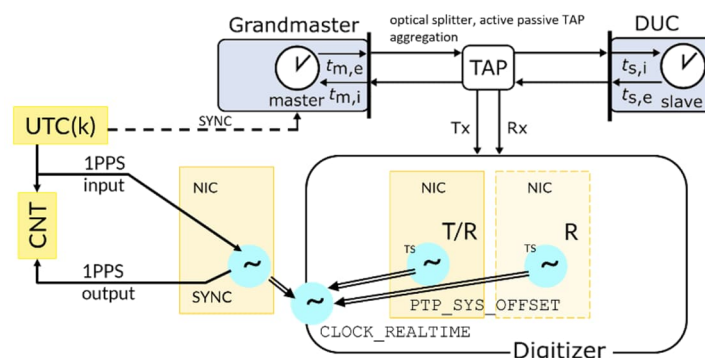


Figure 28 Generic setup using Ethernet interfaces and Linux kernel APIs. This setup uses three interfaces, one for external sync, and two for capturing the tapped communication between time source and sink.

The typical TAP device duplicates the respective unidirectional data streams on a transmission line to two interfaces that can capture the relevant traffic. The network interface clocks are used to timestamp the incoming Ethernet frames. Timing related capabilities (`ethtool -T`) of the devices are varying, but often explicitly support PTP event packets in the hardware receive filters, which besides a physical clock (PHC) and receive hardware time stamping, is a minimal precondition for being suitable for use as *digitizer* interfaces.

```
ethtool -T eno1
Time stamping parameters for eno1:
Capabilities:
    hardware-transmit      (SOFTIMESTAMPING_TX_HARDWARE)
    software-transmit      (SOFTIMESTAMPING_TX_SOFTWARE)
    hardware-receive       (SOFTIMESTAMPING_RX_HARDWARE)
    software-receive       (SOFTIMESTAMPING_RX_SOFTWARE)
    software-system-clock  (SOFTIMESTAMPING_SOFTWARE)
    hardware-raw-clock     (SOFTIMESTAMPING_RAW_HARDWARE)
PTP Hardware Clock: 0
Hardware Transmit Timestamp Modes:
    off                    (HWTSTAMP_TX_OFF)
```

³ Or other operating systems that expose the Ethernet clock infrastructure as APIs. Linux is however the most readily available option.

```

on (HWTSTAMP_TX_ON)
Hardware Receive Filter Modes:

none (HWTSTAMP_FILTER_NONE)
all (HWTSTAMP_FILTER_ALL)
ptpv1-l4-sync (HWTSTAMP_FILTER_PTP_V1_L4_SYNC)
ptpv1-l4-delay-req (HWTSTAMP_FILTER_PTP_V1_L4_DELAY_REQ)
ptpv2-l4-event (HWTSTAMP_FILTER_PTP_V2_L4_EVENT)
...
ptpv2-event (HWTSTAMP_FILTER_PTP_V2_EVENT)
ptpv2-sync (HWTSTAMP_FILTER_PTP_V2_SYNC)
ptpv2-delay-req (HWTSTAMP_FILTER_PTP_V2_DELAY_REQ)

```

For an interface *x*, the PHC is found in the device tree `/dev/ptpx` and exposes its capabilities through the PTP hardware clock infrastructure for Linux [9]. Several user tools exist that allow to inspect and interact with the clocks in the system, such as `phc_ctl` from the `linuxptp` software suite [10]:

```

phc_ctl eno1 caps
phc_ctl[5797288.125]:
capabilities:
  62499999 maximum frequency adjustment (ppb)
  0 programable alarms
  2 external time stamp channels
  2 programmable periodic signals
  4 configurable input/output pins
  has pulse per second support
  has cross timestamping support
  doesn't have adjust phase support

```

The above example shows the PHC capabilities of a motherboard-integrated Intel I225-LM. The PHC has external time stamp channels and allows to output periodic signals on the configurable pins. Those pins may not always be accessible on the hardware, especially if the solution is integrated as in the example above. If accessible, the PHC can measure external pulses, such as a reference 1 PPS signals. Similarly, can 1PPS be generated that represent the PHC phase and establish traceability to an external timescale. This situation is depicted in the left part of Figure 28. The reference delay and the total internal delay $1PPS_{in}-1PPS_{out}$, i.e. between input reference pulse and its time stamping representation, must be established by using a counter and evaluating the time stamps created by the external events of the time reference. On typical I225/6 expansion cards the SPD pin header can be wired to establish a reference plane for such calibration. Typical values for the internal delay are about 45 ns and need to be estimated for every setup. The inability to determine the time stamp delay with respect to an external reference poses one of the largest uncertainties with this method. If the input and output delays are considered symmetrical, the uncertainty for interfacing external reference is thus in the order of 22.5 ns.

As at least two interfaces are needed to capture all relevant packets, the respective PHCs need to be synchronized, or the phase differences needs to be measured and corrected for.

If synchronization is preferred a PHC can be synced to an external 1PPS reference by steering the PHC using the `EXTTS` measurements. Depending on the quality of the reference and the NIC local oscillatory, synchronizing can be done with a jitter of a few nanoseconds.

```

ts2phc -f ts2phc.conf
ts2phc[92120.552]: /dev/ptp0 offset 199 s0 freq +7328
ts2phc[92121.552]: /dev/ptp0 offset 199 s2 freq +7328
ts2phc[92122.552]: /dev/ptp0 offset 206 s2 freq +7534
ts2phc[92123.552]: /dev/ptp0 offset 0 s2 freq +7390
ts2phc[92124.552]: /dev/ptp0 offset -62 s2 freq +7328
ts2phc[92125.552]: /dev/ptp0 offset -61 s2 freq +7310
ts2phc[92126.552]: /dev/ptp0 offset -44 s2 freq +7309
ts2phc[92127.552]: /dev/ptp0 offset -24 s2 freq +7316
ts2phc[92128.552]: /dev/ptp0 offset -6 s2 freq +7326
ts2phc[92129.552]: /dev/ptp0 offset -4 s2 freq +7327
ts2phc[92130.552]: /dev/ptp0 offset -3 s2 freq +7326
ts2phc[92131.552]: /dev/ptp0 offset -1 s2 freq +7328
ts2phc[92132.552]: /dev/ptp0 offset -1 s2 freq +7327
ts2phc[92133.552]: /dev/ptp0 offset 0 s2 freq +7328

```


Common practice is to use several interfaces with EXTTS time input tied to the same reference creating a common clock. The use of shared PHCs on network cards with several interfaces (e.g. Intel E810-xxvda2) is a convenient method yielding low uncertainties of time tagging the tapped communication. Figure 28 however suggests using a single interface for synchronization and separate interfaces for capturing data. This is a more realistic setup for use with COTS server hardware that integrate interfaces, or the use of compact units with a single PCIe expansion slot for field calibrations. In such a case the PHC synchronization within the same system requires internal measurements. Traditional methods apply repetitive polls of the PHCs versus the system clock to establish statistics that minimize the measurement error, which can be substantial and may not be appropriate for the purpose of PTP calibrations.

PCIe Precision Time Measurements is an PCIe standard (PTM [13]) increasingly found on modern Intel based system which implements an efficient time measurement across the PCI Express bus. Using PTM, PHC and system clocks can be measured with low jitter (e.g. Intel i226, Xeon gen4+) and synchronization can be established across all the PHCs on a system. Typical timing resolution is a few nanoseconds limiting the measurements and a consequent synchronization for which the `phc2sys` tool can be used. Steady state synchronization jitter is usually below 10 ns.

```
phc2sys -s CLOCK_REALTIME -c enpls0 -O 0 -m -w
phc2sys[155.859]: enpls0 sys offset      5246 s2 freq +11979 delay 0
phc2sys[156.859]: enpls0 sys offset      2977 s2 freq +11283 delay 0
phc2sys[157.860]: enpls0 sys offset      1371 s2 freq +10570 delay 0
phc2sys[158.860]: enpls0 sys offset        505 s2 freq +10116 delay 0
phc2sys[159.861]: enpls0 sys offset         70 s2 freq +9832 delay 0
phc2sys[160.861]: enpls0 sys offset        -51 s2 freq +9732 delay 0
phc2sys[161.862]: enpls0 sys offset       -101 s2 freq +9667 delay 0
phc2sys[162.862]: enpls0 sys offset       -76 s2 freq +9662 delay 0
phc2sys[163.863]: enpls0 sys offset       -47 s2 freq +9668 delay 0
phc2sys[164.863]: enpls0 sys offset       -15 s2 freq +9686 delay 0
phc2sys[165.864]: enpls0 sys offset       -30 s2 freq +9666 delay 0
phc2sys[166.864]: enpls0 sys offset         2 s2 freq +9689 delay 0
phc2sys[167.865]: enpls0 sys offset        -9 s2 freq +9679 delay 0
phc2sys[168.865]: enpls0 sys offset         8 s2 freq +9693 delay 0
phc2sys[169.866]: enpls0 sys offset        -1 s2 freq +9687 delay 0
```

It is however not always necessary nor desirable to synchronize clocks. Good practice in time and frequency metrology prefers to measure and track clock differences instead of steering clocks. Any clock preserves its inherent stability if left free running. However, the clocks implemented on network devices often have questionable properties that not always can be exploited, thus rapid steering is a valid option.

Table 11 lists timing related properties of a few common, both legacy and available, both suitable and unsuitable, network interfaces. Suitability for the purpose of replacing the *digitizer* of the absolute method lays in the combination of capabilities of hardware timestamping of PTP frame types, referencing and/or sourcing external timing, and possibly high precisions inter-PHC measurements.

Table 11 Properties of commonly available network interface types, either as pluggable PCIe or found as integrated devices found in COTS server hardware. Unless SFP is indicated, interfaces support electrical twisted pair. Green rows indicate suitability.

Type	Driver	IFace	PHC	TSHW_CLK	TSHW_TX	TSHW_RX	HWFLT_TX	HWFLT_RX all	EXT_PINS	EXTTS	PULSE_OUT	CROSS_TS	SYS_PPS	PTM	Granularity
I210	igb	1GE	1	y	y	y	y	y	4	2	2	n	y	n	-
I225/6	igc	2.5GE	1	y	y	y	y	y	4	2	2	y	y	y	4
I350	igb	1GE	1	y	y	y	y	y	0	0	0	n	n	n	-
82576	igb	1GE	1	y	y	y	y	n	0	0	0	n	n	n	-
BCM5719	tg3	1GE	1	y	y	y	y	n	0	0	1	n	n	n	-
BCM5720	tg3	1GE	1	y	y	y	y	n	0	0	1	n	n	n	-
X553	ixgbe	1GE	0	y	y	y	y	y	0	0	0	n	n	n	-
E810-XXV	ice	25GE 4,2xSFP	1	y	y	y	y	y	0	3	4	n	n	n	-
ConnectX-6 Dx	mlx5_core	25GE 2xSFP	2	y	y	y	y	y	0	0	0	n	n	n	-
RPi CM4	bcmgenet	1GE	1	y	y	y	y	n	1	1	1	n	n	n	-

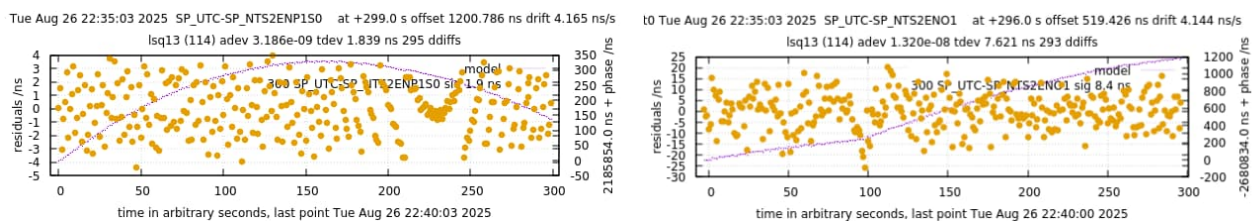


Figure 29 Example of the estimation of free running PHCs with respect to an external reference UTC(SP). The left graph shows a snapshot of the timing of the synchronization interface using external 1PPS input/output. The clock is estimated using high order least squares that allow the short-term interpolation of the clock. The one second time deviation is in the order of 2 ns, as are the residual statistics of the window sized 300 s. The right graph shows the timing estimate of one of the capture interfaces. The measurements involve PTM via the system clock which is managed by NTP. Possible rapid changes in the system clock phase are mainly in common mode in all the measurements. The estimated noise in the capture clock with respect to the reference is about 8 ns.

For practical use a simple PCAP application written in a suitable programming language such as C or C++ can integrate all required settings of the PHC infrastructure and coordinate the necessary time measurements and corrections to yield correct time stamps. Decoding of the captured traffic extracts the same information as with the oscilloscope method and yields the same functionality. For reference and example can be found in [14]

Below an example of the output capturing time stamps for symmetric Peer Delay exchange including an estimate of the clocks involved as depicted in Figure 28. Interface ENP1S0 is used as clock input and management interface of the system that includes time of day disambiguation of the connected reference UTC(SP). Interfaces ENO1 and ENO2 are capture interfaces, where the system identifies as NTS2 providing the common clock for all measurements.

```
#clock measurements      offset_ns      unc clock_difference
1759126403.9995453358    -8288.0 0.0 5.0 SP_NTS2-SP_NTS2EN01 1
1759126403.9996111393    -11489.0 0.0 5.0 SP_NTS2-SP_NTS2EN02 2
1759126403.9997596741     62570.0 0.0 5.0 SP_NTS2-SP_NTS2ENP1S0 0
1759126404.0000000000     95332.0 0.0 5.0 SP_UTC-SP_NTS2ENP1S0
1759126404.0000000000     24474.0 0.0 5.0 SP_UTC-SP_NTS2EN01
1759126404.0000000000     21273.0 0.0 5.0 SP_UTC-SP_NTS2EN02

#captured traffic      type      sequence packet_corr      packet_time_stamp      foreign_PTP_port      message local_clock
1759126404.0364035691 02 0000 0 18720 0.000000000000 1759126441.36400985718 ec:46:70:ff:fe:0a:b2:ff:00:01 Pdelay_Req SP_NTS2EN02
1759126404.0364179027 03 0200 0 18720 0.000000000000 1759126441.36405777931 ec:46:70:ff:fe:0a:b3:00:00:01 Pdelay_Resp SP_NTS2EN02
1759126404.0364238865 10 0000 0 18720 0.000000000000 1759126441.36420416832 ec:46:70:ff:fe:0a:b3:00:00:01 Pdelay_Resp_Follow_Up SP_NTS2EN02
1759126404.0539775662 00 0200 0 11477 0.000000000000 1759126441.53977155685 ec:46:70:ff:fe:0a:b2:ff:00:01 Sync SP_NTS2EN02
1759126404.0539835182 08 0000 0 11477 0.000000000000 1759126441.53979754448 ec:46:70:ff:fe:0a:b2:ff:00:01 Follow_Up SP_NTS2EN02
1759126404.0930478902 02 0000 0 18735 0.000000000000 1759126441.93045997620 ec:46:70:ff:fe:0a:b3:00:00:01 Pdelay_Req SP_NTS2EN01
1759126404.0930630566 03 0200 0 18735 0.000000000000 1759126441.93050408363 ec:46:70:ff:fe:0a:b2:ff:00:01 Pdelay_Resp
1759126404.0930695404 10 0000 0 18735 0.000000000000 1759126441.93065261841 ec:46:70:ff:fe:0a:b2:ff:00:01 Pdelay_Resp_Follow_Up
```

The use of network interface cards has many practical advantages but suffers from difficulties determining the TAP related delays $t_{1..5}$, as shown in Figure 8. TAPs should be passive, such as optical splitters, but for twisted pair interfaces faster than 100BASE, active monitoring TAPs are the only feasible option. As the time stamp points of the Rx and Tx paths are not directly accessible, the estimation of t_5 , with possibly different values t_{5Rx} and t_{5Tx} , requires a calibrated PTP source, such as a White Rabbit Grand Master, to be used to calibrate the setup. Thus, uncertainties of this convenient approach are significantly higher than the oscilloscope method and can be generally to be about 50 ns, which is still sufficient for the application of digital substations, and possibly many other uses. Most modern Ethernet physical layer variants can easily be accessed with the same methodology, up to 10GBASE-T and 25GBASE-xR can be demonstrated.

9 Comparison of absolute and relative calibration methods

For validating the methods presented in this good practice guide, a comparison measurement between VTT's absolute calibration method and VSL's relative calibration method was performed. Both setups were transferred to a common location. VTT's probe was set up to monitor the traffic between VSL's master and slave clocks. The time tag associated with PTP event messages and the internal PTP time inside the devices calculated from the data were compared against a master clock's 1PPS output. The Slave clock 1PPS output timing was calculated based on time interval comparison in the time interval counter (TIC). This way, both master and slave clock's internal time could be compared against their respective 1PPS outputs.

The setups are shown in Figure 30 and Figure 31. The clocks are connected to one another using a 100Base-TX link, with the TAP situated between them. Clock 1 was first configured as a master (Figure 31), itself synchronized from a local UTC realization via 1PPS and NTP. Both master and slave 1PPS outputs were in turn compared to the residual PTP errors calculated from the traffic between the clocks. The master-slave hierarchy was then reversed (Figure 31), with 1PPS output of the new master compared to the traffic similarly to the first case.

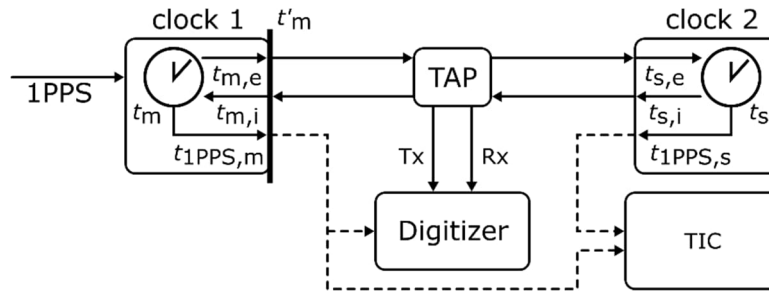


Figure 30. Measurement setup for comparing absolute and relative clock calibration methods. Clock 1 is master.

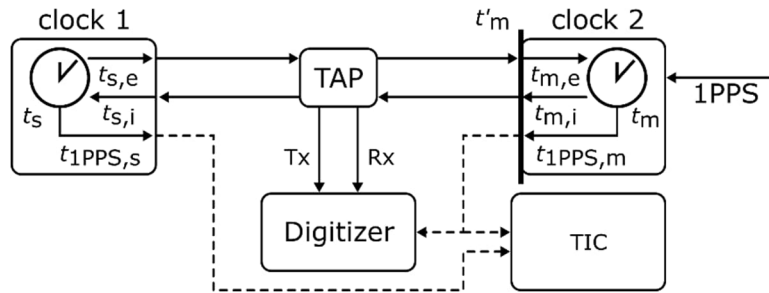


Figure 31. Reversed measurement setup for comparing absolute and relative clock calibration methods. Clock 2 is master.

In both cases, master port 1PPS output is defined as the timing reference plane. All results using the probing method are thus referenced to it. While not drawn in FIGURE, internal time $t_{m/s}$ and asymmetry $t_{a,m/s}$ of both clocks are calculated from the probing data, with positive asymmetry in all cases towards network. Using the probing data, the slave clock timing can be calculated in two ways, directly assuming $t_s = t_{d,s}$ and indirectly from apparent master clock time $t'_m = t_m + t_{a,m} - t_{a,s}$.

Slave clock internal time with respect to its 1PPS output may conveniently be calculated from the interval measurement using the TIC. If we define the slave to master TIC measurement as t_{SM} , with a positive sign when the master is ahead, slave 1PPS output error may be defined as

$$t_{1PPS,s} = t_m + t_{SM} - t_s$$

In a no-error scenario when $t_m = 0$, $t_{1PPS,s} = 0$ and $t_{SM} = t_s$ the slave clock 1PPS output should be aligned with master clock time ($t_{1PPS,s} = t_m$), indicating a perfect operation of the PTP pair. It should be noted that here it is assumed that master clock 1PPS output error $t_{1PPS,m}$ is by definition the same as master clock internal time, but with an opposing sign. In any case, it is included in the calculation through probing the master clock internal time and defining the 1PPS output as the reference plane. If an error such that $t_{SM} \neq t_s$ is introduced by any of the components in the link, i.e. either asymmetry in master or slave clocks or communications path, it should

be visible in both slave internal time and slave 1PPS output time and its magnitude measurable using the probing method or the TIC.

Measurement data including standard deviations from the comparison are summarized in Table 12. The measured 1PPS difference t_{SM} in both measurement setups is shown in Figure 32 and Figure 33. The figures show most importantly the long-term stability of the link, while in the short term, the difference occasionally jumps by multiples of roughly 8 ns. This is due to quantization of the 100 Mbit/s link bit rate and a high-bandwidth clock servo loop in the slave clock, which clearly tracks the instantaneous time delivered by the PTP messages.

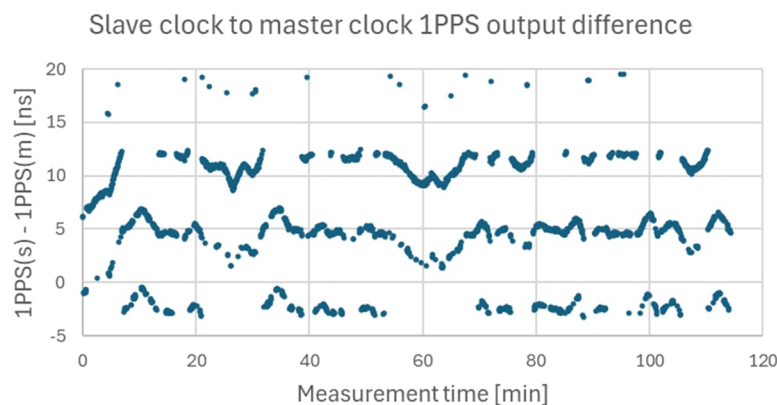


Figure 32. Time interval measurement between master and slave clock 1PPS outputs in setup 1.

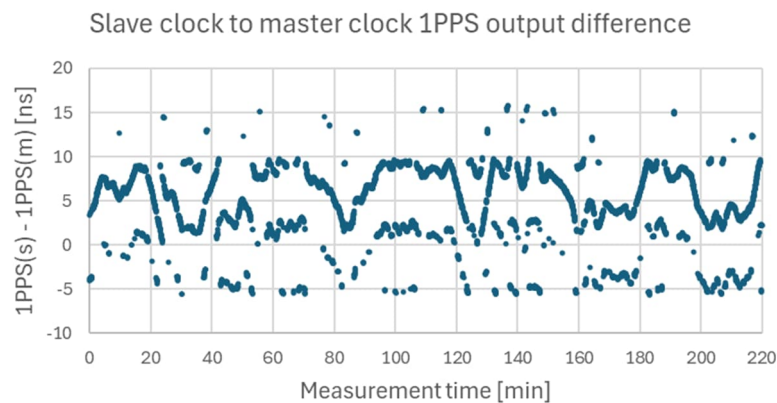


Figure 33. Time interval measurement between master and slave clock 1PPS outputs in setup 2.

The tabulated data first and foremost tells that the clocks in use are as good as they can be in a 100 Mbit/s network. All errors are within the standard deviation of the data. The standard deviation is mostly due to quantization of Layer 1 bit timing, which is visible in both the direct 1PPS measurement in Figure 32 and Figure 33 as well as in individual readings in the data received using the probing method. Both clocks appear to have very low asymmetry, with good repeatability between the measurements performed in the two setups. Master clock internal time, if compared to its 1PPS output is likewise nearly perfect, with a value hardly discernible from zero due to deviation of readings. Slave clock internal time t_s may be calculated in two ways from the probing data: directly from PTP message time tag errors and indirectly from apparent master clock time and slave port asymmetry. Both readings agree within the standard deviation of the data. For calculating slave clock error $t_{1PPS,s}$, the direct method for slave internal time is used. The error is given on the last row in the table. It should be compared to master clock internal time, as in the formula above. The difference between the two clocks is within the standard deviations in both setups, indicating that the clocks work well. Consequently, the comparison shows a clear agreement between the methods, since both methods were utilized to reach the conclusion.

A more interesting comparison case would have been if the clocks performed worse, e.g. if their asymmetries had been large enough to generate an appreciable timing error at the slave device. Adding asymmetry in the link would have accomplished the same. Link asymmetry effect was clearly visible in section 6.5, where a SAMU was calibrated using the probing method to determine master clock error in VTT's calibration setup.

Table 12. Results from the comparison measurements

Property	SETUP 1	SETUP 2
Master clock	clock 1	clock 2
Slave clock	clock 2	clock 1
Asymmetry clock 1	$t_{a,m} = (5.3 \pm 4.1) \text{ ns}$	$t_{a,s} = (7.0 \pm 4.3) \text{ ns}$
Asymmetry clock 2	$t_{a,s} = (3.6 \pm 6.3) \text{ ns}$	$t_{a,m} = (2.2 \pm 4.1) \text{ ns}$
Master clock time $t_m = t_{d,m} = -t_{1PPS,m}$	$(-6.3 \pm 4.1) \text{ ns}$	-3.4 ± 4.1
Apparent master clock time $t'_m = t_m + t_{a,m} = t_{d,m} + t_{a,m}$	$(-1.0 \pm 5.8) \text{ ns}$	-1.2 ± 5.9
1PPS difference slave to master t_{SM}	$(6.2 \pm 5.1) \text{ ns}$	4.5 ± 4.2
Slave clock time		
direct measurement using PTP data $t_s = t_{d,s}$	$(1.1 \pm 6.3) \text{ ns}$	$(-0.3 \pm 4.3) \text{ ns}$
indirect from apparent master clock time $t_s = t'_m - t_{a,s}$	$(-4.6 \pm 8.5) \text{ ns}$	$(-8.5 \pm 7.3) \text{ ns}$
Error based direct measurement + TIC data $t_{1PPS,s} = t_m + t_{SM} - t_s$	$(-1.1 \pm 9.0) \text{ ns}$	$(1.4 \pm 7.3) \text{ ns}$

10 Conclusion and input to standardisation

IEEE 1588-2009 PTPv2 has become a widely accepted standard for synchronizing measurements on a digital substation. Whenever it is used, the timing network inevitably becomes a part of the accuracy and traceability chain for phase displacement measurement data. An analogous situation exists with 1PPS synchronicity, where the timing infrastructure is more accessible and various intermediate devices may be characterized on the field or in a laboratory test setup. While PTPv2 has so far posed an obstacle in traceable calibrations, the Digital-IT project has demonstrated that traceability is possible and, in the end, on a fundamental level the approach is similar to calibrations under 1PPS synchronization. The timing network influence on a calibrated device synchronicity must be determined and taken into account in the calibration result. In a 1PPS case one would define a timing reference plane, which supplies a 1PPS signal to both the reference device and to the DUC. With a proper calibration of the DUC, the phase displacement of the DUC may be determined. In the case of PTP synchronicity, the reference plane should still be defined. But since the time transfer medium is different for both devices, the difference between 1PPS timing for the reference device and PTP synchronicity for the DUC is essential.

Definition of a PTPv2 reference plane with respect to an external 1PPS signal corresponds to calibrating the master clock or master port, which supplies the DUC (slave clock) with its timing data. After a calibrated clock is available, the only remaining influence outside the DUC is the path taken by the PTP data between the master and slave clocks. A high level of symmetry is trivial to provide by using short, equal-length optical fibers or a twister pair cable, with guaranteed (tested) Rx/Tx path delays. In practice, it's nearly impossible to create an appreciable asymmetry in a laboratory setup, where devices are often some meters away from each other. With the two conditions met, the only influence to DUC phase displacement as regard to timing, comes from the DUC itself and is indistinguishable from other implementation errors, which might affect the performance.

Three different methods for calibrating a master clock have been presented in this good practice guide. The methods rely either on determining the master clock output time based on the traffic it sends or on calibrating two similar clocks as a pair. A low-level probing method developed by VTT provides an absolute calibration with low uncertainties but is limited to 100Base-X networks, which are currently used in a process bus implementation between switches and SV transmitting devices. Another traffic-based method developed by RISE uses Linur PTP hardware clocks and suitable network interfaces to obtain the same data. VSL's method on the other hand lends itself to various network speeds and physical media if suitable clocks supporting the requirements are available.

While national metrology institutes may use highly customized and sometimes cumbersome methods for traceable calibrations with lowest uncertainties, a calibration laboratory or even an in-house testing department at a protection equipment manufacturers location may prefer a simpler method. Any wider acceptance of newly developed calibration method should be backed by a clear requirement in standardization. This would cause a demand from calibration labs by their customers and a clear business case, which helps justify investment in developing calibration services. A governing standard should therefore not only set the requirements, but also suggest best practices, such as in IEC 61869-1 for analog output ITs and LPITs, and in IEC 61869-9 for digital output LPITs.

The digital output for LPITs is defined in IEC 61869-9 along with test circuits using two different reference measurement chains in Annex 9D. The 2016 version of the standard suggests using IEC 61850-9-3 for time synchronicity, but omits its implications to phase displacement. The test setups in the annex are ambiguous as regards to the type of time synchronization signal. Based on the work presented in this good practice guide, IEC TC 38 might be able to introduce a more detailed explanation in the annex as to how a calibration should be performed under PTPv2 synchronicity. For a test laboratory or any other actor, the only requirement would be to build a test setup around a calibrated PTP master clock. As is usual, the traceability for the clock could come from a national metrology laboratory, who could leverage the methods presented here. While no data exists yet, it is foreseen that a master clock, itself locked to a traceable, stable time source, would have no long-term drift. The clock calibration would therefore be a one-off event.

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