

# RF Rectifier with Pixel-like Network and Inductive Matching Technique

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**Abstract**— This paper demonstrates an RF rectifier employing a pixel-like network and an inductive matching technique. The pixel-like network acts as an RF choke and is more compact compared to a typical  $\lambda/4$  transmission line with open/short stubs. A pattern generator is developed in Python to create pixel-like networks. The main constraint for the pixel-like network used in a rectifier is to ensure dc current flow, which requires a certain overlap between pixels when generating the network. The design is fabricated on a Rogers RO4350b substrate with a total size of 2.8 cm<sup>2</sup>. Measured peak efficiency is 73.3% at 2.5 GHz with an input power of 23.5 dBm and a dc output voltage of 8 V. Measured efficiency remains above 50% from 1.88 GHz to 3.26 GHz for an input power of 22.3 dBm.

**Keywords**— Pixel-like network, computer-aided design, Voltage-doubler rectifier, Wireless power transmission, Inductive matching technique

## I. INTRODUCTION

Straight microstrip lines are typically used to perform impedance transformation in many RF/microwave PCB circuit designs. Thanks to high computing power, accurate electromagnetic (EM) simulation and machine learning (ML), the realisation of arbitrary geometries has become possible. The arbitrary geometry in this paper is referred to as pixel-like network. Some examples of such RF/microwave designs include antennas [1], passive components [2], [3], and amplifiers [4].

To obtain a highly-efficient rectifier, proper input matching and harmonic-control are employed to minimise the energy loss and to obtain high matching efficiency [5]. Some approaches for this purpose have been proposed and demonstrated such as Class C [6], Inverse Class-F network [7], bandstop filtering [8], inductive-matching [9].

In this paper we attempt to validate the use of the pixel-like network together with the inductive matching network to realise a highly-efficient RF rectifier. The main constraints in the pixel-like network for a rectifier are: 1) each pixel must touch another with a certain overlap to allow dc current flow, and 2) it must fit within the size boundaries. Such a pixel-like network should offer advantages such as being more compact than a typical microstrip-line approach.

## II. CIRCUIT DESIGN

The schematic of the proposed pixel-like RF rectifier is illustrated in Fig. 1. It consists of two Schottky diodes,  $D_1$

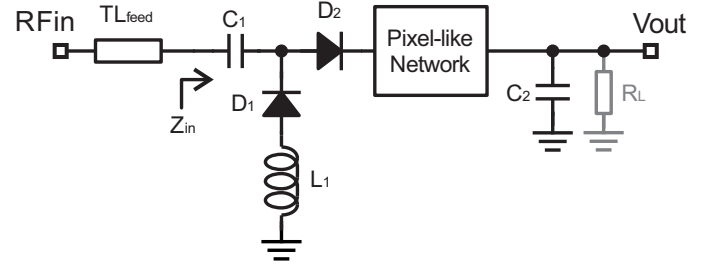


Fig. 1. Schematic of the proposed pixel-like rectifier.

and  $D_2$ , and two capacitors,  $C_1$  and  $C_2$ , serving as charge pumps, an inductor,  $L_1$ , and a pixel-like network acting as an RF choke. A characteristic-impedance of  $50\Omega$   $TL_{\text{feed}}$  is used for the connector only. The dc load,  $R_L$ , is intentionally not attached to mimic the operation of a power management IC (PMIC). A Greinacher voltage-doubler configuration is employed to obtain sufficient dc output voltage.

A pattern generator is used to create the pixel-like network. Since the network will be used in a rectifier, establishing a dc connection is essential. This requirement leads to the unique property and the most important constraint: each pixel must touch another with a certain overlap within the given boundary. A pixel-like network consists of  $11 \times 11$  pixels. The physical dimension of each pixel corresponds to  $1.0\text{ mm} \times 1.0\text{ mm}$  and the overlap between two pixels is set to be  $0.3\text{ mm}$ . The overlap size is limited by the fabrication resolution. An additional pixel is added at both the leftmost and rightmost positions as fixed feeding points, defined as Port 1 and Port 2. An example of the pixel-like network is shown in Fig. 2, illustrating its structure and layout. This results in an actual length of  $11.3\text{ mm}$  for the complete pixel-like network, which is shorter than a  $\lambda/4$  transmission line at  $2.4\text{ GHz}$ . Algorithm 1 describes the proposed pattern generator. In the algorithm, 0 and 1 indicate the absence or presence of metal in a pixel, respectively. The network density, defined as the ratio of occupied pixels to the total number of pixels in the network, can be controlled. The pattern generator is implemented in Python and it outputs PNG, DXF format files as well as an ADS AEL script, simultaneously.

In total 100 pixel-like networks are created which can be

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**Algorithm 1** Generate pixel-like network

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**Require:** pixel\_size (default: 11x11), n (default: 100), start\_end (coordinates), density threshold  
**Ensure:** List of unique binary matrices  
**while**  $i \leq n$  **do**  
    Initialise pixel with starting cell set to "1".  
    **while** pixel not connected to the ending cell **do**  
        Get neighbouring cells of the current cell.  
        **if** surrounding cells = "0" **then**  
            Randomly select a cell and set to "1".  
        **else**  
            Randomly select a cell with value "1".  
        **end if**  
    **end while**  
    Check the generated network  
    **if** structure is not unique or density is insufficient **then**  
        Regenerate network  
    **end if**  
**end while**

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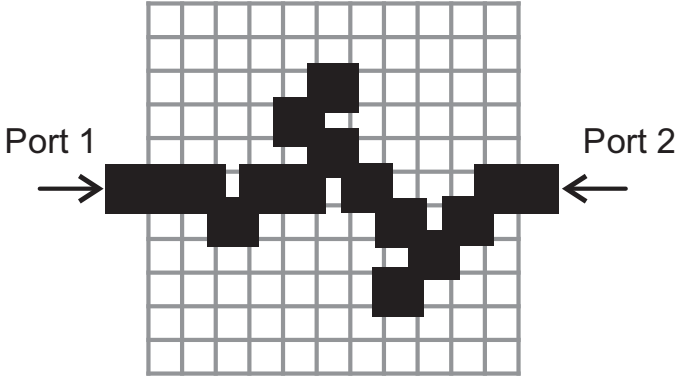


Fig. 2. Example of a pixel-like network. Grid indicates the design space.

simulated in EM simulators, *e.g.* Sonnet or Keysight ADS Momentum. In this work, Keysight ADS Momentum is used to carry out the EM simulations for all the generated networks. For convenience, AEL scripts are loaded directly to perform the simulations.

The simulation and optimisation are performed in Keysight ADS also. The diode model and the S2P file of the lumped capacitor are included in the complete schematic, as shown in Fig. 1. The DataAccessComponent (DAC) is employed to access the simulated EM results of the pixel-like networks. The inductance,  $L_1$ , is used to achieve the matching condition for this design and it is optimised along with the pixel-like networks.  $L_1$  is implemented using a short stub with a fixed width of 0.5 mm matching the width of the diode package. The length of  $L_1$  is one of the optimisation variables. The optimisation goal is set to achieve an efficiency above 70% at the centre frequency. There may be multiple combinations of pixel-like networks and lengths of the short stub. Among these combinations, the one with the highest efficiency is selected for the implementation.

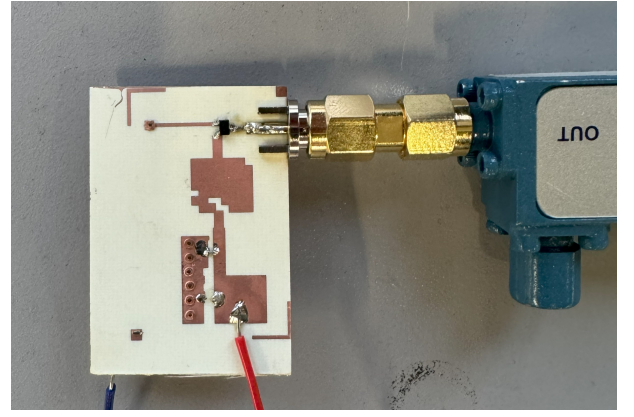


Fig. 3. Photograph of the rectifier.

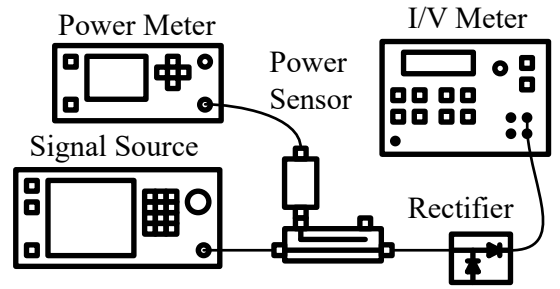


Fig. 4. Illustration of the measurement setup used for evaluating rectifier performance.

### III. IMPLEMENTATION AND MEASUREMENT

The design is fabricated on a Rogers<sup>®</sup> RO4350b substrate with a thickness of 0.7 mm, a relative permittivity,  $\epsilon_r$ , of 3.65, a loss tangent of 0.0031, and a copper thickness of 17  $\mu\text{m}$ . BAT-68 Schottky diodes from Infineon Technologies<sup>®</sup> are employed.  $L_1$  is implemented with a width of 0.5 mm and a length of 8.7 mm microstrip line with a ground via.  $C_1$  and  $C_2$  with a normal value of 10 pF are from the Murata<sup>®</sup> GQM series. The fabricated PCB is shown in Fig. 3 and the size is 2.8 cm<sup>2</sup>. It can be further reduced by replacing  $L_1$  to a lumped inductor or meandering it.

An RF signal generator (SG), R&S SMBV 100, and a Yokogawa dc meter are employed to carry out the measurement. A 10-dB directional coupler and a Keysight E4418B power meter with an RF power sensor are employed to measure the exact input power to the rectifier. Fig 4 shows the measurement setup. The centre frequency of the RF signal is 2.5 GHz and the dc output voltage is fixed by the dc meter to resemble a PMIC.

Simulated and measured efficiencies versus input power are shown in Fig. 5 with dc output voltages from 4 V to 8 V at a frequency of 2.5 GHz. At an input power of 23.5 dBm peak efficiency of 73.3% with a dc output voltage of 8 V is measured. Measured efficiency of more than 60% is reached for an input power between 15.5 dBm and 22.4 dBm with a dc output voltage of 4 V.

Fig. 6 plots the efficiency versus frequency for an input power of 22.3 dBm, 22.9 dBm, and 23.4 dBm. At an

Table 1. Comparison of diode-based voltage-doubler rectifiers.

Ref.	Topology	Freq. (GHz)	Peak Eff. (%)	Input power (dBm)	Diode	Size (cm <sup>2</sup> )
[10]	Greinacher	2.4	65.3	8	SMS7630	4
[11]	Greinacher	2.45	54.2	7	SMS7630	20.8*
[12]	Greinacher	1.85	71	4.7	HSMS-285C	49
[13]	Greinacher	2.4	47.4	12.9	HSMS-286C	17.5*
[14]	Greinacher	2.5	76.5	23.9	BAT-68	8
[15]	Diode array	2.4	69.4	30	HSMS-282P	30
<b>This Work</b>	<b>Greinacher</b>	<b>2.5</b>	<b>73.3</b>	<b>23.5</b>	<b>BAT-68</b>	<b>2.8</b>

\* Antenna included \*\* Estimation from figures

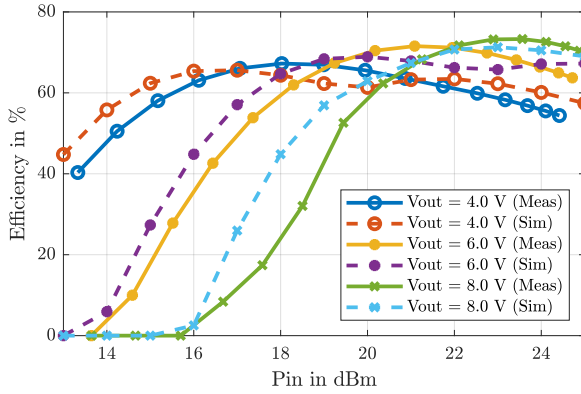


Fig. 5. Simulated and measured efficiency versus input power with various dc output voltages.

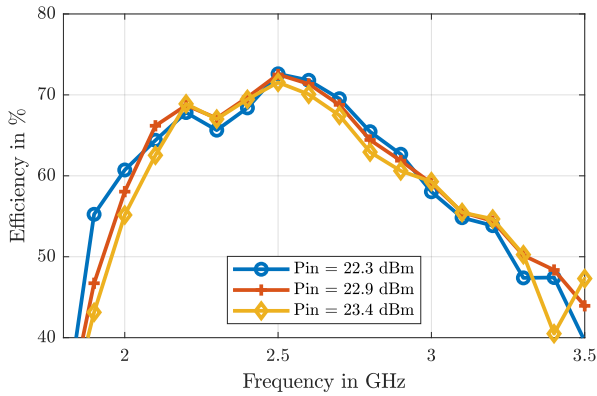


Fig. 6. Measured efficiency versus input frequency with various input power.

input power of 22.3 dBm, the widest bandwidth is achieved. Measured efficiency is higher than 50% from 1.88 GHz to 3.26 GHz at an input power of 22.3 dBm.

Table 1 summarises the performance of the rectifier and other voltage-doubler diode-based rectifiers. It presents a competitively high efficiency above 70% in a small form factor.

#### IV. CONCLUSION AND OUTLOOK

In this paper, we have successfully demonstrated a highly-efficient RF rectifier utilising a pixel-like network in conjunction with an inductive matching technique. The pixel-like network pattern generator has been developed and validated. To the best of the authors' knowledge, this is the first demonstration of a pixel-like rectifier to date. The rectifier achieves a peak efficiency of 73.3% at dc output voltage of 8 V showcasing its potential for wireless power transmission applications. The approach leverages advanced computational tools for pattern generation and optimisation, highlighting the role of computer-aided design techniques in pushing the boundaries of RF/microwave circuit performance.

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