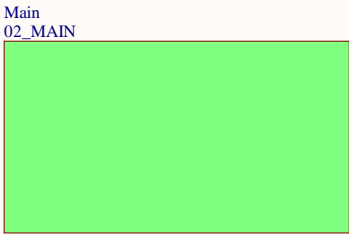
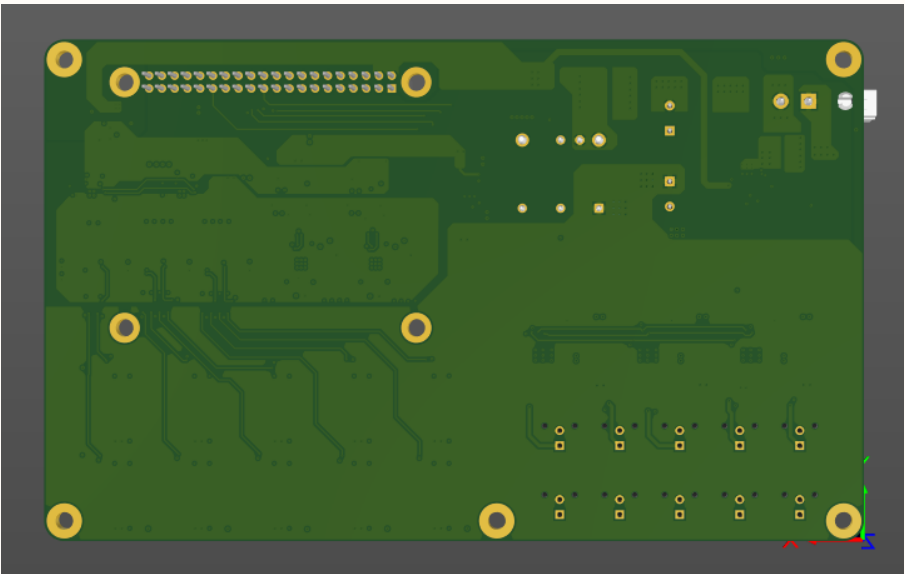
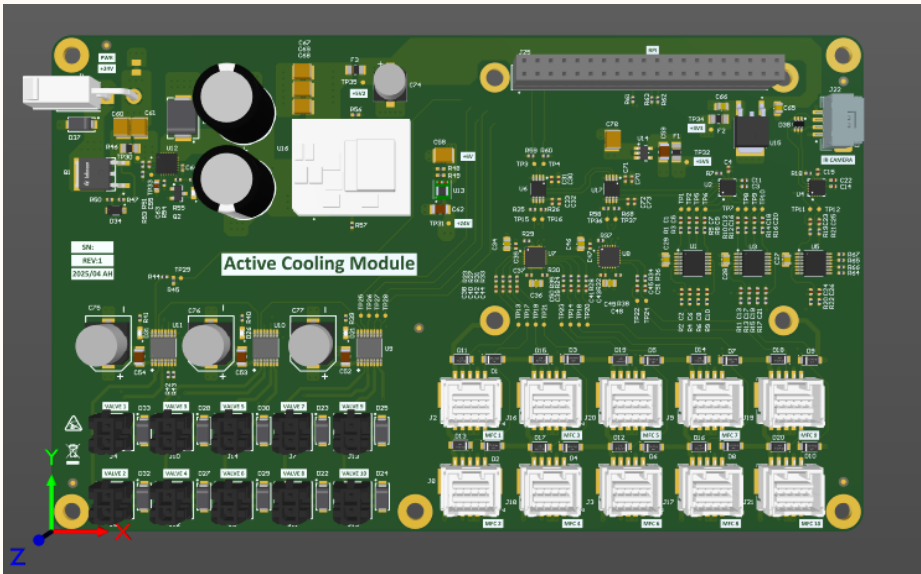


# Active\_Cooling.PrjPcb

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4	MFC_DAC
5	SOLENOID DRIVER
6	POWER SUPPLY
7	CONNECTORS, MECHANICAL
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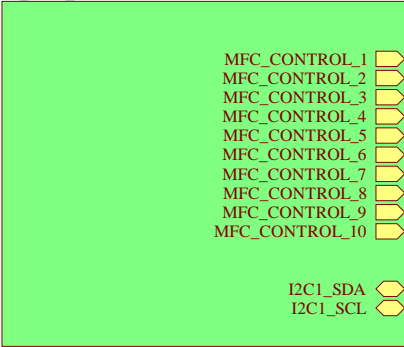
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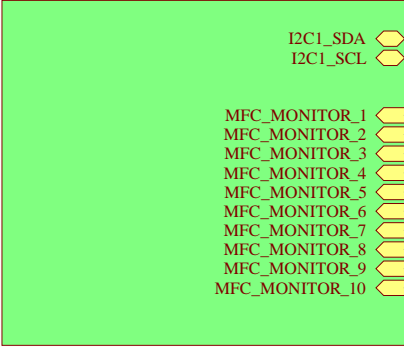


Revision 1	Project Name: Active_Cooling.PrjPcb	Project #: A1-023378-02
	Title: COVER_PAGE.SchDoc	Date: 3/5/2025
Research Center IEP	Drawn By: Antoine Hamel	Sheet 1 of 7
	75 Boul de Mortagne Boucherville J4B 6Y4 Canada	

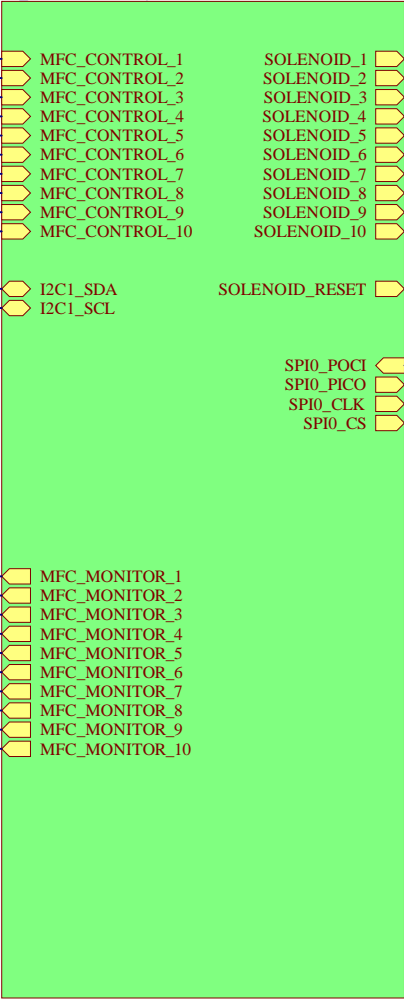
MFC\_DAC  
04\_MFC\_DAC.SchDoc



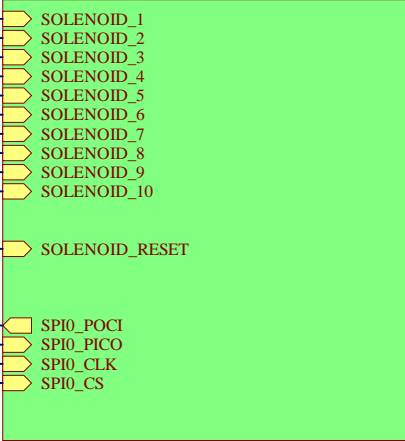
MFC\_ADC  
03\_MFC\_ADC.SchDoc



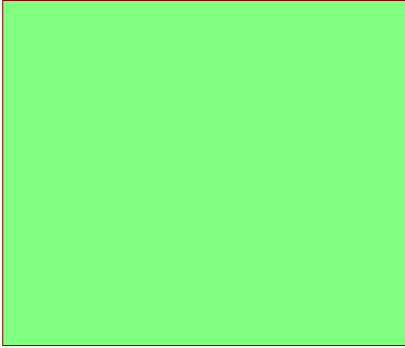
CONNECTORS,MECHANICALS  
07\_CONNECTORS.MECHANICALS



SOLENOID DRIVER  
05\_SOLENOID\_DRIVER.SchDoc

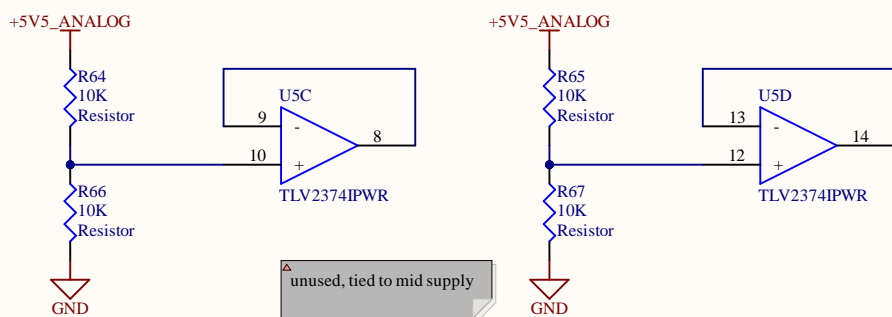
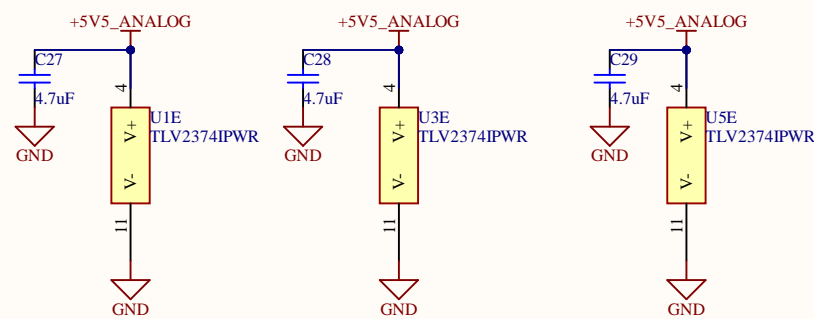
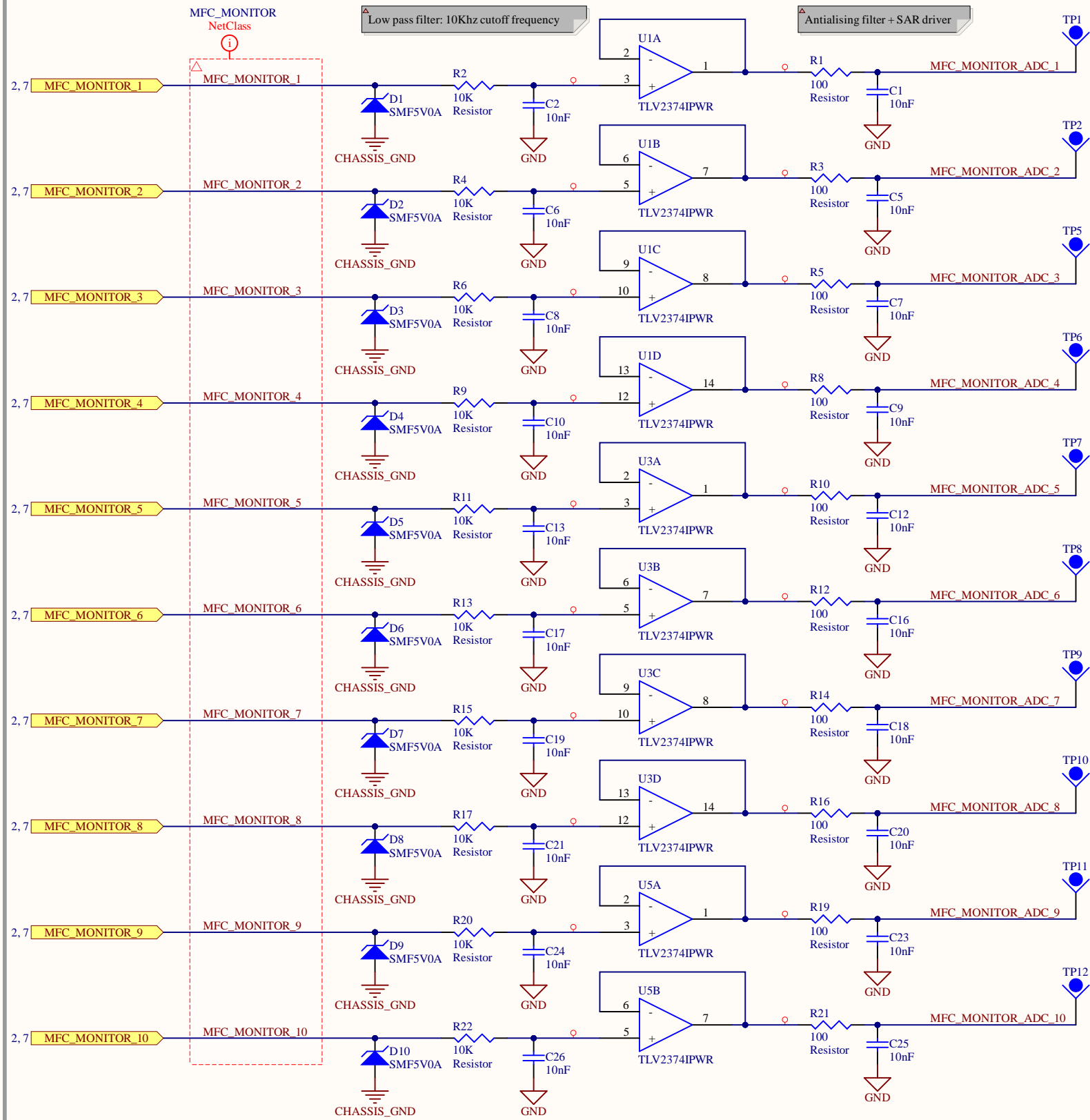


POWER\_SUPPLY  
06\_POWER\_SUPPLY



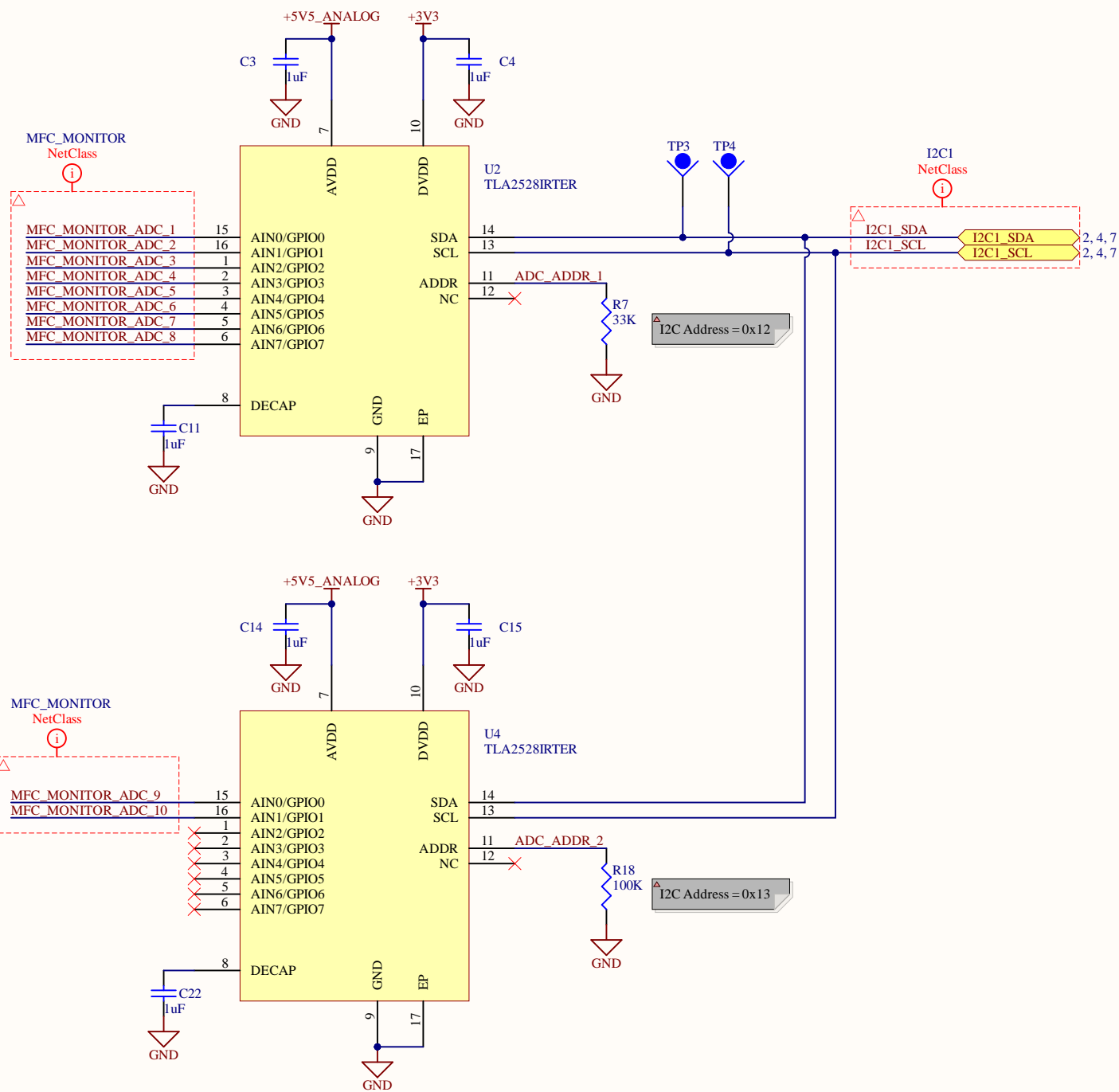
Revision  1	Project Name: Active_Cooling.PrjPcb	Project #: A1-023378-02
	Title:02_MAIN.SchDoc	Date: 3/5/2025
Research Center  IEP	Drawn By: Antoine Hamel	Sheet 2 of 7
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# BUFFERS



<sup>A</sup>ADC sampling capacitance = 12pF  
 ADC internal series resistance = 150ohm  
 $\tau = R \cdot C = (100\text{ohm} + 150\text{ohm}) \cdot (10\text{nF} + 12\text{pF}) = 2.5\mu\text{s}$   
 Number of Time Constants to settle within 1LSB :  
 $-\ln(1/4096) = 8.32\tau$   
 Settling time =  $8.32 \cdot \tau = 20.8\mu\text{s}$   
 Max sampling rate =  $1/20.8\mu\text{s} = 48\text{KHz}$   
 $f_z = 1/(2\pi \cdot R \cdot C) = 159\text{KHz}$

# ADC



## Design Information:

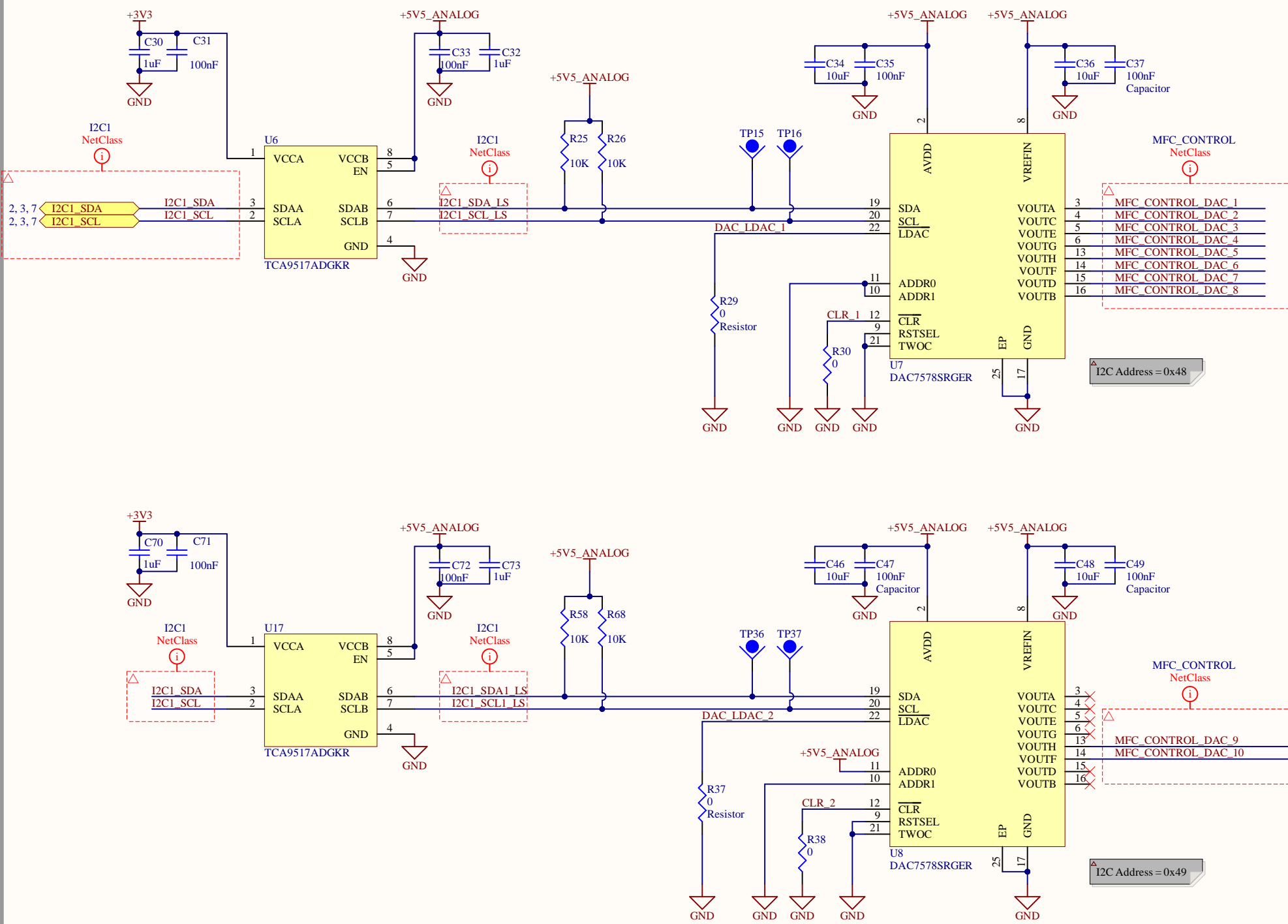
- MFC monitor are analog signals that should be kept clean

## Layout Considerations:

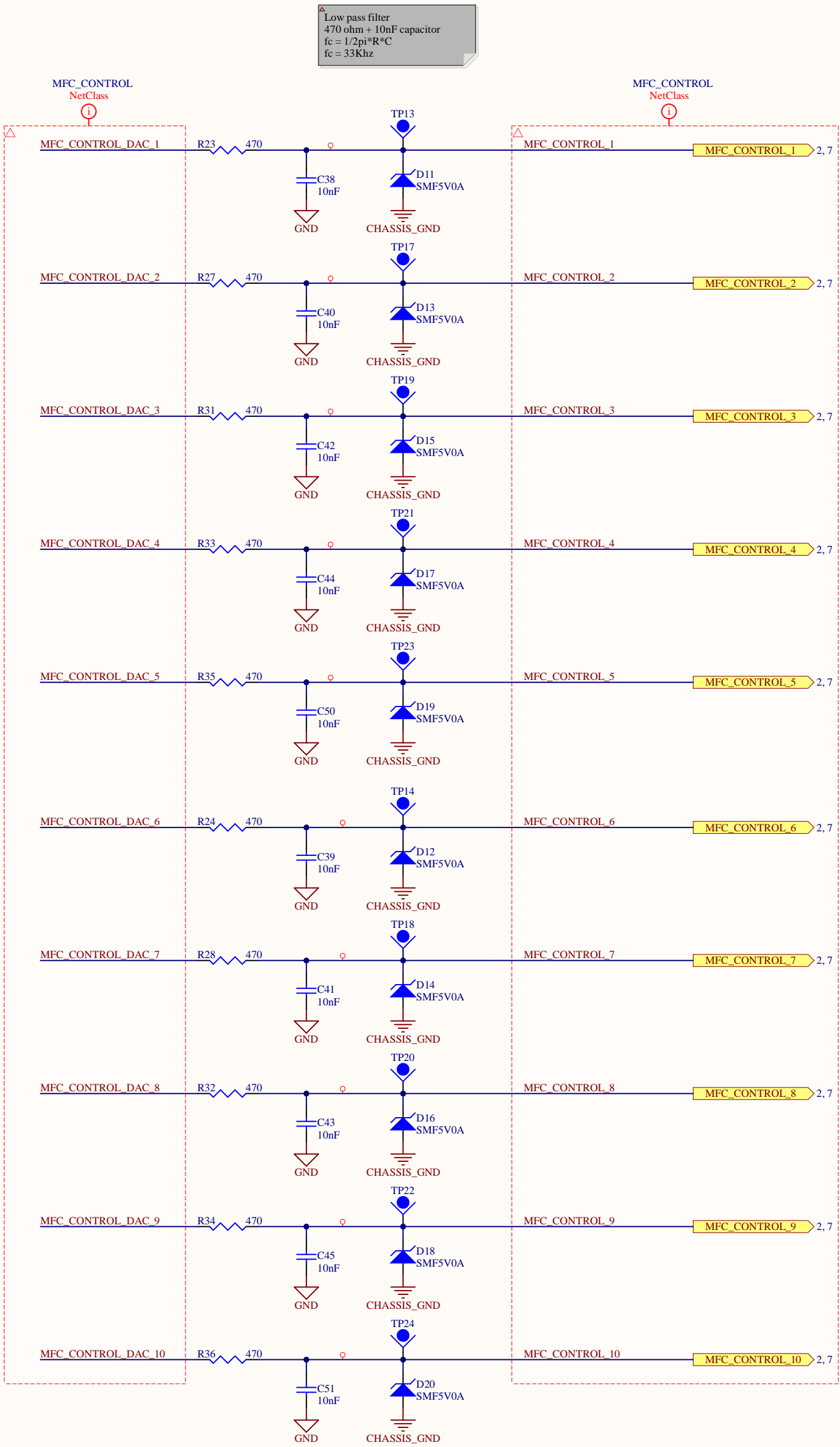
- Route sensitive analog signal away from digital or fast switching signals
- Route analog signals close to 50ohm impedance
- Place ESD diodes close to input connectors and connect to chassis ground near a chassis connection point

Revision 1	Project Name: Active_Cooling.PjPcb	Project #: A1-023378-02
	Title: 03_MFC_ADC.SchDoc	Date: 3/5/2025
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IEP	75 Boul de Mortagne Boucherville J4B 6Y4 Canada	
	MRC-CMRC	

DAC



FILTERING+ PROTECTION



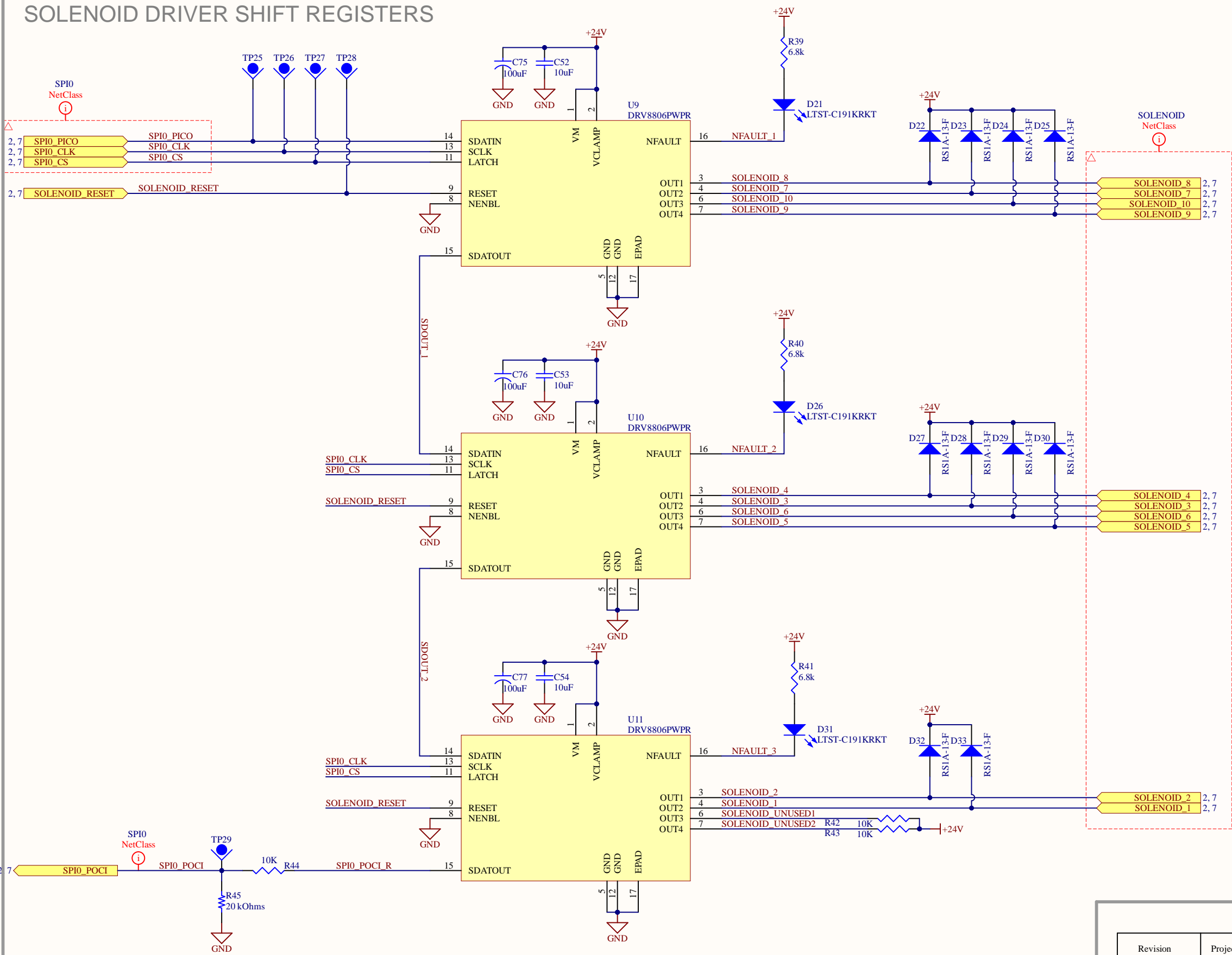
**Design Information:**

- MFC control are analog signals that should be kept clean

**Layout information:**

- MFC control are analog signals that should be kept clean
- Route analog signals close to 50ohm impedance
- Place ESD diodes close to output connectors and connect to chassis ground near a chassis connection point

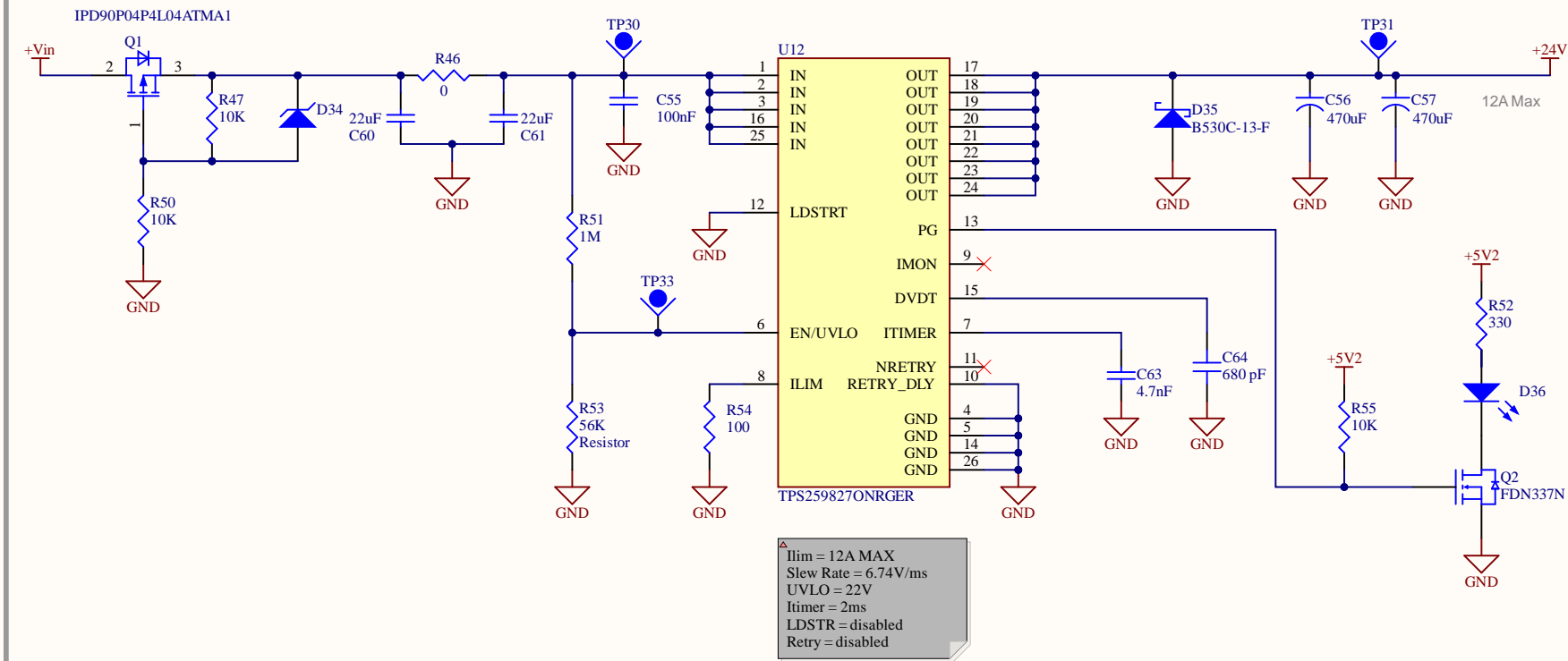
SOLENOID DRIVER SHIFT REGISTERS



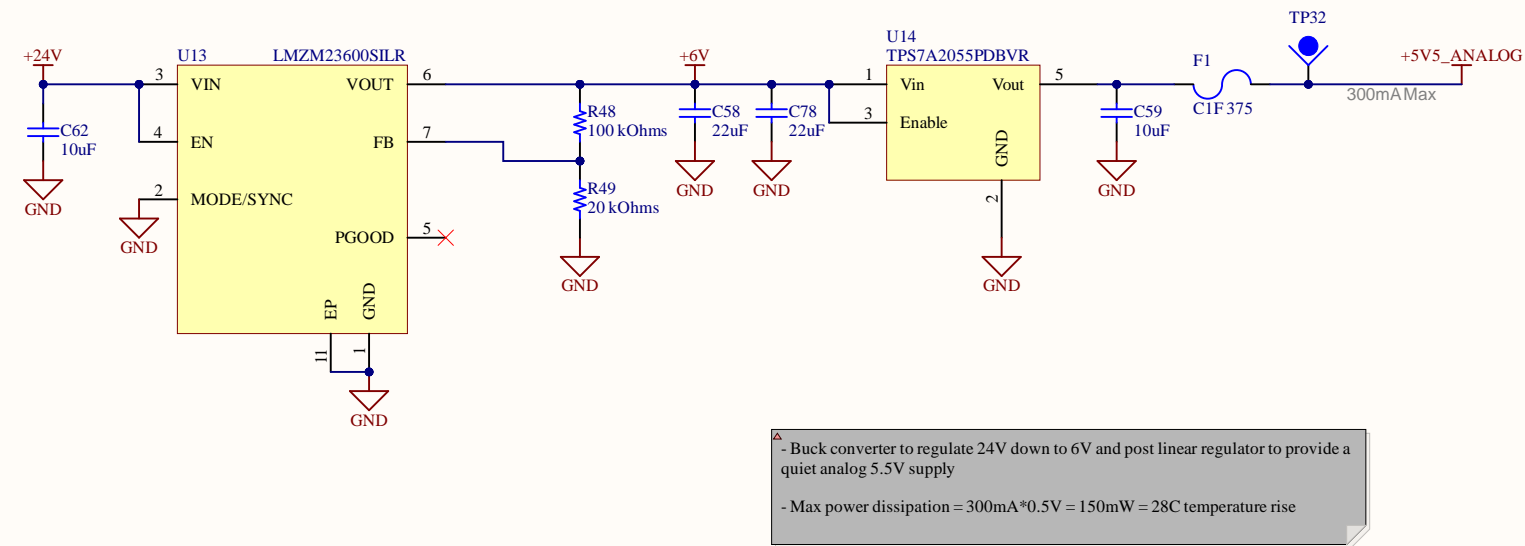
- Layout Considerations:
- Solenoid driver traces should be wide enough to carry max operating current of solenoid valves (0.5A)
  - Place free wheeling diode close to connector
  - Place thermal vias to properly heatsink the DRV8806 ICs

Revision 1	Project Name: Active_Cooling.PrjPcb	Project #: A1-023378-02
	Title:05_SOLENOID_DRIVER.SchDoc	Date: 3/5/2025
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## POWER INPUT + PROTECTION



## 5V ANALOG



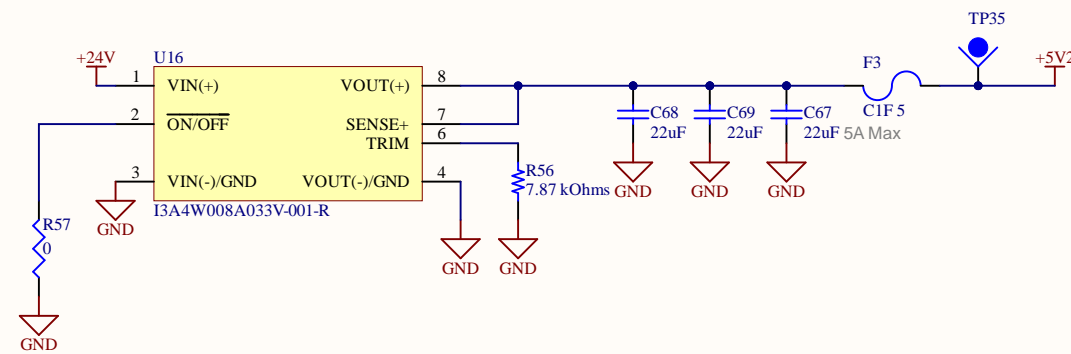
**Design Considerations:**

- Here I am using a 5.5V analog voltage to ease calculations and reference voltage for ADC and DAC. However the RAIL to RAIL ADs and OPAMP won't be able to reach true 5V (closer to 4.9V real world).

I assume that the end of the MFC control won't be required but that might be a wrong assumption. If the end of range required the fix is easy, one can simply swap TPSTA2050PDBVR with the TPSTA2055PDBVR (pin compatible) which will bring the analog rail to 5.5V instead and allow a true full 0-5V control and monitoring voltages

- Always consult datasheet and follow recommend layout for all DC-DC converters and modules

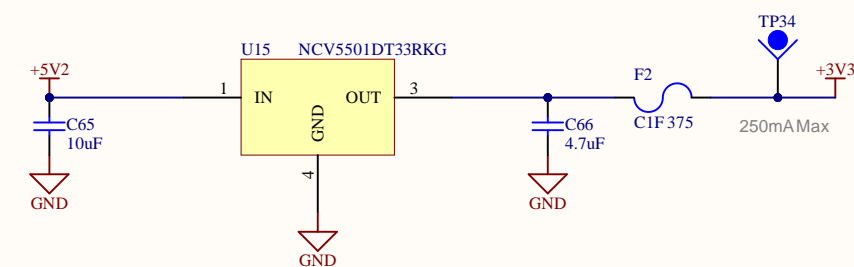
## +5V DIGITAL RAIL




Max power dissipation = 1.9W Worst case scenario. We don't expect to go near 5A at all.

Vout is adjusted to 5.2V with Trimresistor to power the RPI. 5.2V is recommend when powering the RPI through the header pins as recommended in the various forum discussions and documentation

## +3V3 DIGITAL RAIL

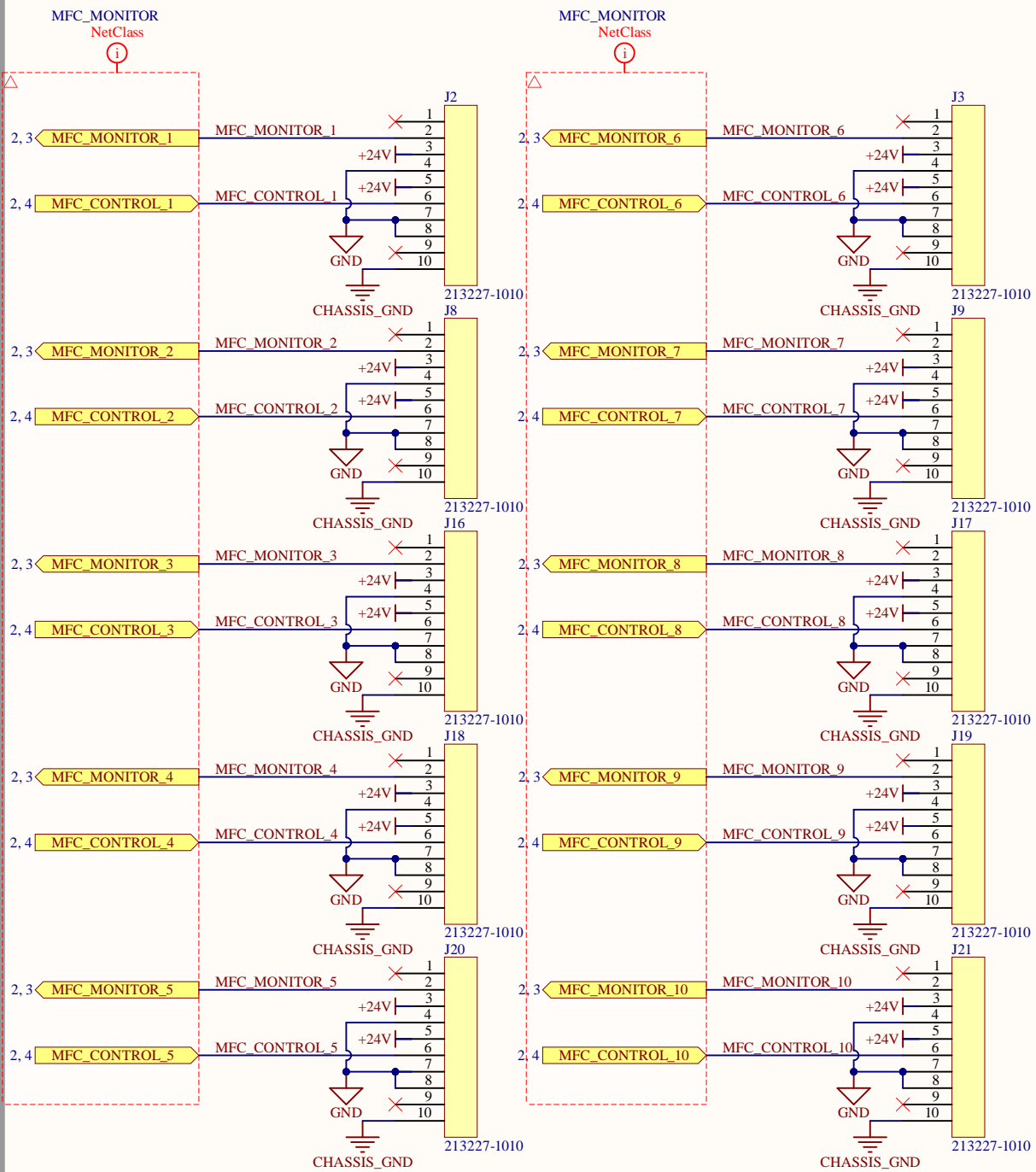


- Buck converter to regulate 24V down to 6V and post linear regulator to provide a quiet analog 5.5V supply
- Max power dissipation =  $1.9V \cdot 250mA = 0.475W = 28.5C$  temp rise

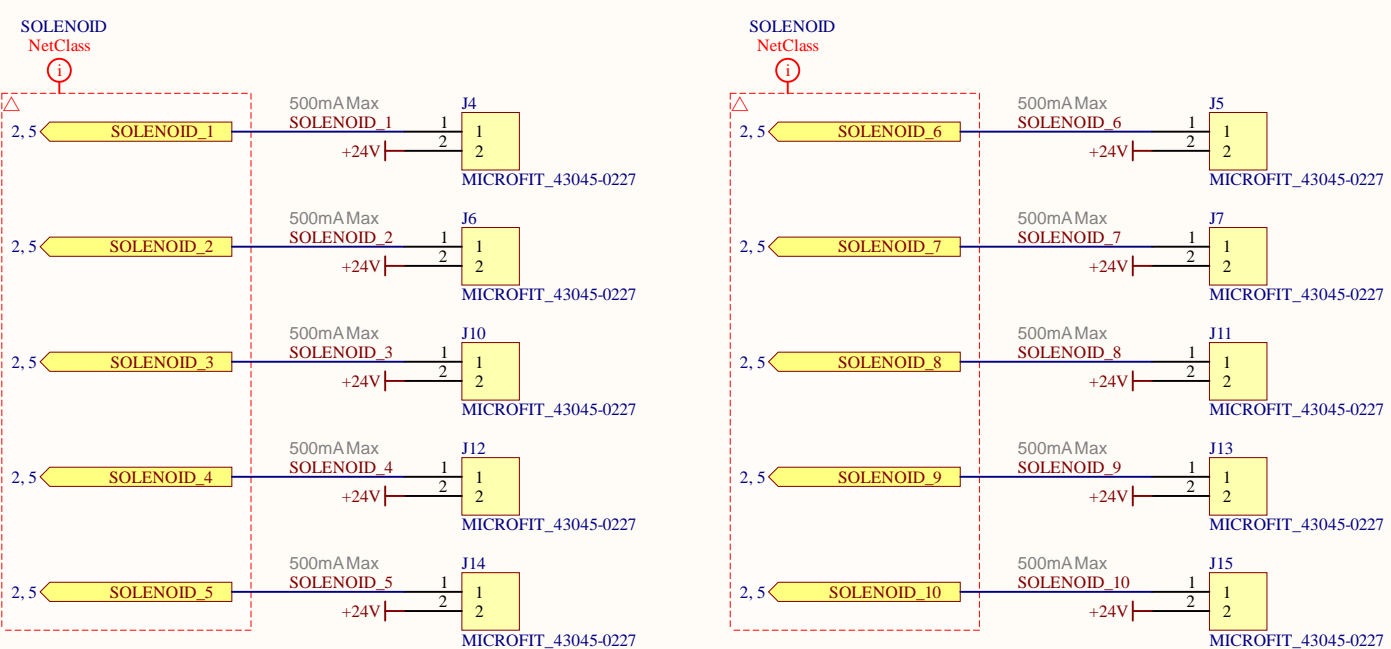
Revision 1	Project Name: Active_Cooling.PjtPch		Project #: A1-023378-02
	Title: 06_POWER_SUPPLY.SchDoc		Date: 3/5/2025
Research Center	Drawn By: Antoine Hamel		Sheet 6 of 7
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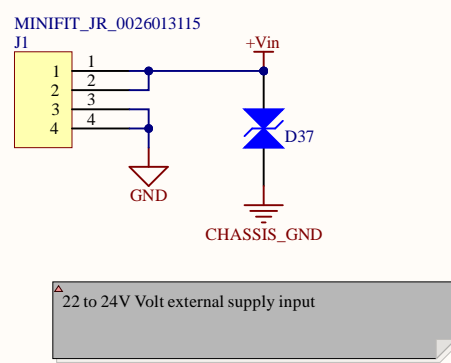
MFC\_CONNECTORS



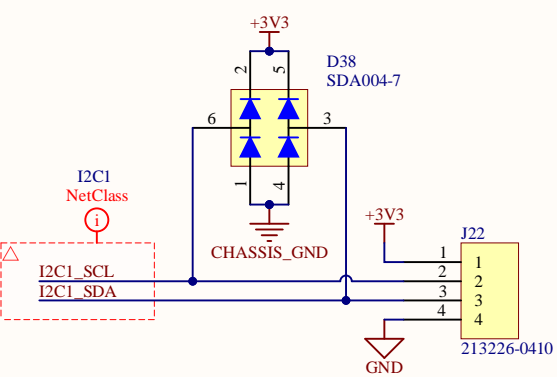
SOLENOID\_CONNECTORS



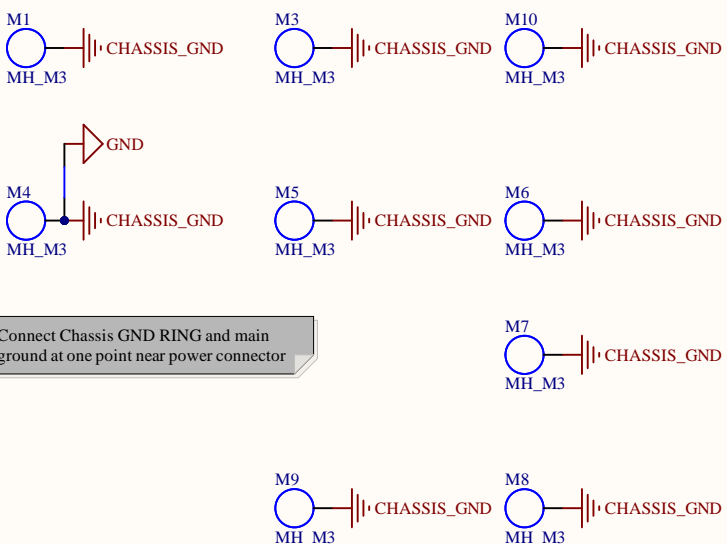
POWER\_CONNECTOR



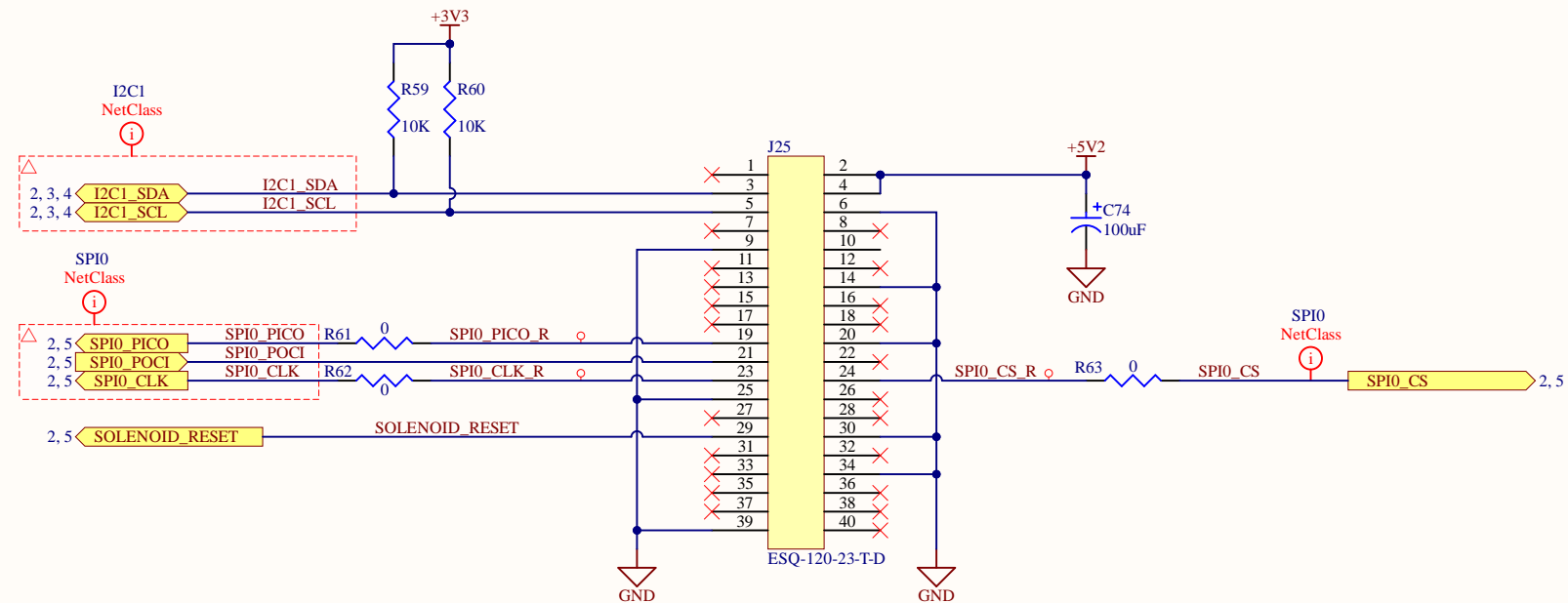
IR CAMERA



MOUNTING HOLES



RASPBERRY PI CONNECTOR



Design Information:

- MFC control are analog signals that should be kept clean

Layout information:

- Place a chassis GND ring around the edge of the PCB and connect it with all mountings holes. Also connect Chassis GND and Gnd plane at one location near the input power supply
- Place mounting holes for rapsberry pi header
- keep in mind that Rpi will be on top in the stack compared to usual hat where Rpi is on bottom

Revision 1	Project Name: Active_Cooling.PjPcb	Project #: A1-023378-02
	Title:07_CONNECTORS,MECHANICALS.SchDoc	Date: 3/5/2025
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	75 Boul de Mortagne Boucherville J4B 6Y4 Canada	<b>MRC-CMRC</b>