

# Supplemental Material – Multi-Objective Memory Bandwidth Regulation and Cache Partitioning for Multicore Real-Time Systems

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## Abstract

In this supplemental material, we present the slowdown plots for all 43 benchmarks profiled in the SD-VBS suite and all 20 benchmarks profiled in the PARSEC suite. These profiles are generated by varying the number of memory bandwidth partitions and cache partitions. Slowdown is calculated as the ratio of the benchmark's execution time with the tested memory bandwidth and cache allocation to its execution time with full memory bandwidth and cache allocation. The slowdown is plotted on a log scale, with the x-axis representing the number of memory bandwidth partitions and the y-axis representing the number of cache partitions. Slowdown values under extreme memory bandwidth and cache partition allocations are annotated at the corners of each plot.

Some benchmarks cannot be completed with certain cache allocations (e.g., with only one cache partition), and their corresponding slowdown values are left blank (white in the heatmap). The benchmarks are ordered alphabetically.

**2012 ACM Subject Classification** Computer systems organization → Real-time systems; Computer systems organization → Embedded software

**Keywords and phrases** Multi-objective optimization, memory bandwidth regulation, cache partitioning, partitioned scheduling, real-time systems

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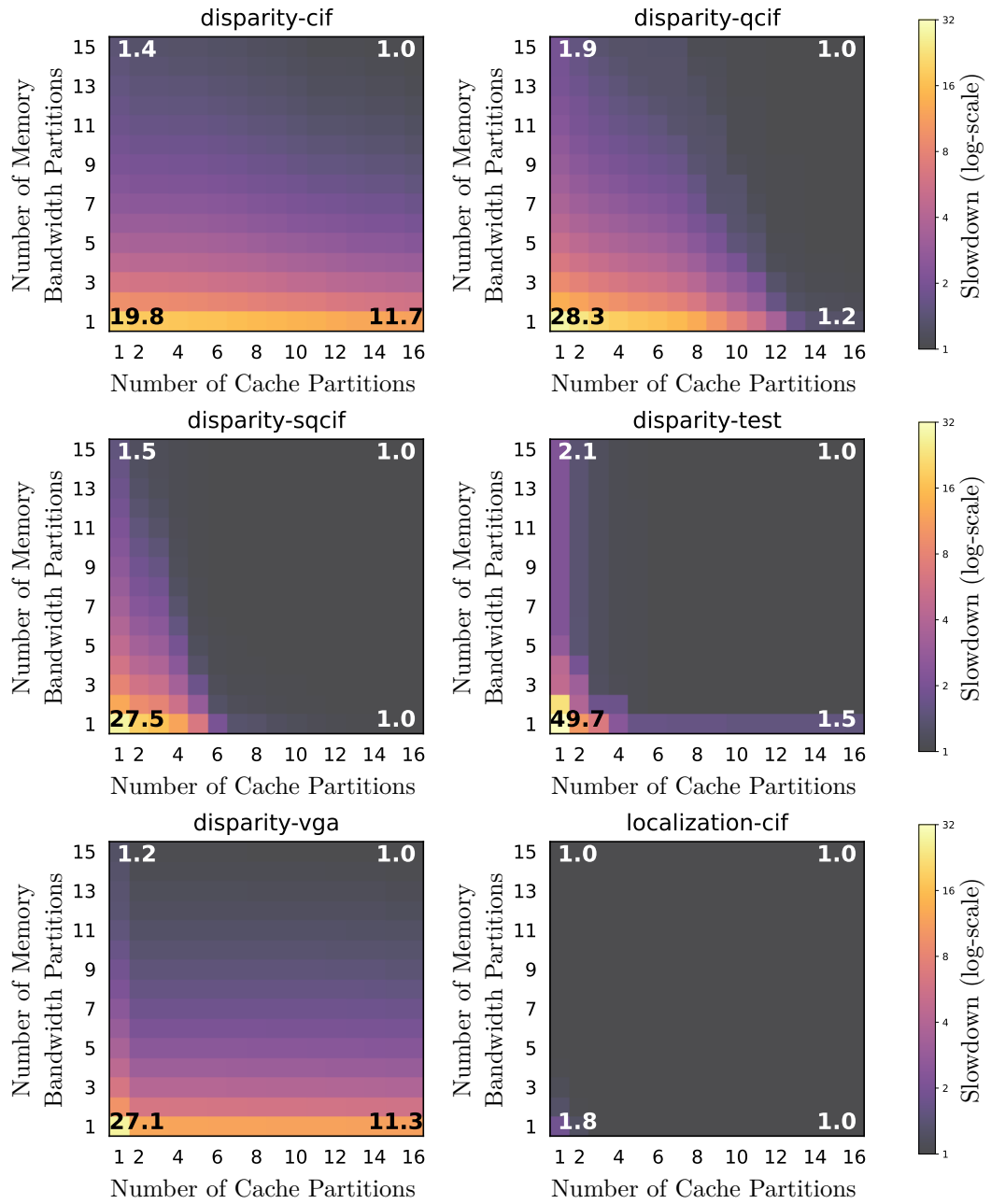
Editor: Renato Mancuso; Article No. 7; pp. 7:1–7:12

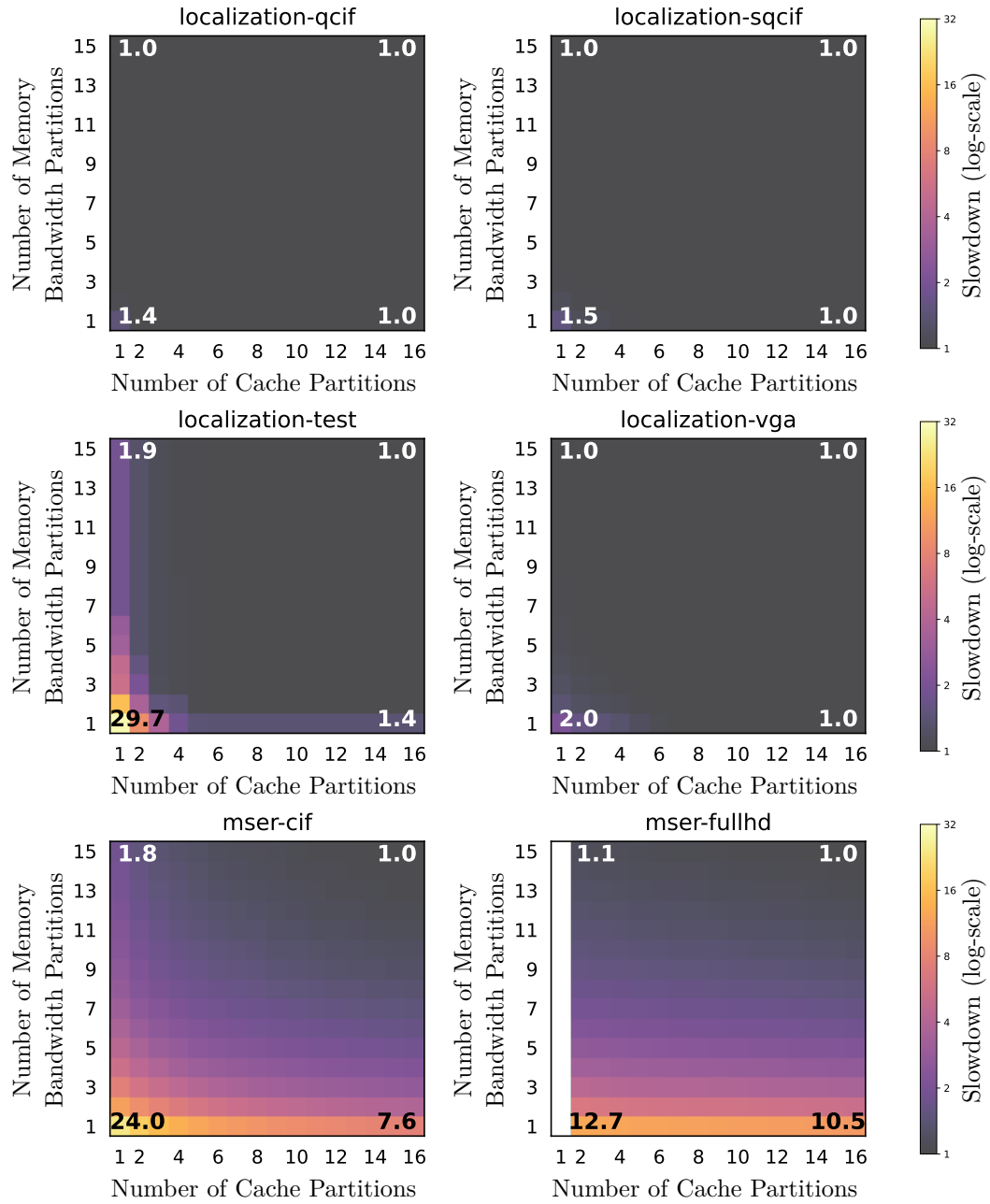


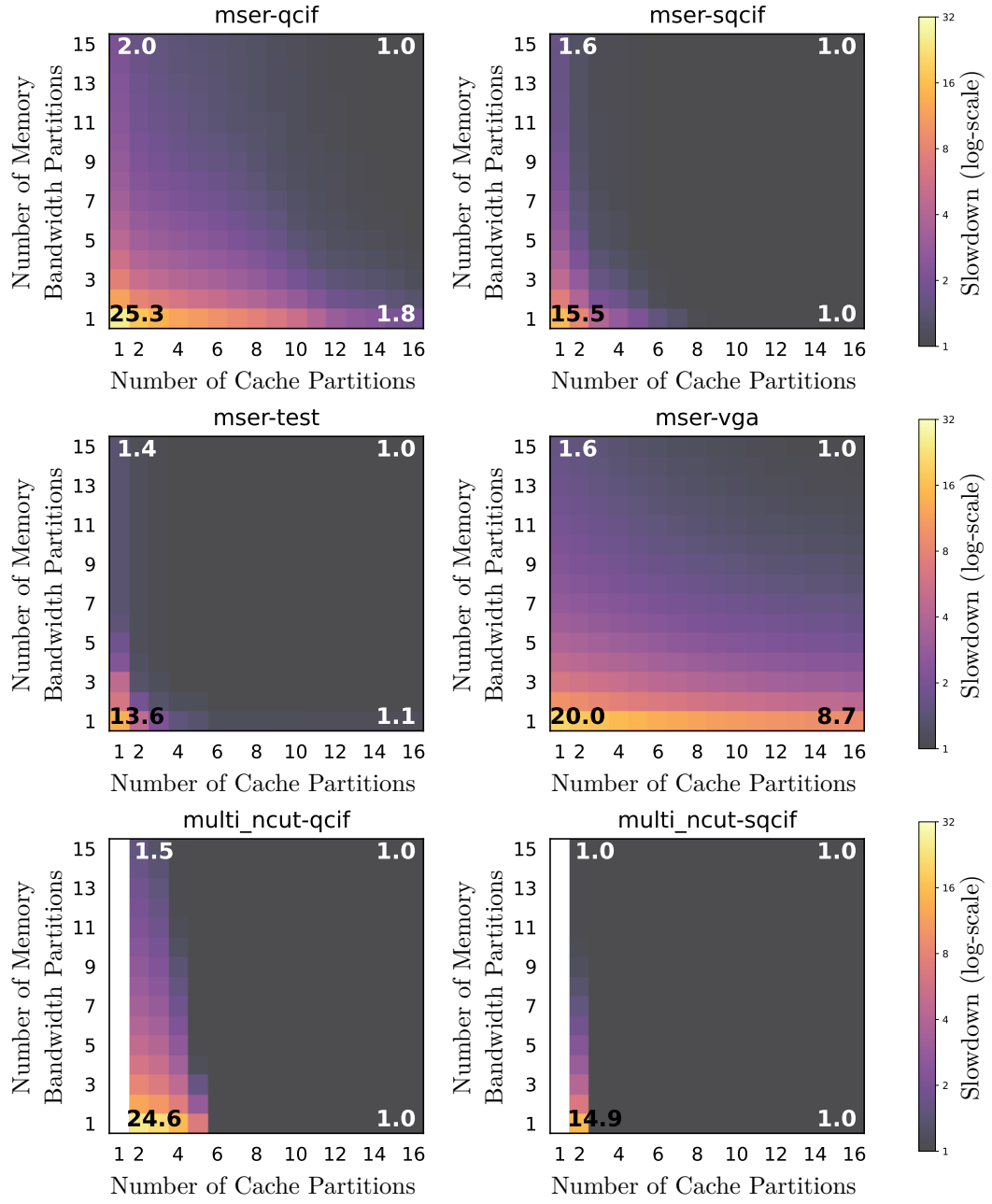
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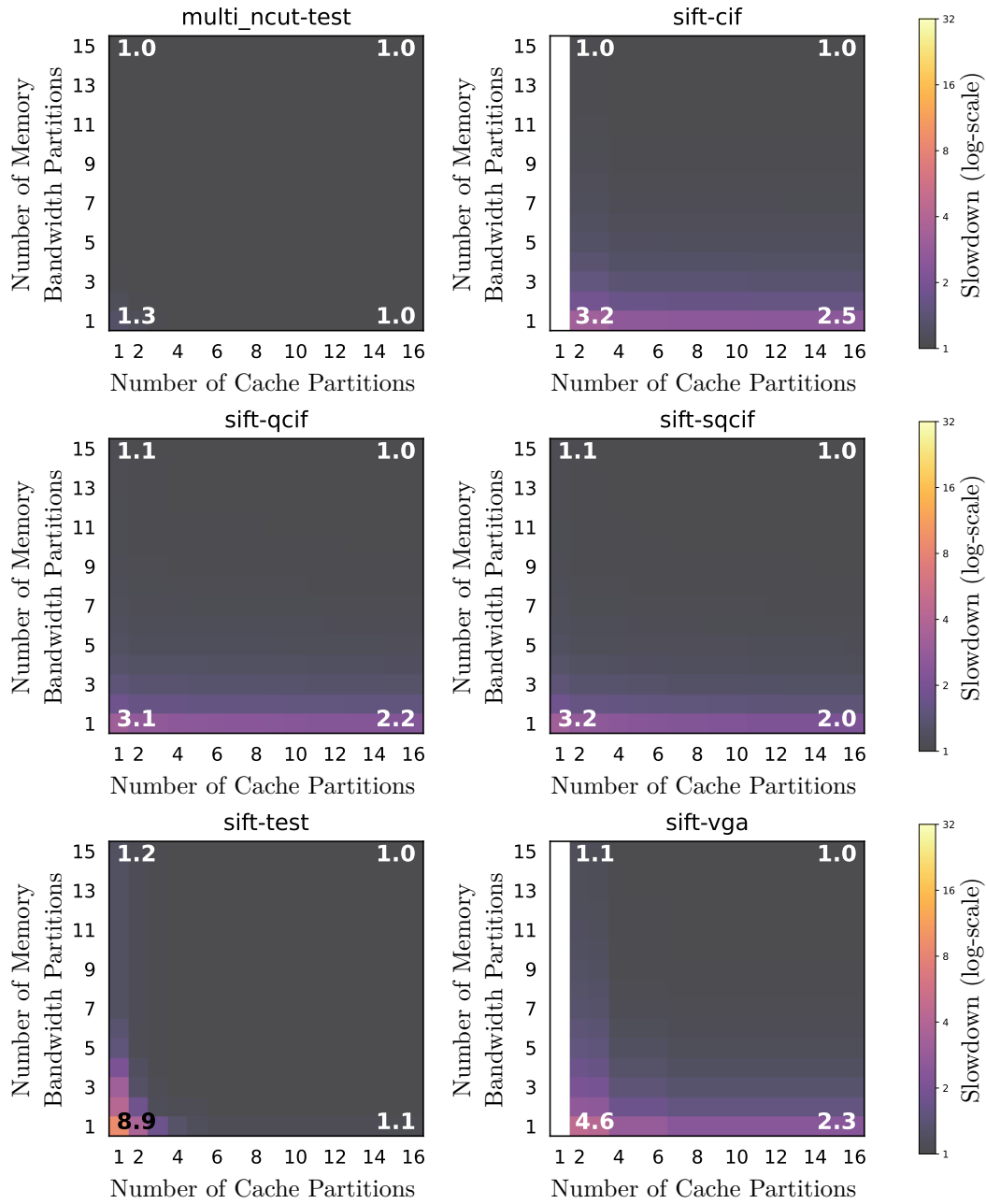
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## 1 SD-VBS Benchmarks

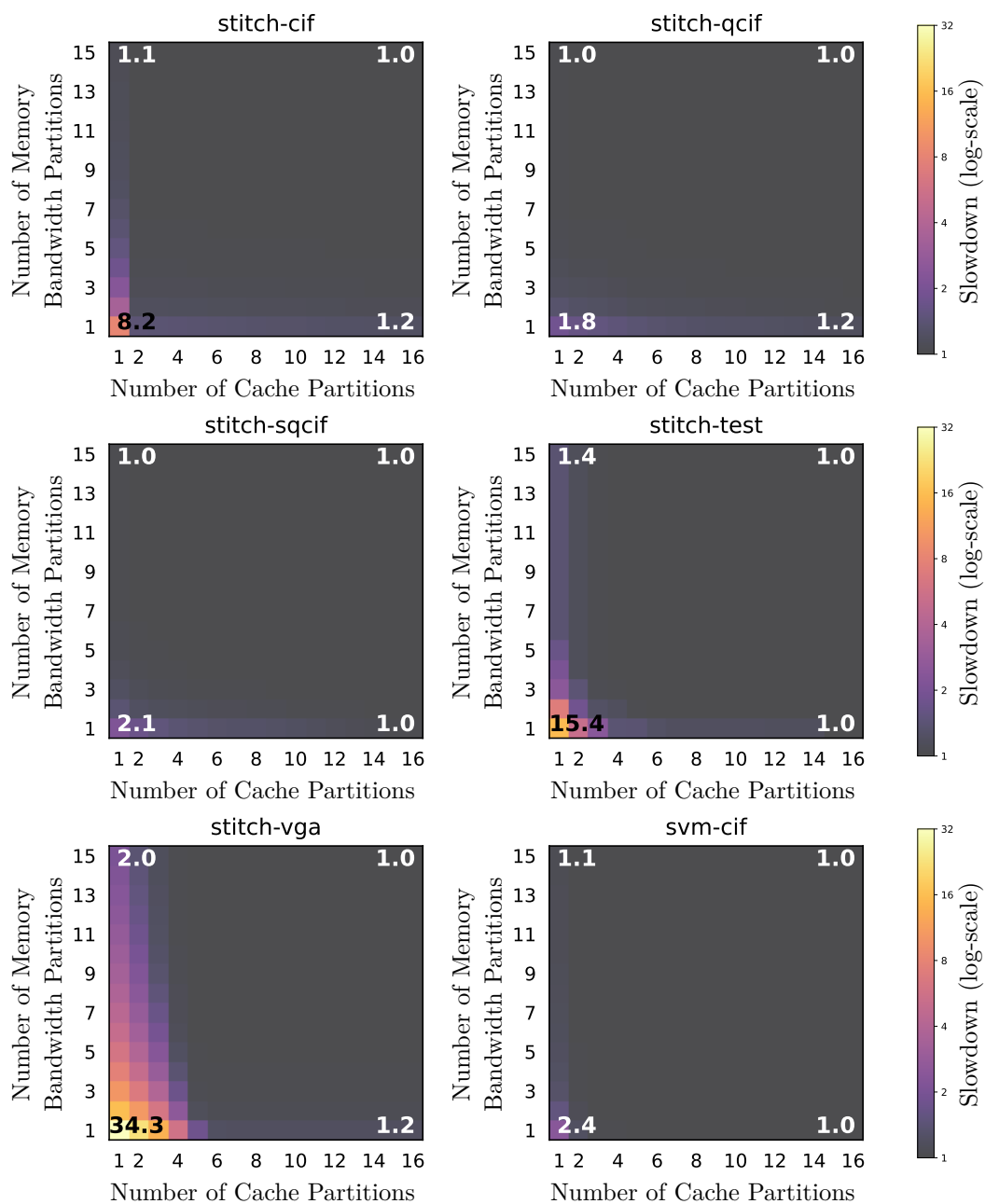


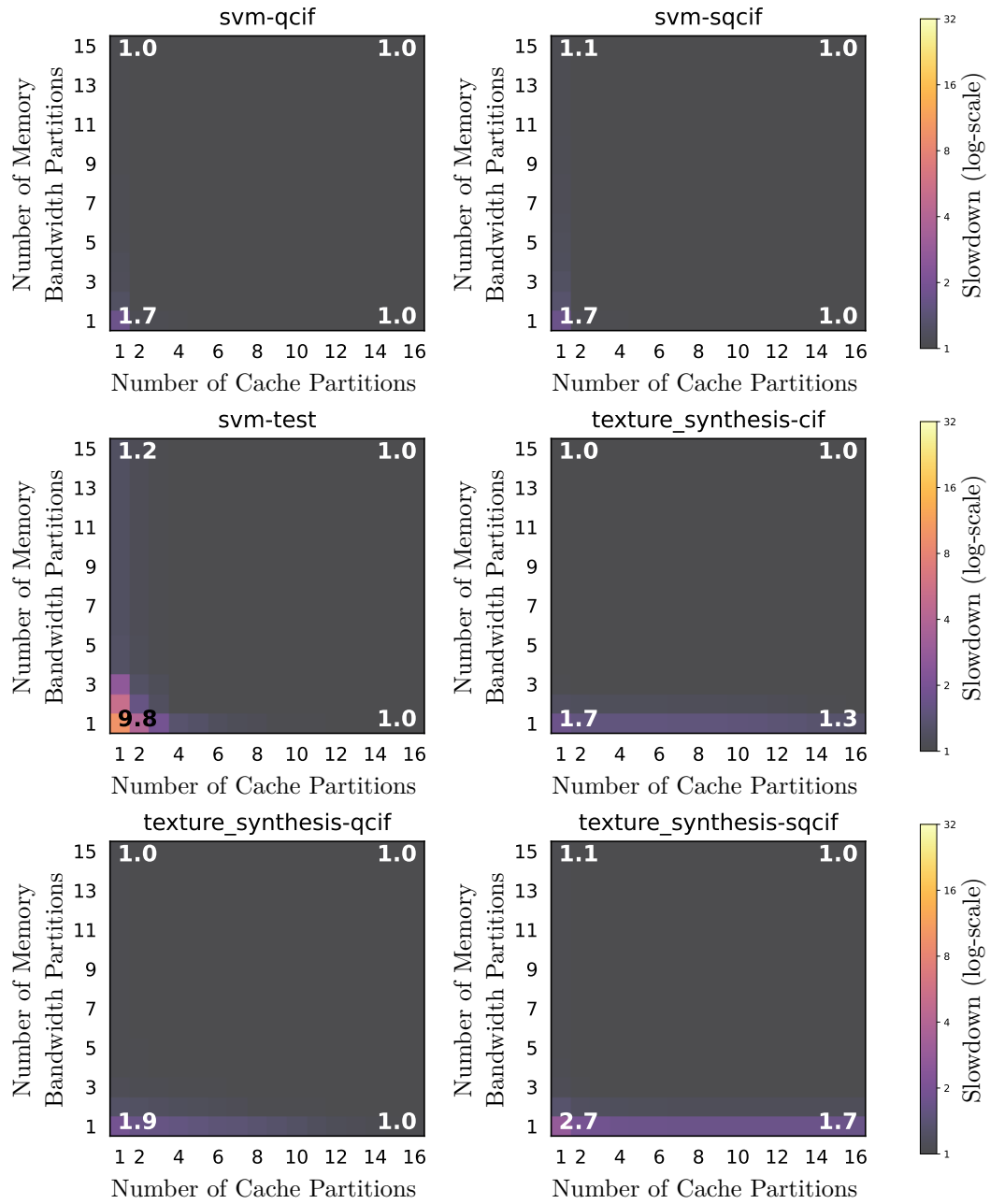


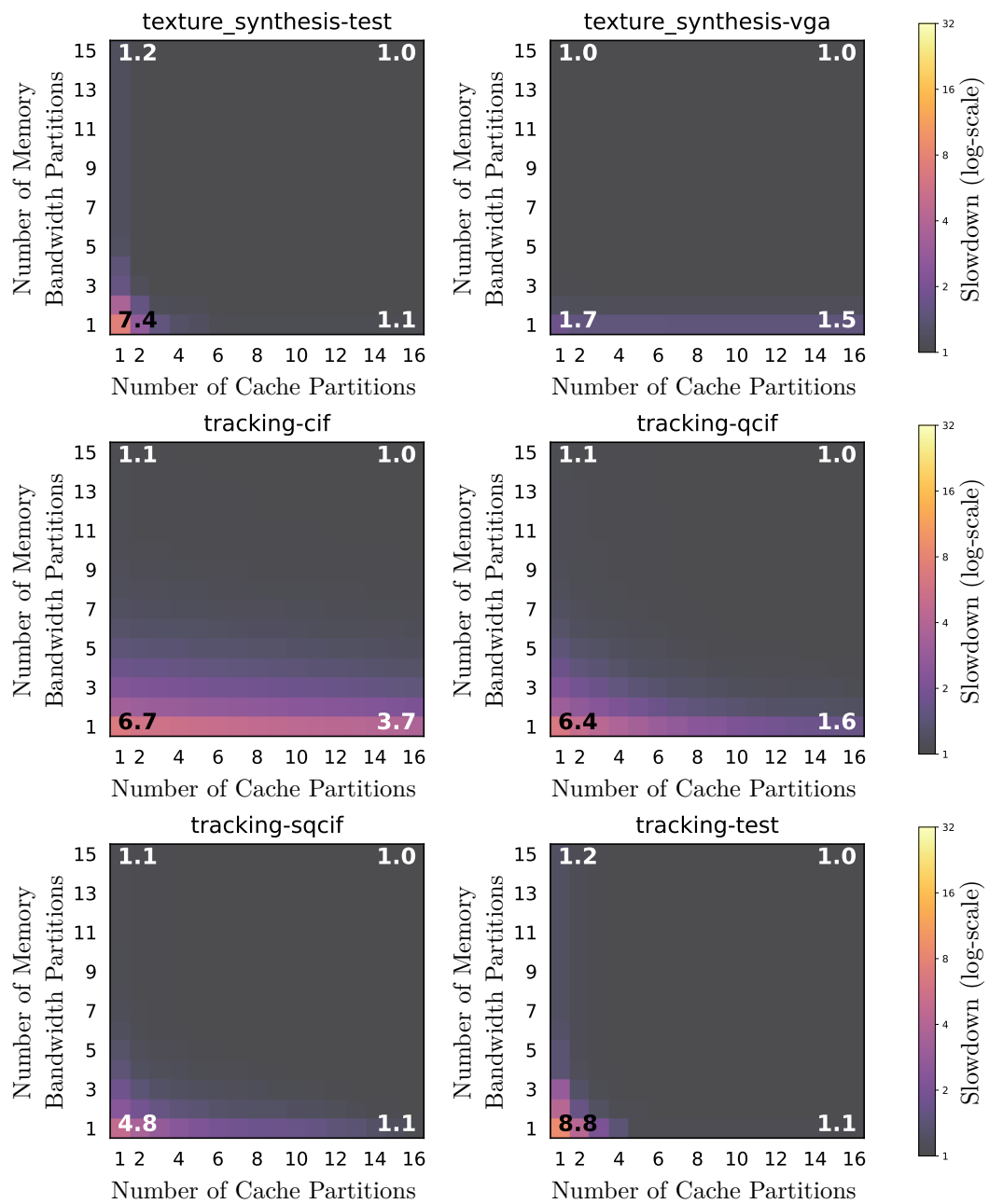




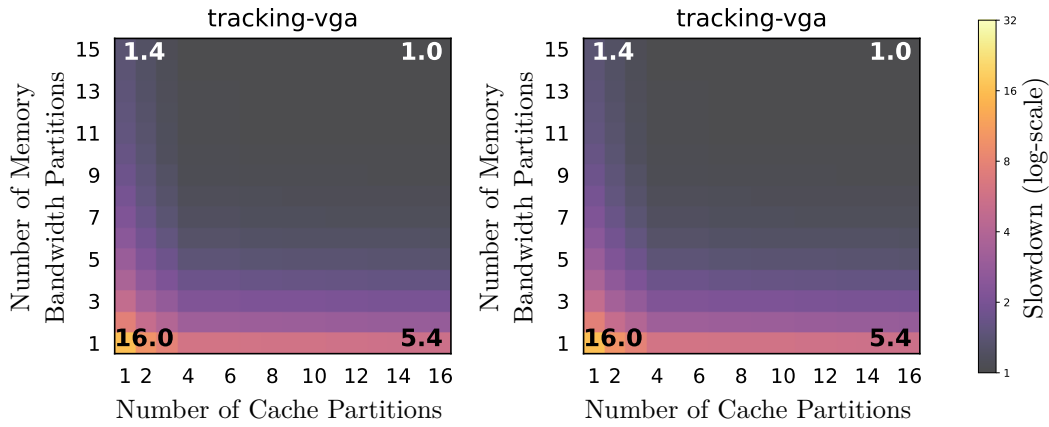
## 7:6 Multi-Objective Memory Bandwidth Regulation and Cache Partitioning



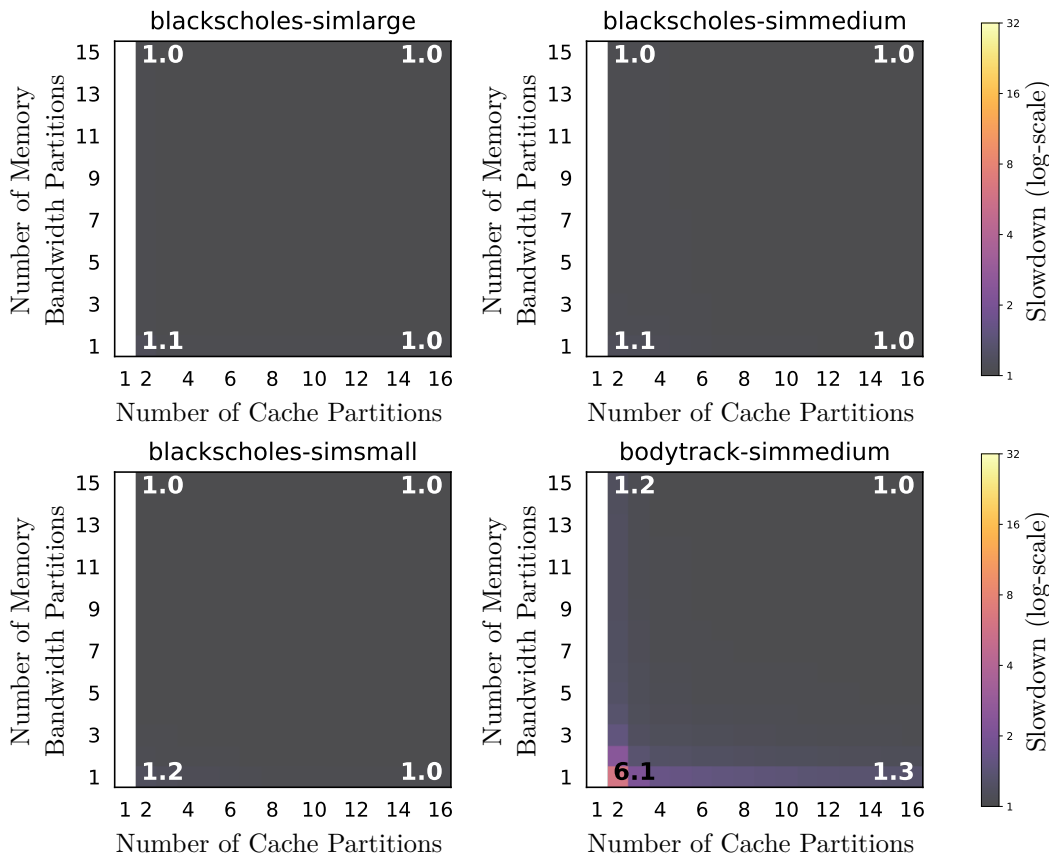




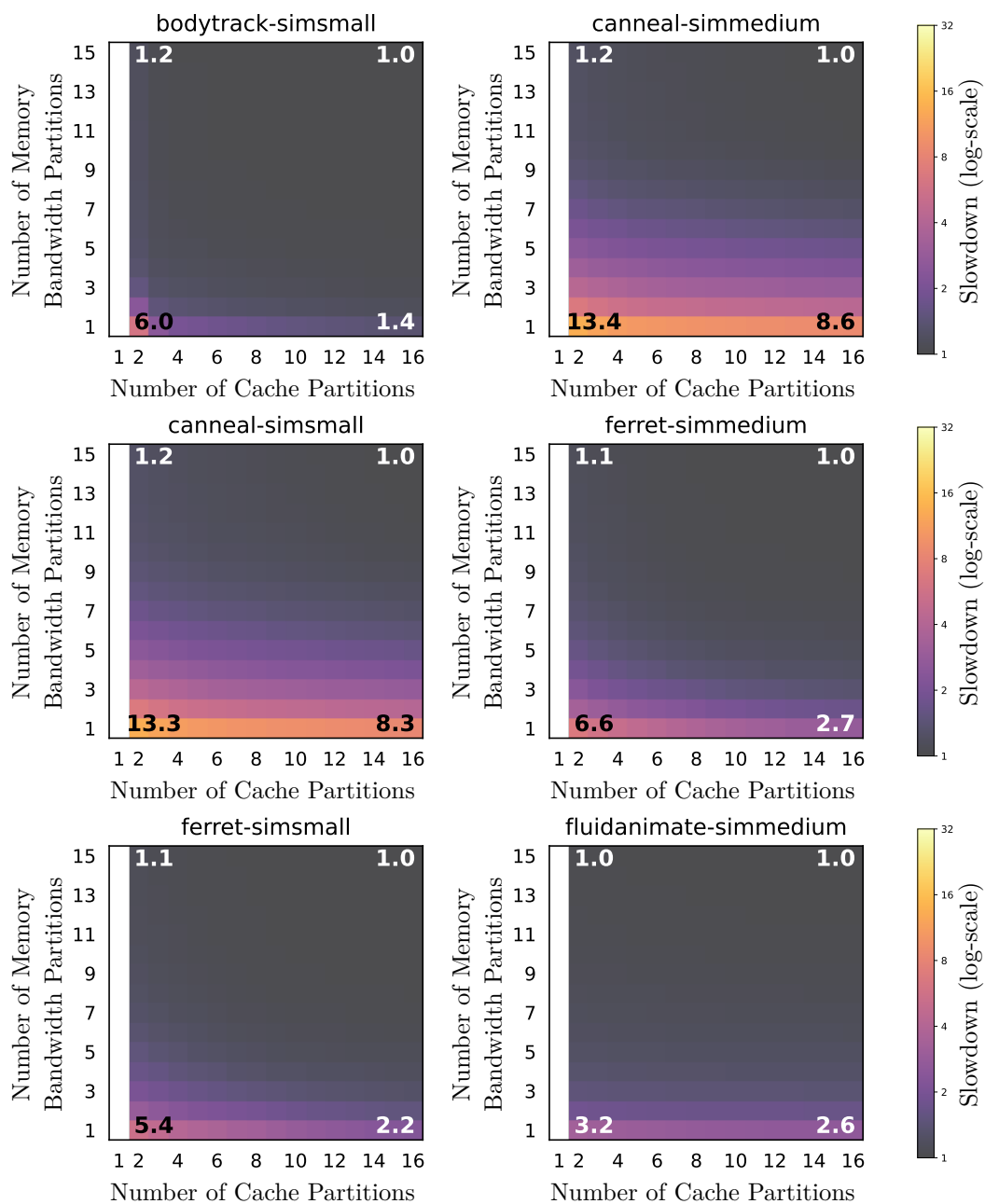


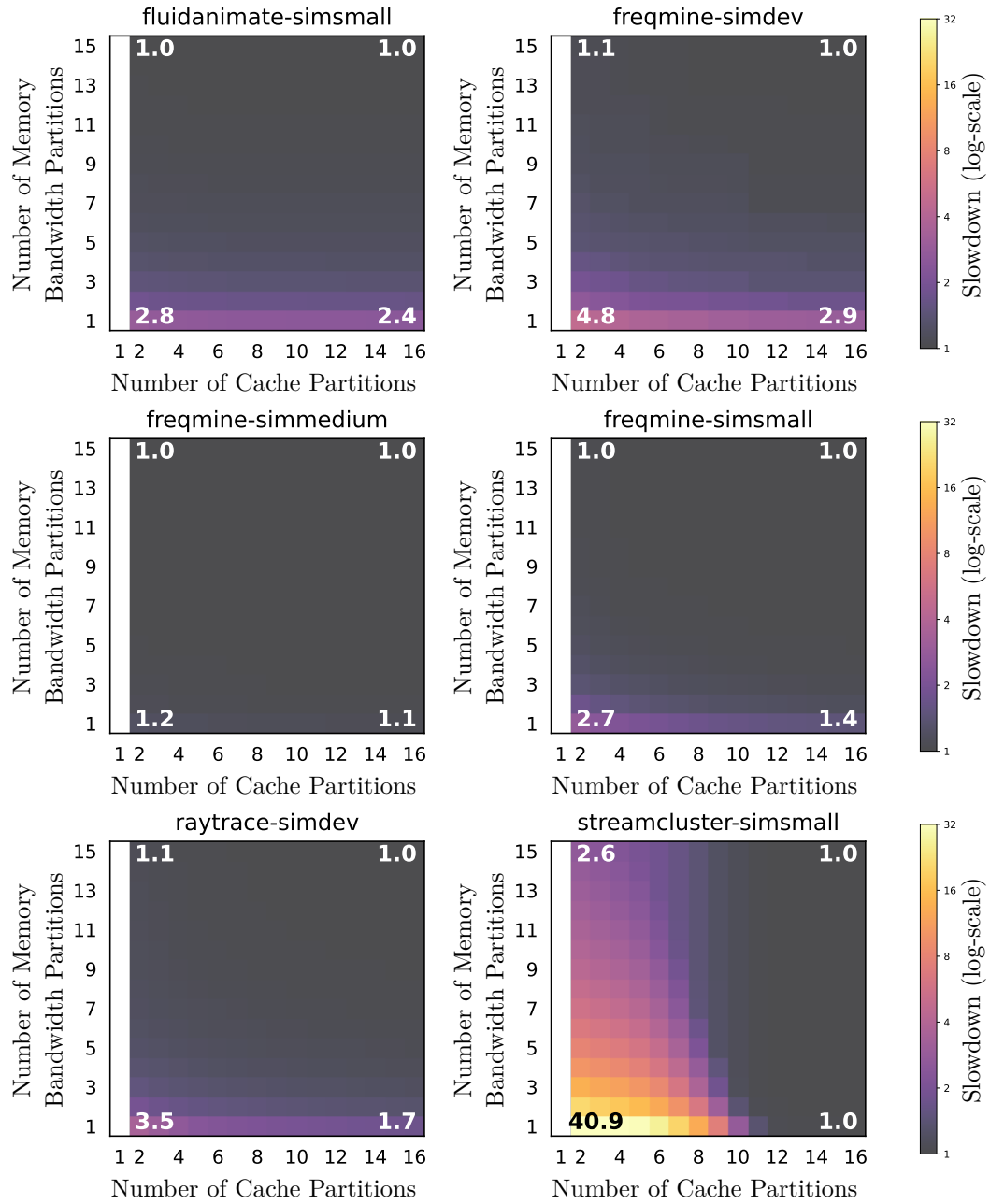


2 PARSEC Benchmarks



## 7:10 Multi-Objective Memory Bandwidth Regulation and Cache Partitioning





## 7:12 Multi-Objective Memory Bandwidth Regulation and Cache Partitioning

