Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

DESIGN ELECTRONICS FOR CLUSTER COUNTING AND PRODUCTION OF A 4-CHANNEL PROTOTYPE

MILESTONE: MS29

Document identifier:	AIDAinnova-MS29
Due date of milestone:	End of Month 46 (January 2025)
Report release date:	17/02/2025
Work package:	WP7: Gaseous Detectors
Lead beneficiary:	INFN
Document status:	Final version

Abstract:

In the context of drift chambers and for the application of the cluster counting technique, the object of this task is to be able to implement, within a single FPGA board, peak finding algorithms (with high peak-finding efficiency) for the parallel processing of as many channels as possible (4, at this stage).

The Advancement and Innovation for Detectors at Accelerators (AIDAinnova) project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 101004761. AIDAinnova began in April 2021 and will run for 4 years.

Delivery Slip

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Executive summary

This document describes the strategy pursued to define the best possible configuration of software and hardware tools necessary to design a multi-channel electronic board for cluster counting/timing.
The aim is to considerably decrease the cost and complexity of the data acquisition system, to reduce the data transfer rate and, at the same time, to provide, in conjunction with data coming from contiguous channels, the ability to correlate hits to form track segments in real time.
After a brief introduction to the subject, a short description of two different algorithms for identifying ionization electron peaks in the waveforms generated by a drift signal is presented. Both algorithms are converted in hardware description languages for use with FPGA.
A list of three different sophisticated hardware solutions is then proposed, among which the final choice for the 4-channel prototype of the readout electronics for cluster counting/timing is indicated.

1. INTRODUCTION

While the ionization loss per unit length by charged particles (*dE/dx*) is commonly used for particle identification, uncertainties in total energy deposition limit particle separation capabilities. To overcome this limitation, the cluster counting technique (*dN/dx*) leverages the Poisson nature of primary ionization, providing a statistically robust method for inferring the mass information. Simulation studies using Garfield++ and Geant4, validated by experimental data [1], indicate that the cluster counting technique can achieve a factor two better resolutions than the traditional dE/dx method in helium-based drift chambers. However, in real experiments, finding single electron contributions and identifying ionization clusters is extremely challenging due to the high density of electron signal peaks in the time domain.

The minimal requirements to perform efficient cluster counting on a drift chamber front-end are: *1 GHz* bandwidth, *2 V* dynamical range, signal to noise ratio larger than 10, on the digitizing electronics more than *10 bits* and *a* sampling rate larger than 1 *GSa/s* over a 1 *microsecond* time window.

Moreover, for a hypothetical drift chamber at the next generation of lepton colliders, like INTREPID, the one proposed by the IDEA detector at FCC-ee [2], an efficient implementation of the cluster counting technique, given the high drift chamber granularity and the expected machine luminosity, may require data transfer rates of more than *1 TB/s*. A possible way out of this complication consists in transferring, in real time, for each hit drift cell, only the minimal information relevant to the application of the cluster timing/counting techniques, i.e., the amplitude and the arrival time of each peak associated with each individual ionization electron, instead of the full digitized signal waveform. A reduction of the order of 100 in data transfer can thus be achieved.

This can be accomplished with the use of simple algorithms on an FPGA for the real-time pre-processing of the digitized data generated by the drift chamber. The same algorithms, in addition, will provide background and noise filters, thus further facilitating the track finding procedures.

2. OBJECTIVES

The goal of this task is to be able to implement, within a single FPGA board, peak finding algorithms (with high peak finding efficiency) for the parallel pre-processing of as many channels as possible (4, at this stage). The aim is to considerably decrease the cost and complexity of the system, to reduce the data transfer rate and, at the same time, to provide, in conjunction with data coming from contiguous channels, the ability to correlate hits to form track segments in real time. This information, besides providing a precise (order of a few *ns*) event time stamping, can be used to exploit the possibility of defining a first-level trigger based on track multiplicity, with latency compatible with the maximum drift time.

3. SOFTWARE IMPLEMENTATION

Two distinct algorithms for electron peak-finding, running in real-time as the signal waveform is being digitized, have been elaborated:

- DERIV, based on the first and second derivative of the digitized signal waveform. The peaks are detected by imposing thresholds on the local amplitude of the signal waveform and on its first derivative. A threshold criterion is also imposed on the sign of the second derivative. All thresholds are in units of the r.m.s. value of the detected signal noise. Fig. 1 illustrates graphically the results of this algorithm applied to a drift tube signal. The algorithm has been successfully implemented on FPGAs, reaching satisfactory results in terms of peak-finding efficiency and purity.

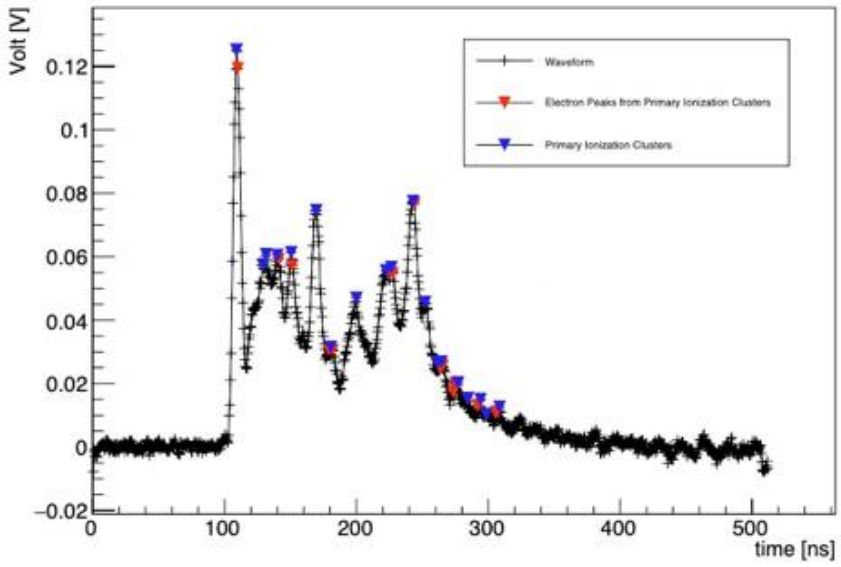

Fig. 1 DERIV algorithm applied to a drift tube signal waveform.

- RTA, based on a bin-by-bin matching of the signal waveform with a normalized single-electron-pulse template, generated with raising and falling exponential, empirically inferred from the experimental data, and digitized according to the data sampling rate. The algorithm scans the signal waveform, running over the bins, and compares it to the pulse template, normalized to the amplitude in the search window, by constructing an agreement assessment quantity established by an empirical cut-off value. Fig. 2 illustrates the application of the RTA algorithm to the same waveform of Fig. 1. Small differences in the found peaks with respect to the DERIV algorithm are due to the peculiarity of the two algorithms.

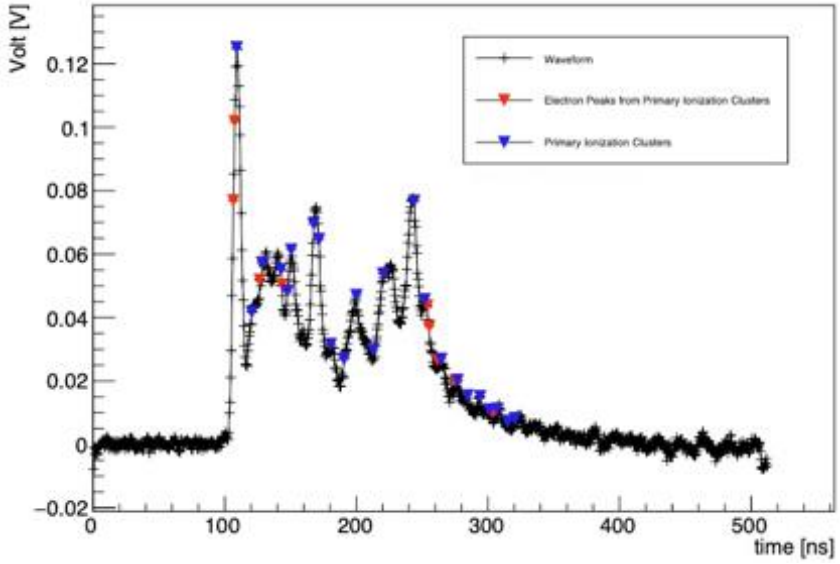

Fig. 2. RTA algorithm applied to the same waveform of Fig. 1.

Both algorithms are executed in real time, while the signal waveform is being digitized, lagging just by the a priori defined single pulse search window, t_w. Their full execution, therefore, occurs after a time interval t_{algo}, typically a few clock steps, added to the maximum drift time, t_{max}.

In addition to a C++ version used for the analysis of beam test data, both algorithms, limited to the identification in the digitized drift chamber signal waveform of the individual ionization electron peaks and to recording their time and amplitude, have been developed as VHDL/Verilog hardware description languages for FPGA programming.

As far as the DERIV algorithm is concerned, at the start of the signal acquisition and processing procedures, a counter is set to provide the timing information. A peak at the *i-th* bin is defined by relating its amplitude, with the first and second derivatives, to those of a number *n* of preceding and successive bins, in the time window t_w, with *n* depending on the rise and fall times of the single electron signal and of the ADC sampling rate. The amplitude and time of a found peak are then sent to a pipeline memory which is continuously filled as new peaks are found. When a trigger signal occurs at time t_0, the reading procedure is enabled and the data relative to the found peaks in the [t_0, $t_0 + t_{max}$] time interval, where t_{max} is the maximum drift time, are transferred to an external device. Results of the application of the VHDL version of the DERIV algorithm (CluTim algorithm), implemented on a *Virtex 6* FPGA have been published [3].

The RTA algorithm is implemented in a similar manner and can be executed alternatively to the DERIV algorithm. A comparison between the results of the two algorithms will be the subject of a forthcoming report.

For each event, the list of found peaks, with their relative time and amplitude, is stored in a pipeline memory, which is transferred to the data acquisition system in case of a trigger signal, or, alternatively, overwritten by the new list of peaks found in the subsequent event.

Peak finding is a typical classification problem, suitable for the application of Long Short-Term Memory (LSTM) networks, predominantly used to classify sequential data. Therefore, a third algorithm, ML, based on Recurrent Neural Networks (RNN), has also been fully developed [4]. However, since its implementation on FPGAs requires dedicated hardware and software procedures, this approach has been deferred and the focus of this task has been limited to the application of the DERIV and RTA algorithms with their suitable hardware implementations.

4. HARDWARE IMPLEMENTATION

As far as the hardware implementation is concerned, a voltage-sensitive preamplifier (Texas Instruments LMH6522 [5]), shown in Fig. 3, with a maximum high voltage gain of 20 and a high bandwidth (*1.5 GHz*) is used to drive a high-performance digitizer. It contains four digitally controlled variable gain amplifiers (*DVGA*), each one with an independent, digitally controlled, attenuator and a high linearity, differential output amplifier (the differential inputs and differential outputs can be converted to single-ended signal paths to easily interface with *50* Ω single-ended equipment), optimized for low distortion and maximum system design flexibility.

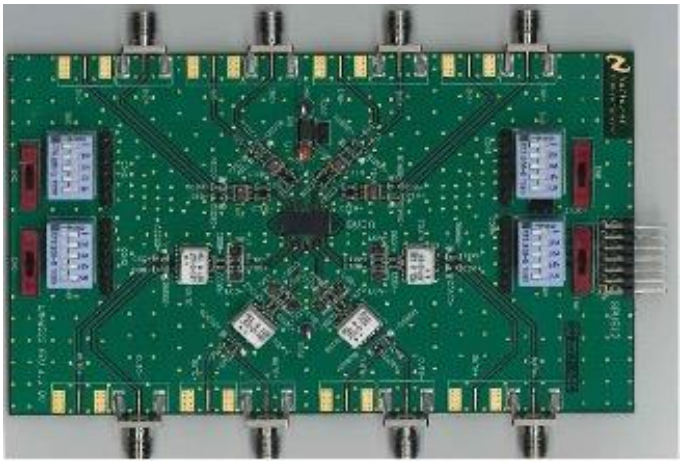

Fig. 3. TEXAS Instrument LMH6522 evaluation board.

After the preamplification stage, the digital conversion of the drift chamber waveform, at the proper sampling rate, and the simultaneous FPGA algorithm implementation continue with one of the following approaches.

4.1. TEXAS INSTRUMENT ADC32RF45 coupled to the XILINX FPGA KCU105

This approach, shown in Fig. 4, where only one of the two dual-channel ADC is shown, provides the best performance in terms of the cluster counting requirements and is used also as a test bed to compare the performance of different algorithms and of alternative hardware implementations.

The ADC32RF45 [6] is a *14-bit*, *3.0 GSa/s*, dual-channel, analogue-to-digital converter (ADC) that supports waveform sampling with input frequencies up to *4 GHz* and beyond. It is designed for high signal-to-noise ratio (*SNR*), and channel isolation over a large input frequency range. It supports the *JESD204B* serial interface, a system-level software providing a performance optimized framework to integrate the ADC with various FPGA platforms, where the data are framed, encoded, serialized, processed and output.

Xilinx's KCU105 [7] evaluation board is a powerful and versatile FPGA development platform specifically designed to provide high-performance computing, enabling wide-band data acquisition over JESD204B high-speed serial connectivity. It utilizes the Xilinx Vivado development environment, enabling to easily develop and validate algorithms. It is equipped with *64-bit DDR4* component memory, offering robust storage and memory management for the specific applications of cluster counting, ensuring efficient data handling, and supporting faster processing speeds.

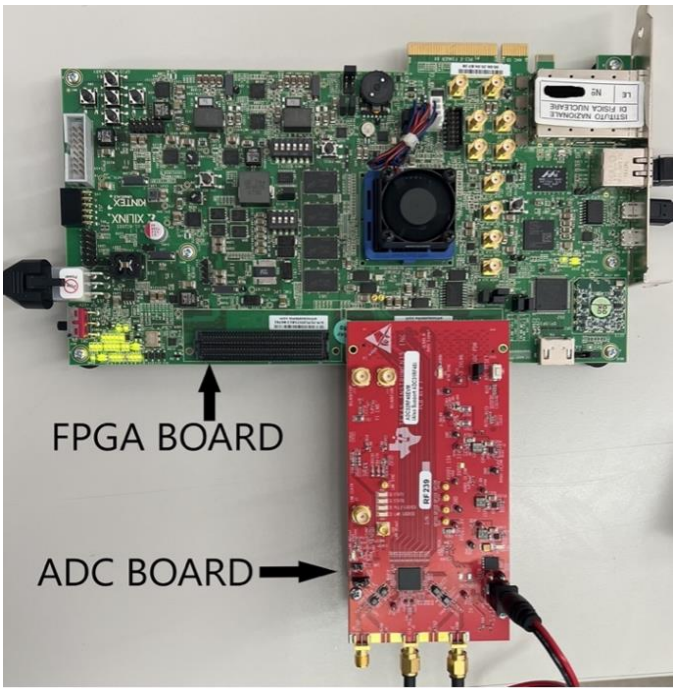

Fig. 4. The experimental setup of the coupling of the ADC32RF45 evaluation board (only a single dual-channel board is shown) with the FPGA KCU105 evaluation board.

4.2. CAEN digitizer VX2751

The VX2751 [8], shown in Fig. 5, is a 16-channel digital signal processor offering, independently for each of the 16 channels, waveform digitization and recording. It can manage the entire acquisition chain, from the input signal sampling in the ADC to the processing of the signal and readout.

The analog single-ended input channels, with software selectable input gain up to x100 and *500 MHz* bandwidth, are digitized with a *14 bit, 1 GSa/s* ADC, compatible with the minimal requirements for cluster counting. The sampled data are used to initiate the digital pulse processing sequence, managed in the FPGA at the firmware level, where different firmware types, including custom algorithms, like DERIV and RTA, can be selected via software. Besides VHDL programming language, the available Sci-Compiler software, a block-diagram-based graphic tool, offers a very flexible and user-friendly way to build up more complex algorithms.

At the end of January 2025, CAEN has commercially released the first version of the VX2751 and provided us with a module. Therefore, we are now in the process of implementing the cluster counting algorithms and testing the whole procedure.

Hopefully, by the end of the project in September 2025, we will be able to update this document with the results of a direct comparison between the CAEN VX2751 and the ADC32RF45 + KCU105 with experimental drift tube waveforms.

Fig. 5. CAEN digitizer VX2751.

4.3. NALU Scientific ASoCv3 and HDSoC

For a very short time we have been provided by Nalu Scientific [9] with an evaluation board of the ASoCv3 chip. We have been able to test its performance on the bench, without being able to use real signals out of a drift tube, for lack of time. Fig. 6 illustrates the specifications of the ASoCv3 chip and Fig. 7 shows the experimental set up, together with a Digilent Nexys FPGA board with a serial communication interface.

Parameter	Spec
Sample rate	2.4-3.6GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Number of ADC bits	12 bits
Supply Voltage	2.5V
RMS noise	~1.5 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps (see below for details)
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

Fig. 6. Specifications of the ASoCv3 chip produced by Nalu Scientific.

In Fig. 8, left, an AWG simulated drift tube signal is compared to the same signal seen by the ASoCv3, at right. Bandwidths limitations are evident, concealing structures with close peaks. Moreover, a worsening of the signal to noise ratio is observed.

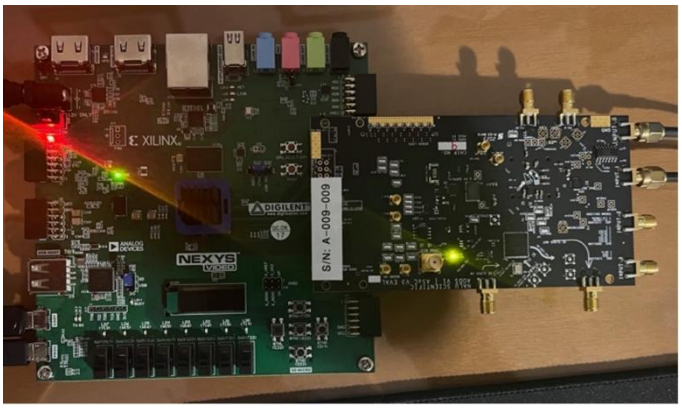

Fig. 7. Test setup of ASoCv3 chip evaluation board by Nalu Scientific.

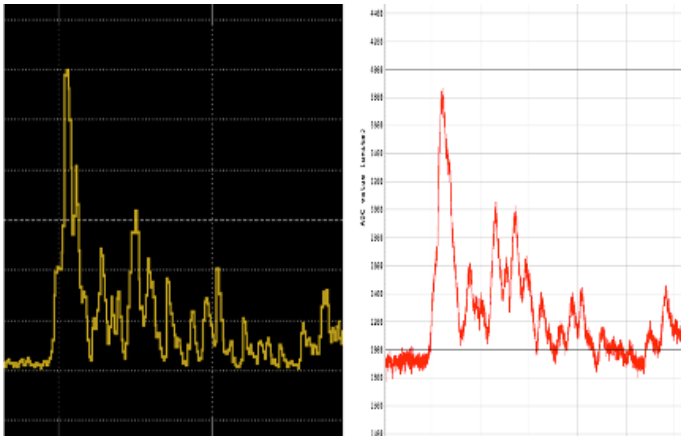

Fig. 8. AWG simulated drift tube signal, at left, compared to the same signal seen by the ASoCv3 setup. Full horizontal scale is 500 ns.

Nalu Scientific has also developed a new high-density chip, HDSoC, with 64 channels, *> 600 MHz* analog bandwidth and up to *2 GSa/s* sampling rate. Fig. 9 illustrates the specifications of the HDSoCv1 chip. A 32 channels evaluation board of this chip has been procured (thanks to CAEN Technologies, US branch of CAEN, distributor for Nalu Scientific), together with a Digilent Nexys FPGA board with a serial communication interface. The electronic setup, shown in Fig. 10, is currently under testing.

Parameter	Spec
Sampling Rate	1-2 GSa/s
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	TBD

Fig. 9. Specifications of the HDSoCv1 chip produced by Nalu Scientific.

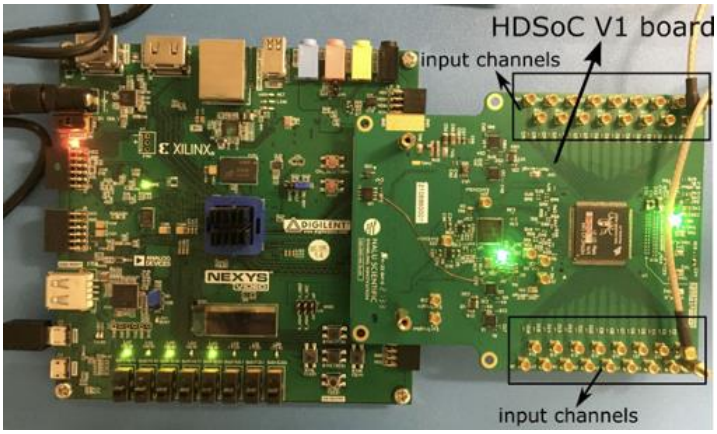

Fig. 10. Test setup of the 32-channels HDSoCv1 evaluation board.

5. CONCLUSIONS

While the studies for implementing ML algorithms on FPGA are continuing as a possible configuration for the data acquisition architecture of the INTREPID drift chamber of the IDEA detector at FCC-ee, both from the software and hardware points of view, we have concentrated our efforts on the three alternative hardware implementations listed in the previous paragraph, equipped with the described DERIV and RTA algorithms.

- **NALU SCIENTIFIC ASoCv3 and HDSoC**

From a visual inspection of the signal of Fig. 8, it is evident that the quoted bandwidth of the ASoCv3 chip, *850 MHz,* is marginal for an efficient application of the cluster counting technique. The multi-peak structure visible in the first 50 *ns* of the AWG signal at the input of the chip appears blended at the output, impairing a correct detection of the number of electron peaks. Moreover, the worsening of the signal-to-noise ratio by more than a factor 3 contributes to the peak finding inefficiency for lower amplitudes. We expect an even inferior performance from the test of the HDSoCv1 chip, since its analogue bandwidth is quoted to be even lower, *600 MHz*. We are confident that future versions of these chips will provide better performance in terms of bandwidth, and we will pay attention to new releases. However, at this stage and for this task, we decline this solution.

- **CAEN digitizer VX2751**

Although we have not been able yet to evaluate the performance of the very recently (January 2025) released VX2751 digitizer, according to the experience gained with the Nalu ASoCv3 tests, the CAEN quoted *500 MHz* bandwidth sounds even more marginal. However, the high input gain and the larger number of bits, 14, may moderate the bandwidth limitations. We are, therefore, eager to complete our tests and to formulate a complete evaluation of the performances of the VX2751. In the meantime, we are optimizing both peak finding algorithms by taking advantage of the available Sci-Compiler software.

- **TEXAS INSTRUMENT ADC32RF45 coupled to AMD Kintex FPGA KCU105**

We propose this configuration as the final choice, as it represents the best solution in terms of performance, satisfying the requirements of the cluster counting/timing technique.

Therefore, we envisage the 4-channels prototype electronics chain for cluster counting, shown in Fig. 11, made of a sequence of the following blocks:

- **Texas Instruments LMH6522** as a first stage of a 4-channels voltage sensitive preamplifier, directly connected to the terminated outputs of the drift tubes.

- **Texas Instruments ADC32RF45**, two dual channel analog-to-digital converter chips on an interface card, accepting at the input the four differential outputs of the preamplifier, and sending the digitized outputs through the serial interface JESD2048 to the FPGA.

- **AMD Kintex UltraScale FPGA KCU105**, with the DERIV and RTA algorithms implemented on, as described above.

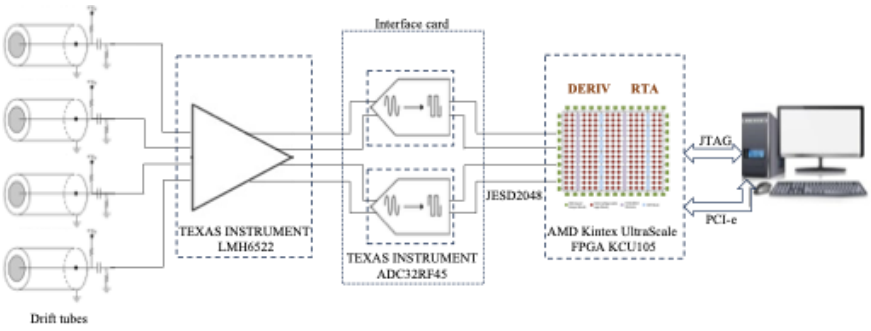

Fig. 11. Block diagram of the 4-channels prototype electronics chain for cluster counting.

6. REFERENCES

[1] Elmetenawee, W. et al. (2024) Advancing Particle Identification in Helium-Based Drift Chambers: A Cluster Counting Technique Study through Beam Tests. In: *Proceedings of 42nd International Conference on High Energy Physics (ICHEP2024)* 18-24 July 2024, Prague, Czech Republic.

[2] Benedikt, M. et al. (2019) FCC-ee: The Lepton Collider: Future Circular Collider Conceptual Design Report Volume 2. *Eur. Phys. J. Spec. Top.* 228 (2019) 261-623.

[3] Chiarello, G. et al. (2017) The Use of FPGA in Drift Chambers for High Energy Physics Experiments. *2017 JINST 12 C03056* - ISBN 978-953-51-3208-0.

[4] Zhao G., Wu L., Grancagnolo F., De Filippis N., Dong M., Sun S., (2024) Peak finding algorithm for cluster counting with domain adaptation. *Computer Physics Communications* 300 (2024) 109208, arXiv:2402.16270

[5] https://www.ti.com/product/LMH6522

[6] https://www.ti.com/product/ADC32RF45

[7] https://www.xilinx.com/products/boards-and-kits/kcu105.html

[8] https://www.caen.it/products/vx2751/

[9] https://www.naluscientific.com/