Application of Reliability Test Standards to SiC Power MOSFETs

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***Abstract*—The application of existing reliability test standards, based on Si technology, to SiC power MOSFET reliability qualification can in some cases result in ambiguous test results. Depending on the exact measurement procedure, a given device stress tested under identical conditions may either pass or fail. The large variations observed in I_D-V_{GS} characteristics, and accompanying shift in threshold voltage (V_T) and change in leakage current, are likely due to the complex time, temperature, and bias dependent nature of the charging and discharging of significant numbers of near-interfacial oxide traps (and possibly mitigated by the movement of mobile ions) which are not present in Si power devices. The variation in V_T following a high temperature gate-bias (HTGB) stress is shown to be dependent on the measurement delay time, sweep direction, and temperature. Negative gate-bias temperature stress results show that device reliability may be limited due to increased drain leakage current in the OFF-state, which is caused by large shifts in V_T depending on the gate-bias stress time, bias magnitude, and stress temperature. In addition, positive gate-bias stressing at elevated temperature may increase power dissipation in the ON-state.**

Keywords-component; Power MOSFETs, SiC, V_T instability, oxide traps, HTGB, BTS

I. INTRODUCTION

Silicon Carbide (SiC) power devices provide enhanced temperature operation with higher breakdown field capability, enabling the development of power systems with higher power density, lower losses, and the promise of improved reliability. Advances in material and device technology have resulted in the development of power SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) with higher blocking voltage and lower specific on-resistance in comparison to their silicon (Si) counterparts [1, 2]. The feasibility of SiC MOSFET devices for power electronics applications has been recently demonstrated with the development of several power modules [1-2]. However, device reliability issues, including threshold voltage (V_T) instability [3, 4], must first be resolved.

In this paper, we investigate the effects of high temperature gate bias (HTGB) stress on the reliability of 4H-SiC power MOSFET devices within the guidelines of accepted industrial and military standards for stress test qualification of semiconductor devices. Our findings reveal that the application of existing standards (e.g. JEDEC JESD22-A108C [5], MIL-STD-750E [6], and AEC-Q101 [7]), which are based on Si device technologies, may result in inconsistent pass/fail results when applied to SiC MOSFET devices due to a large threshold voltage variation that strongly depends on measurement conditions.

For instance, the Joint Electron Devices Engineering Council (JEDEC) standard [5] requires that post burn-in electrical measurements be completed as soon as possible, but no longer than 96 hours after removal of the bias. This 96-hour window for electrical testing appears to be inappropriate in qualifying SiC MOSFET devices because of the complex time, temperature, and bias dependent nature of the observed V_T instability, which is likely due to the charging and discharging of near-interfacial oxide traps through a direct

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tunneling mechanism [3, 8]. This complex dependence causes the drain current versus gate-to-source voltage (I_D-V_{GS}) characteristics to be sensitive to both the measurement sweep speed and direction, which are not addressed at all by the present standards.

Our stress results also show the large variability in the threshold-voltage shift due to variations in stress bias, time, and temperature. The different existing standards, with their varying stress conditions, may also result in inconsistent device evaluations. For example, the Automotive Electronics Council (AEC) standard [7] calls for a 1,000 hour HTRB and HTGB stress, whereas the Department of Defense (DoD) Mil Std 750-E [6] only requires a 48 hour stress, at 80% of the maximum rated gate bias.

This variability in the threshold-voltage shift makes it critical to carefully assess the applicability of existing Si-based testing standards as they begin to be used to qualify SiC-based power electronics. A proper reliability test should be able to quickly and non-destructively evaluate a device's suitability for long-term, reliable operation and separate bad parts from good ones. Before existing reliability standards are applied to SiC power devices, we must determine if they are adequate for evaluating the reliability of SiC-based technology.

The present standards also differ in relation to electrical measurement procedures. For example, JESD22-A108C [5] allows for electrical testing at elevated temperature but only after post-stress room temperature measurements have been performed. AEC-Q101 [7] requires that pre- and post-stress electrical measurements occur at room temperature, but does not explicitly state whether device characteristics could be made at elevated temperatures.

There is little consistency between the standards as it relates to device failure criteria as well. The AEC standard, for example, explicitly requires that specific device parameters remain within electrical test limits of the specification and within ± 20 percent of their pre-stress values. If not, these devices are deemed as failing. Leakage currents, however, cannot exceed five times their initial value. The applicable JEDEC and DoD standards are not so clear in regard to device failure criteria.

II. Experimental Procedure

We have examined the effects of HTGB stressing on the I_D-V_{GS} characteristics of large area (0.56 cm^2) SiC power MOSFET devices. These devices are research samples with voltage and current ratings of 1200 V and 67 A, respectively, and fairly representative of the state-of-the-art in SiC MOSFET technology. Two populations of power MOSFETs were evaluated. Previous, but unpublished negative bias temperature stress (NBTS) revealed significant V_T drift in devices from Group A. Devices from Group B were redesigned to mitigate V_T drift issues associated with previously fabricated Group A devices. Both device groups have a thermally-grown gate oxide which received a standard nitric oxide (NO) post-oxidation anneal.

During a stress cycle, all devices were stressed at a temperature of 150 °C with either V_{GS} = +15 V or –15 V depending on whether a positive bias temperature stress (PBTS) or negative bias temperature stress (NBTS) was applied, unless otherwise specified. For the duration of the temperature ramp, V_{GS} was maintained at ± 15 V with V_{DS} = 0 V. The device temperature generally stabilized in approximately 90 seconds, after which, the high-temperature bias stress was initiated. At the end of the stress, the device was rapidly cooled to room temperature in about 90 seconds while maintaining the gate-bias stress.

I_D-V_{GS} measurements were typically made immediately following an HTGB stress cycle with V_{DS} = 50 mV once the device reached room temperature and the stress bias was removed. The stress and measurement sequences were made using an Agilent 4155C Parameter Analyzer. Following a PBTS cycle, an immediate sweep down of V_{GS} from +15 to −5 V was made to measure the effect of the stress on the device I_D-V_{GS} characteristics. After a NBTS cycle, an immediate sweep up of V_{GS} from –5 to +15 V was made to measure the effect of the stress on the device I_D-V_{GS} characteristics. The SiC MOSFET devices were characterized by measuring shifts in the linear extrapolated V_T and low current (1×10^{-6} A) V_{GS}, both pre- and post-stress. The

change in threshold voltage (ΔV_T) and gate bias (ΔV_{GS}) characterizes the effect of the stress and was determined by taking the differences between post- and pre-stress values for V_T and V_{GS}, respectively.

III. Results and Discussion

In the following sections we examine the effects of HTGB stress testing and variations in the subsequent measurement conditions on the I_D-V_{GS} characteristics of relative state-of-the-art SiC power MOSFET devices and demonstrate the shortcomings in existing reliability and qualification standards when applied to SiC power MOSFETs.

A. Previous Results

It has been previously observed on various SiC MOSFET devices from different manufactures that gate-bias stressing results in instability of the I_D-V_{GS} characteristics, with positive-bias stress causing a positive shift and negative-bias stress causing a negative shift. The resulting V_T shifts are not permanent and may be reversed by a reversal of the applied gate bias. This instability is likely due to the charging and discharging of near-interfacial oxide traps by electrons tunneling to and from the SiC [8]. Recent high-temperature bias-stress testing of power SiC MOSFETs, including self-heating caused by ON-state current stressing, reveals a significant increase in this V_T instability in some devices, which may be due to the activation of additional oxide traps, related to an oxygen vacancy defect referred to as an E-prime center [3]. A smaller variation in V_T instability in other devices with increasing temperature may either be due to improved gate oxide processing or to the presence of mobile ions, which will cause an opposite shift to that caused by charge trapping [9]. A negative V_T shift can give rise to increased leakage current in the OFF-state, especially at elevated temperature where an increased stretch-out of the subthreshold slope has been observed [3]. Therefore, high-temperature gate-bias testing of these devices is necessary for complete reliability monitoring and device qualification.

B. Measurement Parameters

Previous work on SiC power MOSFETs [3,4,8-10] have shown how measurement parameters and conditions can affect the data. Here, we investigate the effects of three measurement-specific parameters and their implications for robust reliability testing: delay time, sweep direction, and temperature.

1) Measurement Delay Time

In this section, we examine the effects of measurement delay time on the transfer characteristics of SiC power MOSFETs following both positive and negative static HTGB stresses. Measurement delay is defined as the time between removing the gate-bias stress and initiating an I_D-V_{GS} measurement sweep. This delay time should not be confused with the time associated with making an I-V measurement (i.e. gate sweep speed). Variation in measurement speed has been previously shown to produce a considerable variation in the I_D-V_{GS} characteristics and corresponding V_T of SiC MOSFETs [8, 10] due to the sensitivity of the oxide trap charging process to the bias applied during the measurement. The JEDEC standard allows for a 96 hour window for electrical testing after removal of the bias stress. However, the data presented below indicates that this large time window may not be appropriate when testing SiC power MOSFETs due to the complex nature of the charge trapping that occurs.

Positive bias temperature stressing generally produces a positive shift in V_T. Fig. 1 illustrates the large variation in I_D-V_{GS} characteristics of a representative Group A SiC power MOSFET following a one-hour gate-bias stress at 150 °C with V_{GS} = +15 V, depending on whether the

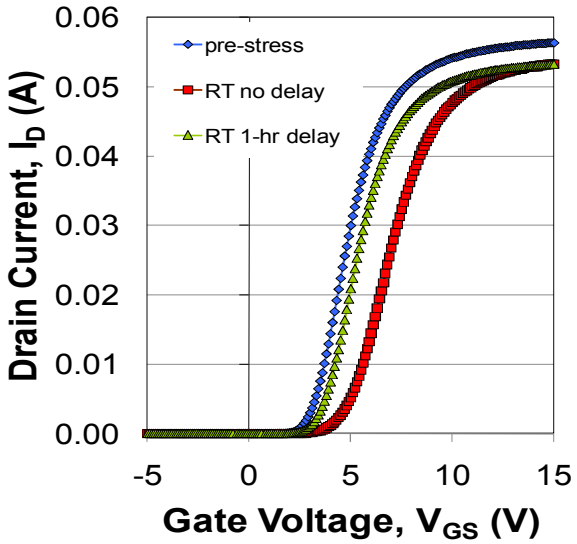

Figure 1. Effect of measurement delay on the I_D-V_{GS} characteristics of a Group A MOSFET following PBTS.

measurement is made immediately after rapidly cooling back to room temperature, or after a delay of one hour. To further dramatize the difference, the immediate measurement was made by sweeping down in gate bias, from +15 V to −5 V, whereas the later measurement was made by sweeping up in gate bias in the conventional manner. None of the present standards address sweep direction. We examine the effect of sweep direction further in Section III.B.2 on the device transfer characteristics following PBTS.

The linearly extracted V_T from the PBTS data shown in Fig. 2 indicates that the immediate post-HTGB measurement, which revealed a significant positive shift in V_T, would result in device failure based on the AEC standard [7] which requires that post burn-in measurement parameters remain within ± 20 percent of the pre-stress value, whereas the later measurement would not. This result clearly illustrates the time-dependent nature of the charge trapping.

Devices from Group B exhibited a similar response to positive HTGB stressing, although the magnitude of these shifts was smaller under identical PBTS conditions due to improved gate oxide processing. The range in ΔV_T with no delay time for devices from Group B was 0.2 V to 0.4 V, compared to a ΔV_T range of 0.9 V to 2.9 V for devices from Group A. It should be noted that although some of these devices may have remained within the 20 percent variation standard based on these test results,

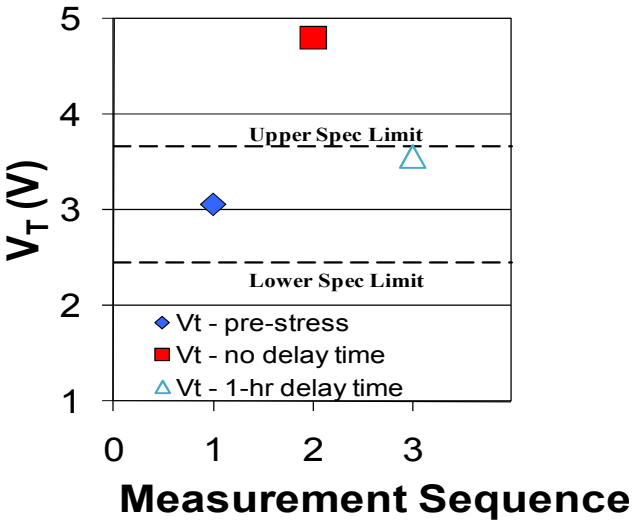

Figure 2. Linearly extracted V_T variation following PBTS within AEC standard (±20%)

the one-hour bias stress time used in this case is much shorter than the standard stress times. Longer bias stress times would have led to greater V_T shifts—see Section III.C.3.

Conversely, NBTS typically induces a negative shift in measured V_T. Fig. 3 shows the variation in response due to measurement delay time following a one-hour gate-bias stress at 150 °C with $V_{GS} = -15$ V for a typical device from Group A. Although the variation in V_T between the immediate and one-hour delayed measurements is not as great as in the PBTS case, the immediate measurement does result in an increase of the *OFF*-state leakage current due to the larger negative shift in V_T. Similarly, Fig. 4 shows

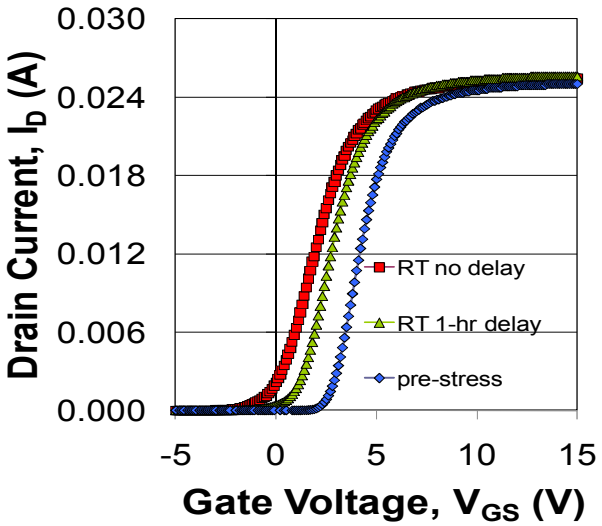

Figure 3. Effect of measurement delay on the I_D-V_{GS} characteristics of a Group A MOSFET following NBTS.

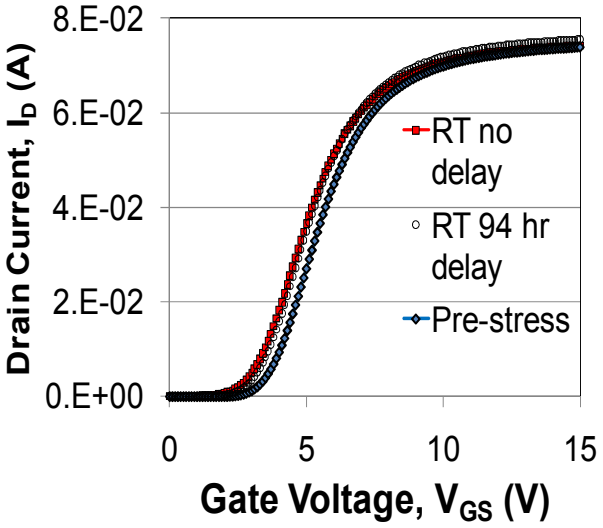

Figure 4. Effect of measurement delay time on the I_D-V_{GS} characteristics on a Group B MOSFET following NBTS.

the variation in response following a one-hour gate-bias stress at 150 °C with V_{GS} = –15 V for a representative device from Group B. The immediate and delayed measurements show a much smaller variation than devices from Group A, even when the delay in the second measurement is much greater—in this case 92 hours later. The initial V_T shifts to the left are reduced for devices from Group B, which results in some improvement in *OFF*-state drain leakage current. This is discussed further in Section III.C.2.

2) Measurement Sweep Direction

Next, we examine the effect of sweep direction on the transfer characteristics of SiC MOSFET devices following PBTS. As before, the stress bias and temperature were +15 V and 150 °C, respectively, although the bias stress time in this case was only 1,800 s. Pre-stress device characterization of the six devices from Group B for this part of the study yielded an average V_T of 3.59 V with a standard deviation of 0.07 V. In all of the pre-stress measurements, the gate was swept up from V_{GS} = 0 V to V_{GS} = +15 V.

The effect of sweep direction was determined by measuring ΔV_T and comparing the difference between sweeping up and sweeping down during the post-stress measurement. On average, we observed a ten percent larger shift for devices swept down in gate bias following the PBTS. This difference has been found to be much larger when the gate bias is swept up beginning at a negative value. The sensitivity of these results show again the importance of the bias applied during the measurement and how long that bias is applied, i.e., the sweep time. In comparing these results with those of Section III.B.1, it appears that sweep delay time is a more important variable than sweep direction.

3) Measurement Temperature

SiC MOSFETs are expected to operate reliably at junction temperatures approaching 150 °C. It becomes critically important to understand the effects of bias-temperature stressing on the high-temperature I_D-V_{GS} characteristics. In this section we examine the effects of a negative HTGB stress on both the room temperature and high temperature transfer characteristics of several Group A and Group B SiC MOSFETs. Fig. 5 and Fig. 6 show representative results for devices from Group A and Group B, respectively. Pre-stress characteristic curves were taken at both room temperature and 150 °C. The stress conditions for the NBTS test were V_{GS} = –15 V and T = 150 °C. Immediately following the stress, a sweep up of the gate was made in order to measure the change in the high-temperature transfer characteristics. The device was then rapidly cooled to room temperature under bias and the gate was again swept up to measure the device I_D-V_{GS} characteristics.

The high-temperature values for V_T are consistently about 1.5 V more negative than the corresponding room temperature values for all the

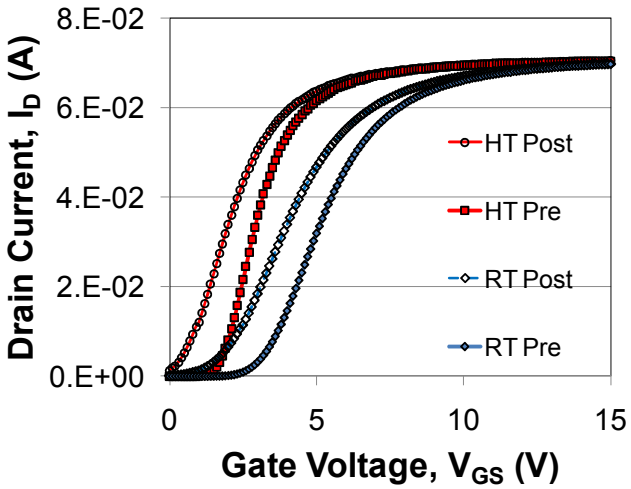

Figure 5. Comparison of transfer characteristics pre- and post-stress at high and room temperature – Group A.

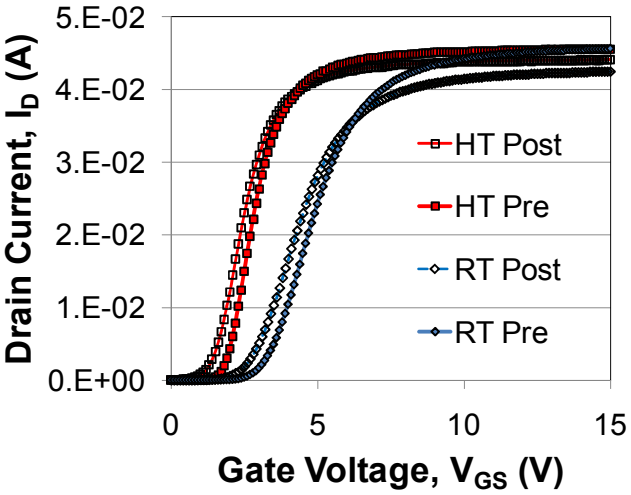

Figure 6. Comparison of transfer characteristics pre- and post-stress at high and room temperature – Group B.

devices tested, although slightly less following the NBTS. Comparing the pre- and post-NBTS results show an additional negative V_T shift of about 1.4 V for Group A devices and about 0.3 V shift for Group B devices, consistent with the PBTS results discussed in Section III.B.1.

As expected, the post-stress high-temperature curves show the largest negative shift of the I_D-V_{GS} characteristic as well as the largest increase in the *OFF*-state leakage current. Fig. 7 provides a summary of the room and high temperature leakage current results. The subthreshold characteristics for Group B devices are only moderately improved over devices from Group A even though ΔV_{GS} (for I_D = 1×10^{-6} A) is significantly less: a 1.5 V negative shift versus a 2.8 V shift, respectively. The subthreshold-voltage instabilities are typically larger than the linear V_T instabilities due to an increased stretch-out of the subthreshold slope under a negative bias stress [3]. The measured high temperature post-stress drain current at V_{GS} = 0 V was five orders of magnitude higher than the room temperature pre-stress drain current at V_{GS} = 0 V for devices from Group A, whereas devices from Group B exhibited an increase of approximately three to four orders of magnitude in drain-leakage current. The decrease in the pre-stress drain current between room temperature and 150 °C for Group B devices was due to the disappearance of an initial high edge leakage characteristic and not to any voltage shift.

C. Stressing Conditions

Section III.B discussed how variations in the measurement conditions affect the stress results. This section examines the effect of variations in the stress conditions themselves, specifically gate bias, temperature, and time.

1) Bias Stress Dependence

Fig. 8 is a plot of a series of I_D-V_{GS} curves measured on different devices having positive gate voltage stresses of 10, 12, and 15 V, along with a representative pre-stress curve for devices from Group A. The stress temperature and time for the PBTS are 150 °C and 1 hour, respectively. The post-stress curves shift further to the right with increasing bias-stress magnitude. A plot of the increase in ΔV_T with stress bias is shown in Fig. 9.

A similar study looking at variations in NBTS with a constant stress temperature and time of 150 °C and 1 hour, respectively, for negative gate voltage stresses of –5, –10, and –15 V were performed on devices from Group B. The negative shift of the I_D-V_{GS} characteristics increases, as expected, with larger negative stress biases. The measured V_T shift was only 0.02 V for V_{GS} = –5 V, whereas the V_T shift was 0.23 V for V_{GS} = –15 V. As previously discussed in Section III.B.1, the magnitude of the V_T shifts under NBTS for devices from Group B are less than similarly stressed devices from Group A.

2) Temperature Stress Dependence

The temperature dependence of the gate-bias stress is illustrated in Fig. 10, which shows a plot of ΔV_T as a function of stress temperature. ΔV_T was

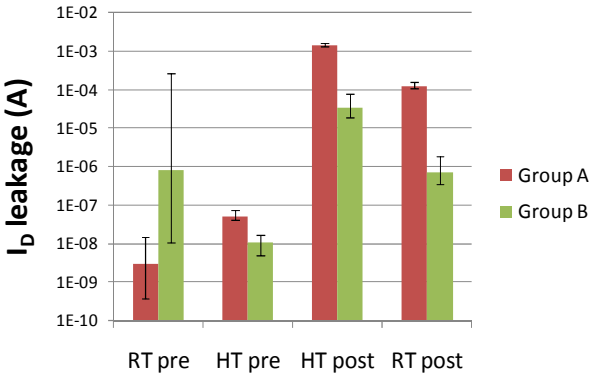

Figure 7. Comparison of pre- and post-stress room and high temperature drain leakage currents at V_{GS} = 0 V following NBTS (V_{GS} = –15 V; T = 150 °C) for devices from Groups A and B.

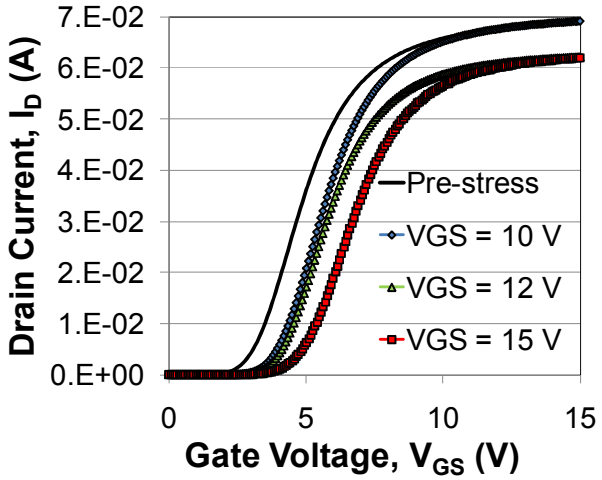

Figure 8. Bias dependence effect on the I_D-V_{GS} characteristics of Group A devices.

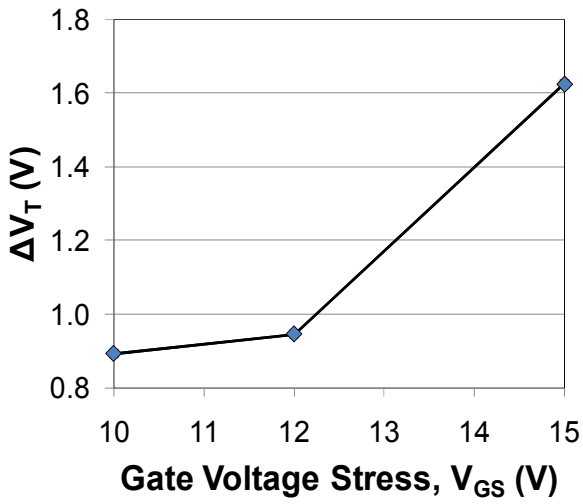

Figure 9. Dependence of V_T shift on stress bias for Group A devices with T = 150 °C and t = 1 hour.

calculated by taking the difference of the post- and pre-stress V_T values extracted from the measured I_D-V_{GS} curves, with a different device from Group B used for each stress temperature—which varied from 25 °C to 150 °C for a one hour NBTS with a constant gate-bias stress of –15 V. Clearly, the greater the stress temperature the larger the negative V_T shift, with a sharp increase observed above 100 °C. These results for NBTS are consistent with a report of previous results for a positive bias temperature stress [3], which attributed an increase in V_T instability to an increase in the number of active near-interfacial oxide traps (see Section III.A).

3) Stress Time Dependence

The time dependence of the bias-stress is illustrated in Fig. 11 for a 150 °C, –15 V negative bias temperature stress of a device from Group B. The individual bias stress times at temperature were 320 s, 1,000 s, 3,200 s, and 10,000 s. At the end of each NBTS, the device was cooled to room temperature under bias and an immediate I_D-V_{GS} measurement was made. Fig. 11 plots the drain current on a log scale to show the effect of bias stress time on the subthreshold device characteristics. Longer stress times result in larger negative shifts. The *OFF*-state leakage current taken at V_{GS} = 0 V increased from its pre-stress value of 3×10^{-8} A to 6×10^{-6} A after a cumulative stress time of approximately four hours.

Fig. 12 shows the corresponding smaller shift of the linear V_T value versus the log of the individual stress times. This underscores the importance of monitoring the subthreshold current under NBTS, which can increase more dramatically due to the stretch-out of the subthreshold slope and lead to significant increases in leakage current [3].

These results emphasize the importance of the bias stress time, which varies among the different existing standards. For example, the AEC standard [7] calls for a 1,000 hour HTRB and HTGB stress, whereas the Mil Std 750-E [6] only requires a 48 hour stress, at 80% of the maximum rated gate bias.

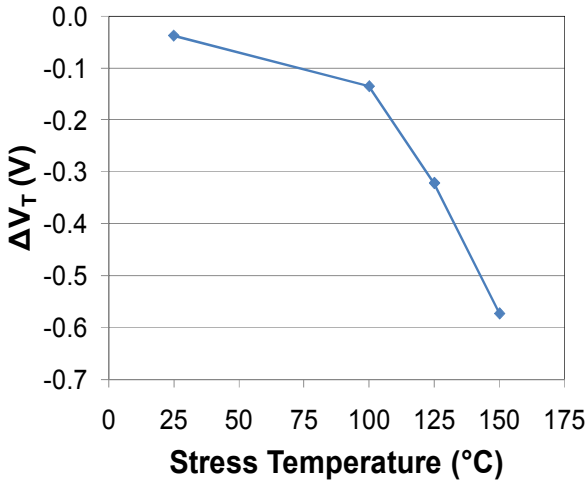

Figure 10. Dependence of V_T shift on stress temperature for Group B devices with V_{GS} = –15 V, t = 1 hour.

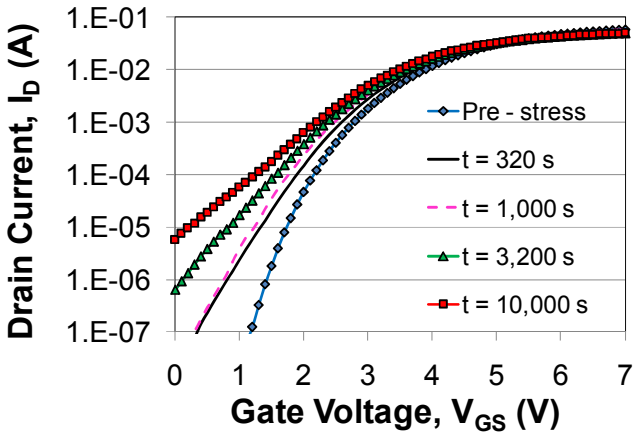

Figure 11. Time dependence of the subthreshold I_D-V_{GS} characteristics for a representative Group B device with V_{GS} = –15 V and T = 150 °C.

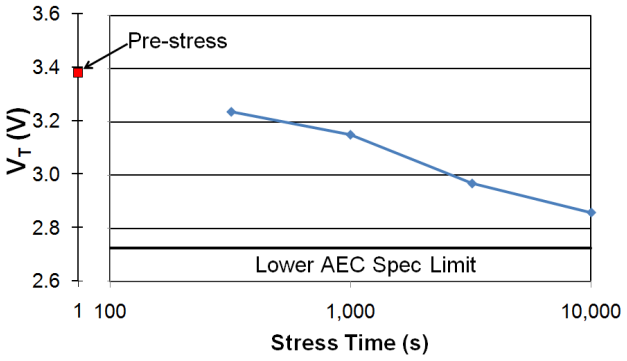

Figure 12. Dependence of V_T shift on stress time for a representative Group B device with V_{GS} = –15 V and T = 150 °C.

4) Effect of PBTS on the ON-state Characteristics

Finally, we examined the effect of PBTS testing on the ON-state characteristics (I_D-V_{DS}) for devices from Group B by applying a positive bias temperature stress (V_{GS} = +15 V, T = 150 °C). However, because of the large currents involved, a single room-temperature I_D-V_{DS} trace was made using a 371B Tektronix curve tracer by sweeping up in drain bias with a constant V_{GS} = +15 V applied during the temperature stress and cool down using an external DC power supply. Fig. 13 shows the effect of the PBTS on the ON-state characteristics for stress times of 24 and 92 hours. These results show an increase in the forward voltage drop ($V_{DS–ON}$) for increasing stress duration, especially at higher drain currents. If these devices are operated at I_D = 50 A (J_D = 125 A/cm^2), then the PBTS results in a 12 percent increase in $V_{DS–ON}$ for a 92-hour stress. This will result in greater ON-state power dissipation and an increase in the junction temperature, which may impact not only performance, but long-term device reliability as well.

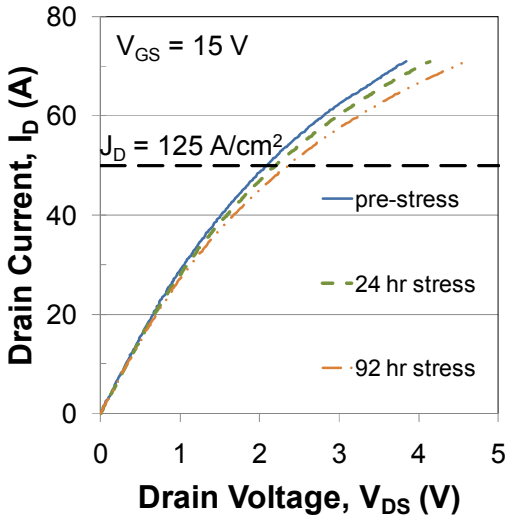

Figure 13. Effect of stress time on the I_D-V_{DS} characteristics of a representative Group B device with V_{GS} = + 15 V and T = 150 °C.

IV. Conclusions

This work has shown the large variation in the *I-V* and drain-leakage characteristics of SiC power MOSFETs due to variations in both measurement and stress conditions. Specifically, we have shown that the shift in the post high-temperature stress I_D-V_{GS} characteristics is strongly dependent on the measurement delay time, as well as the gate-sweep direction. Previous results have shown that the measurement speed is also of critical importance, with faster measurements revealing larger actual V_T shifts. Although the standards call for pre- and post-BTS measurements to be performed at room temperature, it is important to measure at the stress temperature as well since SiC power MOSFETs are expected to operate at these temperatures and the leakage current under negative bias stress is worse at elevated temperatures.

Similarly, we have shown that these shifts are highly dependent on the bias stress conditions, including bias magnitude, stress time, and temperature. Although all the standards call for testing at elevated temperature, there is a significant variation in the bias-stress time requirements, and some variation in bias magnitude requirements. Both variables have been demonstrated to be significant. In particular, a sharp increase in the magnitude of the V_T shift is observed with increasing stress time at temperatures above 100 °C.

We have shown that, as currently written, power device reliability testing standards such as those from JEDEC, AEC, and DoD do not place enough emphasis on constraining the conditions of measurement when evaluating a device parameter such as V_T. Seemingly minor alterations in measurement procedures, which can be in full compliance with a standard's specifications, may in fact produce vastly different results on a given device. In certain situations, the choice in

measurement parameters can make the difference between success and failure. It is therefore important that any standards used be mindful of the unique issues associated with SiC MOSFETs, especially as the technology matures.

For example, the 96 hour window between stress and measurement allowed by all three standards considered here appears to be unsuitable. More specifically, it is important that the existing standards be modified to require faster, and more immediate post-stress measurements with the gate-bias swept down following a positive bias stress, and that elevated temperature measurements be required as well. Otherwise, inconsistent pass/fail results may occur when applied to SiC power MOSFETs.

It is also critical that the bias-temperature-stress times be long enough to allow for the activation of all the elevated temperature mechanisms which may occur under actual operational conditions. Charge trapping effects will get worse, although for some devices this effect may be countered by mobile ion drift. It is also important to determine appropriate accelerated test conditions so that non-operational failure mechanisms are not introduced.

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