Impact of SiC Components on the EMC behaviour of a Power Electronics Converter

Eliana RONDON, Florent MOREL, Christian VOLLAIRE
Laboratoire Ampère (CNRS UMR 5005), Université de Lyon, Ecole Centrale de Lyon, 36 avenue Guy de Collongue 69134 Écully, France
Eliana.rondon-pinilla@ec-lyon.fr

Jean-Luc SCHANEN
G2ELab (CNRS UMR5269) Grenoble INP/UJF, Bat Ense3 BP.46, F-38402 SMH cedex Grenoble, France

***Abstract*— In this paper, the EMC behaviour of a switching cell is studied in a standardized environment, using both experiments and simulations. The environment model has been validated separately. The EMC emission using SiC JFET and Si MOSFET are compared. With the SiC JFET the simulation study shows a good agreement with the experiment up to 20MHz while with the Si MOSFET the validity domain of the model is less than 500kHz due to the simplistic model included in the SABER library. The experimental study shows that the EMC perturbations measured at the LISN are 10dB larger with the SiC JFET than with the Si MOSFET at a frequency range from 200kHz to 4MHz.**

I. INTRODUCTION

The recent technological progress of semiconductors and increasing demand for power electronic converters with new specifications such as high frequencies, high voltages, high temperatures and strong current densities have promoted SiC (Silicon Carbide) components to be developed and used more and more. However these components create new issues in Electromagnetic Compatibility (EMC) because of the conditions of high frequency switching and high commutation speeds (high di/dt and dv/dt) compared to other conventional components in power electronics. A precise study of the perturbations generated by the SiC components is therefore necessary.

The aim of this work is to predict levels of conducted emissions generated by a power electronics converter. Then the EMI spectrum of two technologies (SiC and Si components) are predicted and compared with experimental results in order to deduce the frequency range of the validity domain of the model. Conducted emissions with both components are also compared to quantify the impact on EMI of the use of SiC devices.

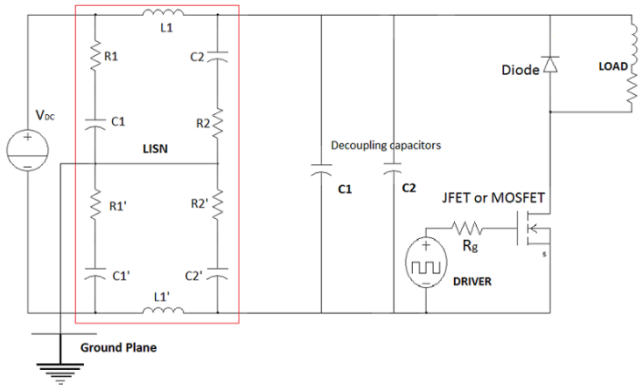


Figure 1. Considered converter

For the simulation study, not only the devices have to be taken into account. A realistic model for EMC must be identified for the passive and the parasitic elements [1,2]. In order to predict compliance to EMC standard, a LISN (Line Impedance Stabilization Network) must be included in the model.

In this paper a buck converter is considered (Fig. 1) as a basic switching cell. The active components (i.e. disturbances sources in EMC) are a Si Schottky diode (MUR1540), a Si MOSFET (IRFPG50) or a SiC JFET manufactured by SiCED/INFINEON Company. The models used for the diode and the MOSFET are provided in the Saber® [3] library. The SiC JFET model was developed in [4]. The characterisation of the SiC components must be made to readjust the electrical parameters of the model [4]. In section II, passive parts are modelled with equivalent electrical circuits. The considered parts are the load, the decoupling capacitors, the LISN, and finally the interconnections effects in tracks (inductive and capacitive). In section III, the model is compared to measurements. Firstly, the model including all passive parts is compared with impedance measurements in order to validate the stray elements. Secondly, the voltage in the 50Ω positive terminal

of the LISN is predicted in the Saber® simulation environment (time domain) and compared with the measurements. In section IV, a comparison of the emission levels for the two semiconductor components in Si and SiC are presented. Finally conclusions are presented in the section V.

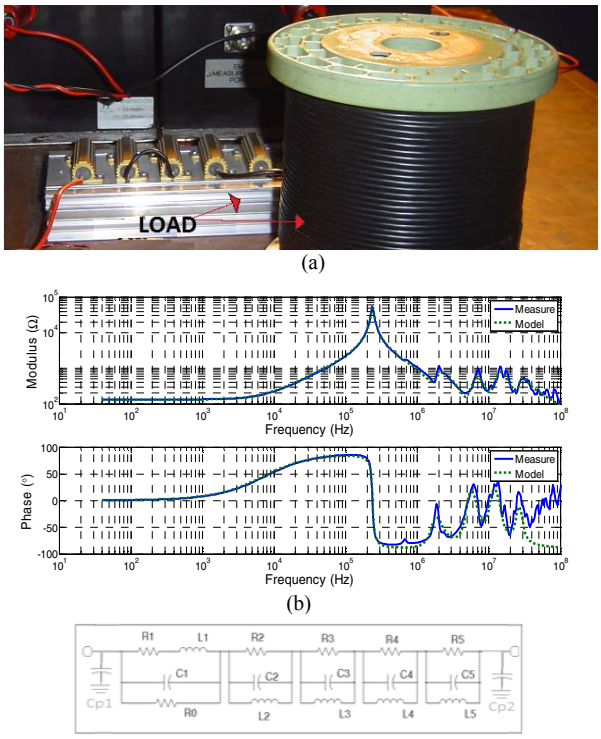
II. PASSIVE AND PARASITIC COMPONENTS MODELING

A. Passive components

For the passive components (load, decoupling capacitors and LISN) an impedance meter AGILENT 4294A was used to extract the frequency behavior of each component. The R, L load (Fig. 2) exhibits several resonances, due to technological realization. To take into account these multiple resonances, various R-L-C cells are included in the model.

An optimization algorithm (written in MATLAB) is used to compute the parameters of a proposed electrical model (deduced from the frequency behavior of the component) in order to minimize the difference between the measurement and the impedance of the model.

Figure 2 shows the measurement of the load with the impedance meter compared with the model.



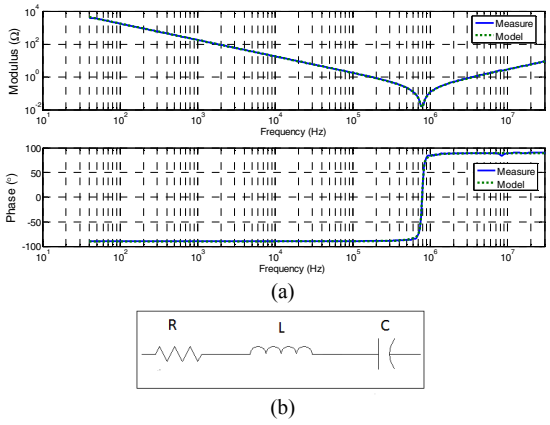
(a)

(b)

(c)

Figure 2. Load impedance: (a) module (b) measure and simulation (c) Model

Two decoupling capacitors are used: an electrolytic capacitor (C1) and a ceramic capacitor (C2). The electric model used for the decoupling capacitors is the conventional esr-esl-C. (Fig. 3).

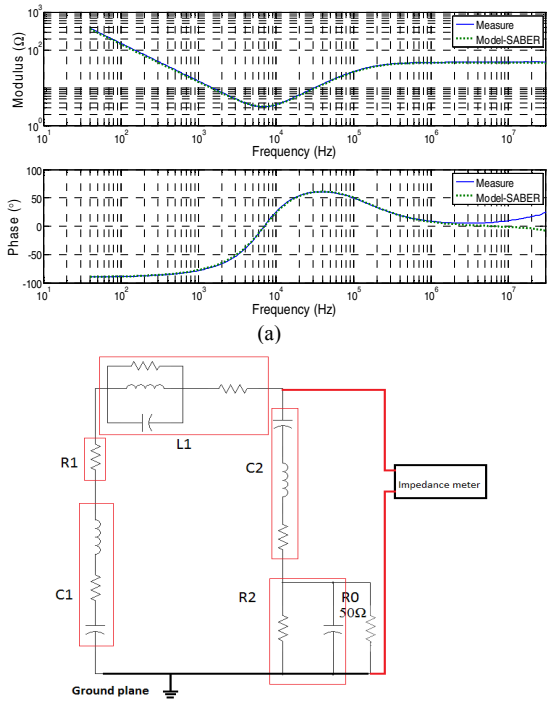


(a)

(b)

Figure 3. Impedance of a decoupling capacitor: (a) measure and simulation for the decoupling capacitor (b) Capacitor model

The LISN used is a "50A: Prana Tegam-50 Ohms-50uH". Its schematic is represented in Fig. 1. Even if this standard equipment is usually considered as perfect, each component was measured and an equivalent circuit model has been developed. Figure 4 shows the validation of the association of models for every component; including the cables which will be used between the LISN and the converter. We prove this way that couplings between components are negligible.



(a)

(b)

Figure 4. Impedance of the LISN: (a) measure and simulation (b) model

B. Parasitic elements

B.1 Inductive effects

The cabling model is very important in the converter design; it is responsible for the over-voltage across the

switch terminals due to the high di/dt generated during the switching step. Common mode current is also generated due to stray capacitive behaviour and large dv/dt.

The magnetic coupling, the skin effect and the proximity effect are all taken into account by modelling the tracks of the PCB with InCa3D® software [5], this version models only the inductive and resistive aspects based on PEEC method (Partial Element Equivalent Circuit) [6]. The capacitive behaviour will be added further. InCa3D® generates a matrix of impedances and the coupling with Saber® is automatically achieved using differential equations written in MAST language.

To better investigate the cabling influence in the converter behaviour, asymmetric and long tracks are used. With this design the disturbing effects are higher in the considered bandwidth. The considered board is presented in figure 5.

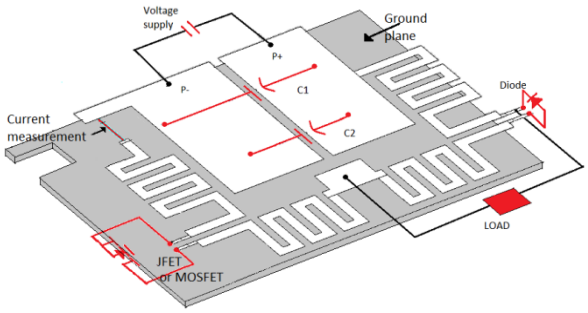
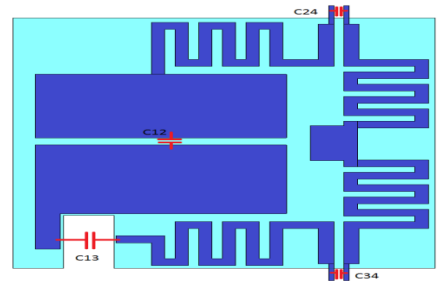


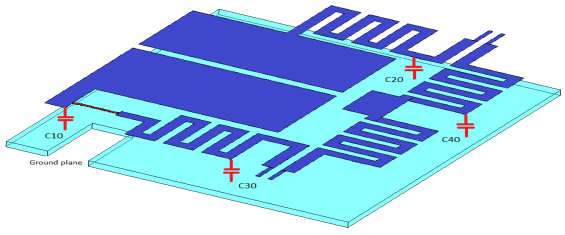
Figure 5. Circuit geometry

B.2 Capacitive effects

The stray capacitance offers a path to the common mode current. Four stray capacitances between tracks (Fig. 6a) and four between tracks and ground plane (Fig. 6b) are considered.



(a)



(b)

Figure 6. Stray capacitances: (a) between tracks (b) between tracks and ground plane

The values of parasitic capacitance depend on the geometry of the physical structure. Three formulations of the literature are used for the calculation, (the classical formula of paralleled plate condensators, Sakurai and Tamaru formula, method of conformal transformations) [7] and compared to measurements with the impedance meter.

The figure 7 shows the electrical model of the capacitances previously mentioned. These capacitances cannot be directly measured. Indeed when the impedance meter is placed between two points, it measures several capacitances associated in series and/or in parallel.

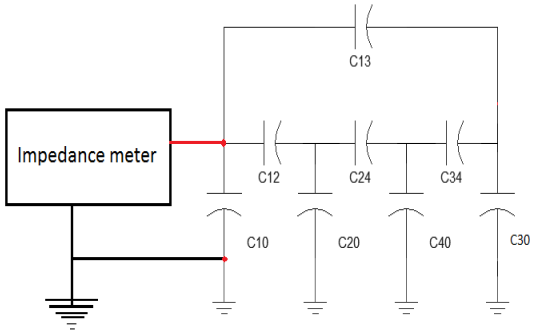
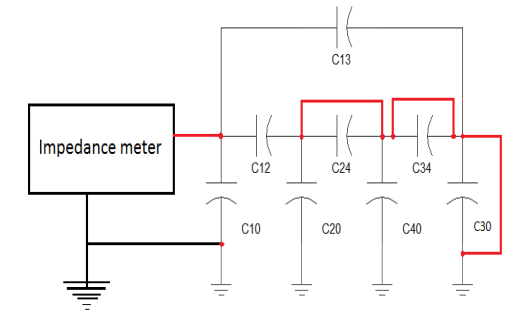


Figure 7. Electrical model of the parasitic capacitances when parasitic inductances are neglected

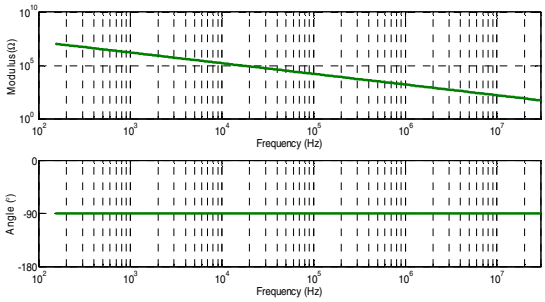
An adapted methodology has been used to obtain capacitance values. It consists in using short- or open-circuits between the cooper tracks. The impedance meter measures equivalent values. Figure 8a explains measurements realized to find the value of Ceq1 with an impedance meter. Some capacitances between tracks and between tracks and ground plane are plugged to the ground and others are circuits opened between the tracks, this association reduces the diagram from eight to three capacitances in parallel. The equation for this measurement is the following:

$$C_{eq1}=C_{13}+C_{10}+C_{12} \quad (1)$$

The value for the measurement of C_{eq1} is exposed figure 8b; the coupling is capacitive until a frequency of 30MHz.



(a)



(b)

Figure 8. Electrical model of the parasitic capacities for the measurement Ceq1 (a) Result of measurement with the impedance meter for Ceq1 (b)

Seven other measurements are performed then a set of linear equations is then obtained and solved to give the stray capacitances values.

Finally, the computation method that gives better results is Sakurai and Tamaru formula. This formula appreciates edge effects.

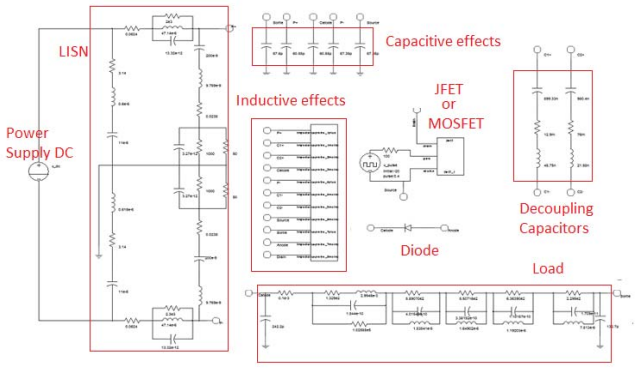
Since the stray capacitances between tracks have been found negligible compared to the capacitances between tracks and ground plan [8], only four stray capacitances have been integrated to the Saber® model.

Finally the presented method (simulation in InCa3D® for the inductive effects and the Sakurai Tamaru formula for the capacitive effects) allows the predicted parasitic effects of the routing without construction of a prototype.

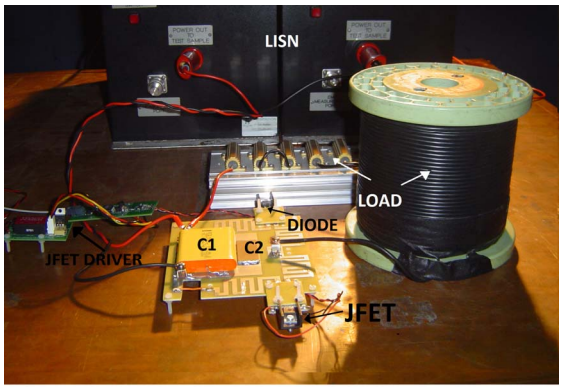
III. VALIDATION OF THE MODEL

A. Switch environment validation

To validate the model of the switching cell (Fig. 9b), impedance measurements have been carried out and compared with the Saber® model (Fig. 9a); all the parasitic elements are taken into account.



(a)



(b)

Figure. 9 Converter and LISN in the Saber® software (a) Buck converter module (b)

In the measurement configuration (Fig. 10a) the diode is replaced by a short circuit and the impedance "viewed" from the JFET or MOSFET is measured. Symmetrically, in another measurement, the JFET or MOSFET are replaced by a short circuit and measurements from the diode are realised. Finally, in another configuration, the impedance from the 50Ω resistor inside the LISN is measured; the active components are replaced by open- or short-circuit.

The comparison of the results for the first measurement configuration of the figure 10a is presented in the figure 10b. All measurements show good agreement between the models and the measurements. We confirm by this way that the couplings between components are negligible as the cable between LISN and the decoupling capacitors. It can be considered that the model of passive elements is valid for a wide frequency-range of 40Hz to 30MHz. The approach of passive and parasitic components is then valid for predicting the conducted disturbances.

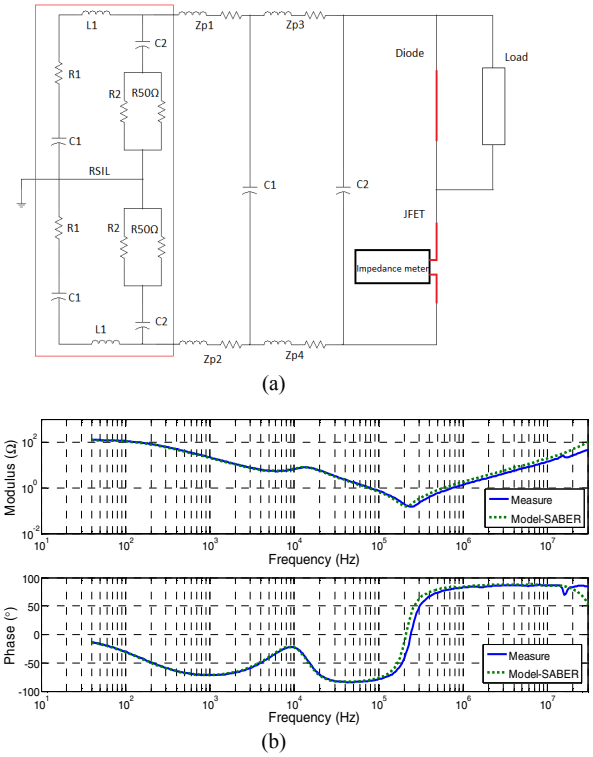


Figure 10. (a) One measurement configuration to validate the model of switches environment (b) Equivalent impedance measured and modeled

B. Simulated spectrum of electromagnetic interferences compared with measurements.

After this validation of the environment, the complete model of the converter is simulated in Saber® software. The model with the SiC and Si components (Fig. 9a) in the temporal domain, take into account the non linear behaviour of semiconductor components.

To validate the complete model of the switching cell (Passive and active elements), data measured in temporal domain with an oscilloscope (LeCroy HRO 66Zi) are compared to Saber model results. Then FFT are computed with Matlab. These measurements are made for the MOSFET and the JFET in the 50Ω resistor of the LISN.

To focus on the emission generated from the power part only, the semiconductor driver has been kept far away from the power module, as illustrated in Fig. 9.

B.1 Comparison between simulation and measurement with the SiC JFET.

The comparison of the spectrum is presented in Fig 11b. We note differences of less than 5dBµV at 2MHz and 5MHz. With the results of figures 10 and 11, the JFET's model can be considered valid up to 20MHz, because of the validity of the model of the passive elements all the differences can be to the models of the switching elements (diode & transistor).

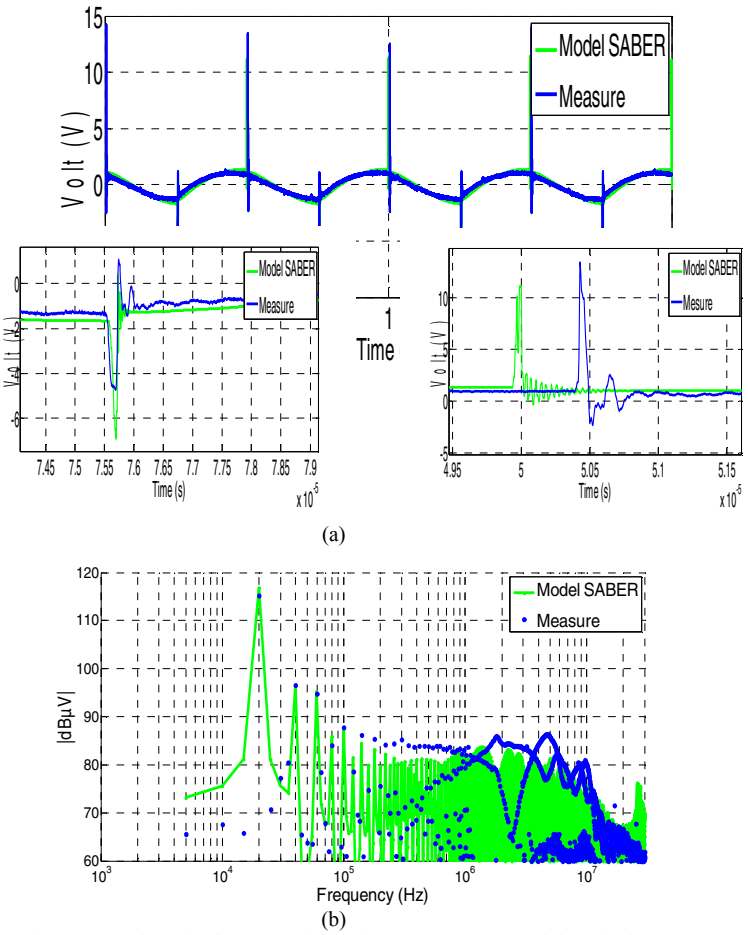


Figure. 11 Voltage in the LISN of the SiC JFET: (a) temporal domain (b) spectrum

B.2 Comparison between simulation and measurement with the Si MOSFET.

In figure 12a, voltage peaks are not well represented in the model. The figure 10b shows the comparison spectral for the voltage in 50Ω LISN resistor.

The model does not work for frequencies up to 500kHz. These results show that the used MOSFET model (included in the SABER library) is not adapted for EMC studies.

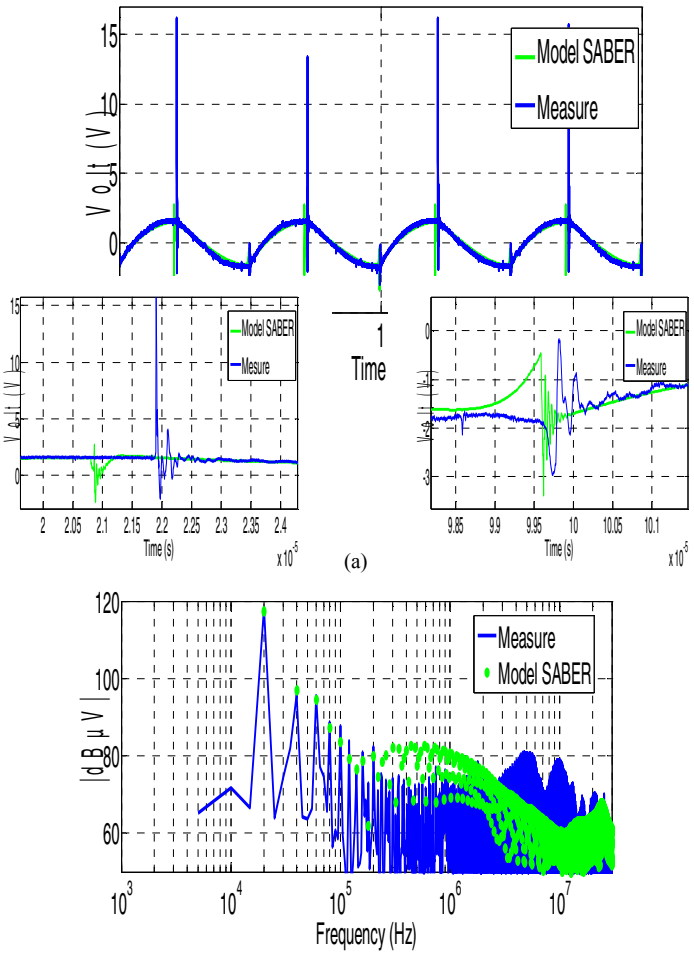


Figure. 12 Voltage in the LISN of the Si MOSFET: (a) temporal domain (b) spectrum

IV. COMPARISON OF MEASURED INTERFERENCES WITH THE JFET (SIC) AND THE MOSFET (SI)

Measurements in time domain are realized to compare the generated interferences for the two semiconductor components. The drain-source voltage is measured for the two components. The switching time for the JFET is 50ns while for the MOSFET is 690 ns.

The voltage in the resistance 50Ω of the LISN was equally measured. In the figure 13, the interferences of the JFET are about 10 dB higher that MOSFET (200KHz-10MHz).

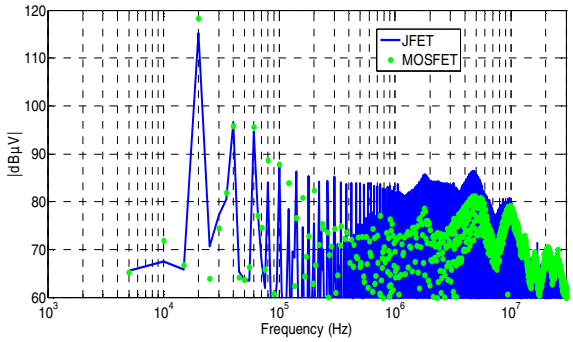


Figure. 13 Comparison of spectrum for two components

V. CONCLUSIONS

A method to take into account stray elements in a power converter has been presented. The impedance model is valid up to a frequency of 30 MHz.

The complete model of the converter (passive components, stray elements, SiC and Si components) was simulated in the Saber® environment in time domain and confronted with measurements. This model allows forecasting the conducted EMI spectrum up to 20 MHz. For the MOSFET, the range of validation of the component model is limited; the MOSFET model (Model SABER library) is not adapted, a particular care must be took to semiconductors models to increase the validity range.

The presented model allows the prediction in EMC without realizing a prototype. Indeed, once modelled, the RSIL can be used for various converters. It is necessary to create a library of passive components (load, decoupling capacitors, filters) to be implemented easily in the model. The cabling model is developed with InCa3D® to the inductive effects with the PEEC method. Analytical calculations for the capacitive effects are made with Sakurai and Tamaru formula. To conclude the methodology previously presented, this is necessary to have a library of semiconductors elements in SiC and Si which modelled correctly the components behaviour.

Finally, comparisons of the interferences between SiC and Si components show that JFET's commutation times are shorter that MOSFET's ones; this factor generates a raise of disturbances in the range of frequency of EMC standards. Future works will be dedicated to the modelling of the gate driver and the study of its impact on EMI.

VI. ACKNOWLEDGMENT

This work is financed by a doctoral fellowship from Rhone-Alpes Region.

VII. REFERENCES

[1] P. Musznicki, J-L. Schanen, B. Allard, "Accurate modeling of layout parasitic to forecast EMI emitted from a DC-DC converter", *IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, pp. 278-283, 2004

[2] N. Doorgah, C. Vollaire, F. Costa, N. Gazel, and R. Meuret,"EMI circuit modeling of a power train on composite ground plane," *Electromagnetic Compatibility (EMC), 2010 IEEE International Symposium on*, vol. 2, 2010, pp. 643-646.

[3] *AIM User Guide, Version* W-2004.12, Saber® & CosmosScope™ December 2004.

[4] H. Morel, Y. Hamieh, D. Tournier, R. Robutel, F. Dubois, D. Risaletto, C. Martin, D. Bergogne, C. Buttay, and R. Meuret, "A Multi-Physics Model of the VJFET With a Lateral Channel", Proceedings of the IEEE 14th European Conference on Power Electronics and applications-EPE, Royaume-Uni, 2011.

[5] Flux3D®, Cedrat, website. [online]. Avalaible: www.cedrat-groupe.com

[6] C. Martin, JL. Schanen, R. Pasterczyk "Power integration: electrical analysis of new emerging package", EPE`03, Toulouse, France.

[7] S.R. Nelatury, M.N.O. Sadiku, and V.K. Devabhaktuni, "CAD Models for Estimating the Capacitance of a Microstrip Interconnect: Comparison and Improvisation", *PIERS Proceedings, Prague, Czech Republic*, pp. 18-23, 2007

[8] V. Ardon, J Aime, O. Chadebec, E. Clavel, "MoM and PEEC Method to Reach a Complete Equivalent Circuit of a Static Converter", EMC Zurich, Suisse, 2009