

Investigation of 1.2 kV SiC MOSFET for High Frequency High Power Applications

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Abstract—SiC is among the most promising materials for next generation power electronic devices due to its superior physical properties to Si and relative mature technology. SiC MOSFET is expected to offer performance improvement over Si counterpart. This paper presents the characterization of 1.2 kV SiC MOSFET, including its static and dynamic characteristics, and its high-frequency (1 MHz), high-power (1.2 kW) zero-voltage switching (ZVS) operation in a half-bridge parallel resonant converter. In comparison with SiC JFET and Si CoolMOS, the advantages and disadvantages of the SiC MOSFET are summarized.

I. INTRODUCTION

Si-based power semiconductor devices have dominated the power electronics applications for decades. However, with increasing demand for high-frequency, high-voltage and high-temperature applications, Si power devices are now facing material limits. Wide Band Gap (WBG) materials, defined as semiconductors with bandgaps greater than 1.7 eV, promise superior performance in power devices. Among different WBG materials, in light of the development status, SiC is the most promising alternative to Si. SiC has an order of magnitude higher breakdown electric field than conventional materials, Si or GaAs, indicating that the power devices made of SiC can withstand much higher voltage stress with much lower on-resistance. Meanwhile, the large band gap energy of SiC also results in a much higher temperature capability and higher radiation hardness. Furthermore, SiC has a higher thermal conductivity, which leads to important benefits for power dissipation, and higher power handling capability [1]-[7].

Although SiC materials have superior characteristics, the system impact of SiC devices must be carefully studied, given their high cost, different size and package characteristics. Currently, only SiC Schottky diodes can be obtained commercially. Among the SiC active switches, SiC JFET, has been reported in many literatures, including modeling, characterization, and system applications [8]-[14]. Due to its normally-off feature and successful applications of Si power MOSFET, SiC MOSFETs are becoming the center of attention and expected to deliver superior performance over Si counterparts. In order to investigate SiC MOSFET for high-frequency, high-power applications, this paper fully characterized the static and dynamic characteristics of an 1.2 kV SiC MOSFET engineering sample, and compared it with a

state-of-the-art 600 V Si CoolMOS. A 1.2 kW 1 MHz parallel resonant converter is achieved with SiC MOSFET.

This paper starts with the static properties of SiC MOSFET characterization in Section II. The dynamic characteristics, including switching performance and body diode reverse recover performance, are presented in Section III. The operation and comparison between SiC MOSFET and Si CoolMOS resonant converters are provided in Section IV. The final comparison results are discussed and summarized in the final section

II. SiC MOSFET STATIC CHARACTERISTICS

The 1.2 kV SiC MOSFET prototype with $4.1 \times 4.1 \text{ mm}^2$ shown in Fig. 1 is developed by Cree. Since very limited information of the prototype was provided with the device, the device is fully characterized. The key static characteristics, including on-resistance, device parasitic capacitance and gate threshold voltage, are presented in this section.



Figure 1. 1200V SiC MOSFET sample from Cree.

a) On-resistance

The on-resistance $R_{ds(on)}$ of the MOSFET measurement is based on the slope of the output characteristics in the linear region. Therefore, the measured resistance is the minimum possible resistance for a given V_{gs} . Unlike commercial high voltage Si MOSFET, the $R_{ds(on)}$ of SiC MOSFET is still significantly influenced by the V_{gs} when it is over 10V. Fig.2 shows the relationship of on-resistance vs. temperature at different gate voltages. High gate drive voltage is preferred for

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low on-resistance, but it is limited by the gate breakdown voltage.

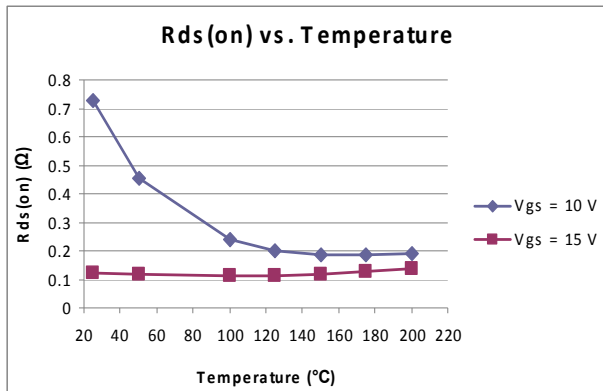


Figure 2. SiC MOSFET on-resistance vs. temperature at different gate voltages.

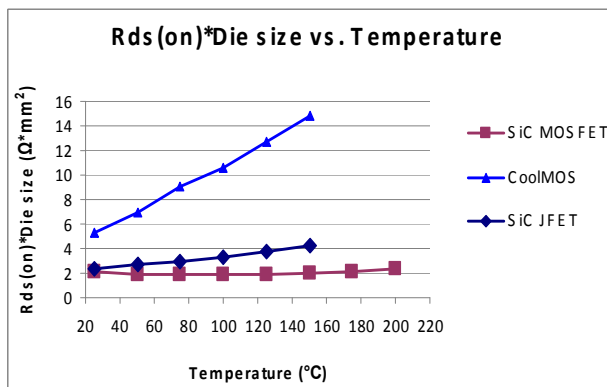


Figure 3. Comparison of specific on-resistance among 1.2 kV SiC MOSFET, 1.2 kV SiC JFET and 600 V CoolMOS.

Fig.2 also shows one of the interesting features of the SiC MOSFET, i.e. its high-temperature on-resistance. Fig. 3 shows the comparison of specific on-resistance at different junction temperatures among 1.2 kV SiC MOSFET, 1.2 kV SiC JFET(2.4 x 2.4 mm²) [15] and 600 V Si CoolMOS [16]. Even compared with low voltage rating Si CoolMOS, SiC power devices still show their obvious advantage on on-resistance. The SiC MOSFET and SiC JFET of the same voltage rating have very close on-resistance at room temperature. However, the on-resistance of SiC JFET is doubled at 150 °C while the on-resistance of SiC MOSFET remains the same as at room temperature. For SiC MOSFET, there is an initial decrease in $R_{ds(on)}$ at low temperatures as the temperature increases, which is followed by an increase in $R_{ds(on)}$ at higher temperatures. This behavior in the $R_{ds(on)}$ of the 1.2 kV SiC MOSFET is due to the different behavior at different temperatures of the three primary resistances in the SiC MOSFET: 1) channel resistance; 2) JFET resistance; and 3) drift layer resistance. The channel resistance decreases with increasing temperature due to the reduction in threshold voltage and simultaneous increase in channel mobility. Both the JFET resistance and the drift layer resistance, on the other hand, increase with increasing temperature due to increased phonon (lattice vibration) scattering of the electrons. At lower temperatures, the channel resistance actually decreases faster with increasing temperature than the combined effect of increasing JFET

resistance and drift layer resistance, thereby causing in initial decrease in overall on-resistance for the SiC MOSFET. At higher temperatures, however, the increasing JFET resistance and drift layer resistance begins to dominate, resulting in an increase in resistance for the 1.2 kV SiC MOSFET.

b) Device capacitance (C_{iss} , C_{oss} , C_{rss})

The input capacitance C_{iss} , output capacitance C_{oss} , and reverse transfer capacitance C_{rss} were measured using the impedance analyzer according to the methods introduced in [17]. The impedance analyzer applied a 50 mV, 1 MHz small signal for all measurements. Figure 4 shows the measured device capacitance at different drain-to-source voltages. The device capacitance is also measured at different temperatures. The variations of device capacitances are negligible at different temperatures.

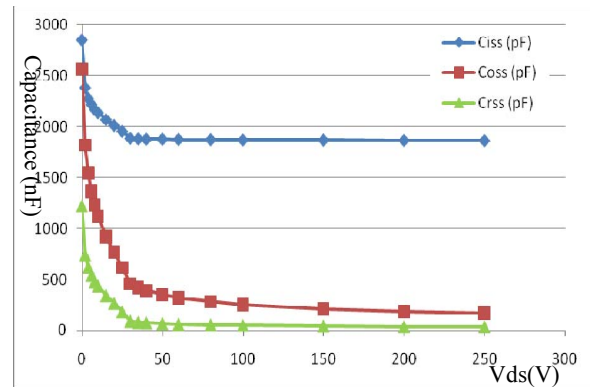


Figure 4. Non-linear capacitances, $C_{iss}/C_{oss}/C_{rss}$.

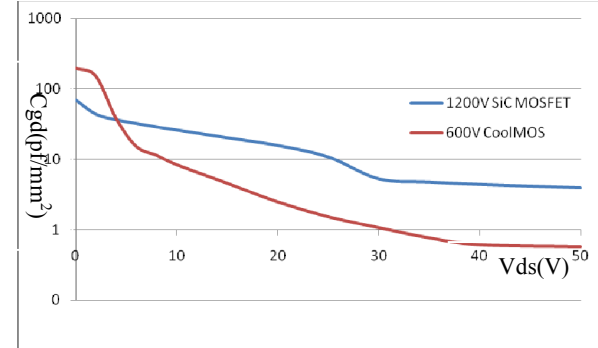


Figure 5 Comparison of C_{gd} capacitance densities.

The SiC MOSFET capacitances are compared with 600V CoolMOS after they are divided by die area. Figs 5-7 show each capacitance density (capacitance per mm²) comparison of gate to drain capacitor (C_{gd} or C_{rss}), gate to source capacitor (C_{gs}) and drain to source capacitor (C_{ds}) between 1200 V SiC MOSFET and 600 V CoolMOS. Due to the large SiC breakdown electric field, the SiC power device can be made with much thinner drift region. Though the thin die help reduce the on-resistance, it increases the capacitances. Even the blocking voltage of SiC MOSFET is two times of Si CoolMOS in this comparison, the SiC MOSFET capacitance densities of C_{gd} and C_{ds} are much larger the Si CoolMOS. Since the blocking voltage has little effect on C_{gs} , the

capacitance densities of C_{gs} of the two devices are very close compared with C_{gd} and C_{ds} . The relatively large C_{gd} will induce undesired large miller charge. With the measured capacitance data, the curve can be described by a curve fitting equation. The charged energy is the integration of the capacitance curves over V_{ds} . The ratio of miller charge (Q_{gd}) to input charge (Q_g) would be of use for gate drive design. Fig. 8 shows the comparison of the ratios. Considering the high voltage applications, the SiC MOSFET has worse conditions for gate drive design.

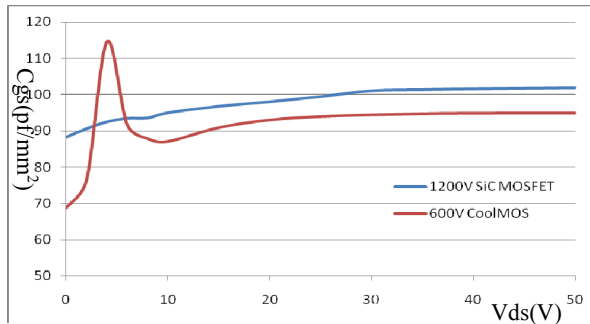


Figure 6. Comparison of C_{gs} capacitance densities.

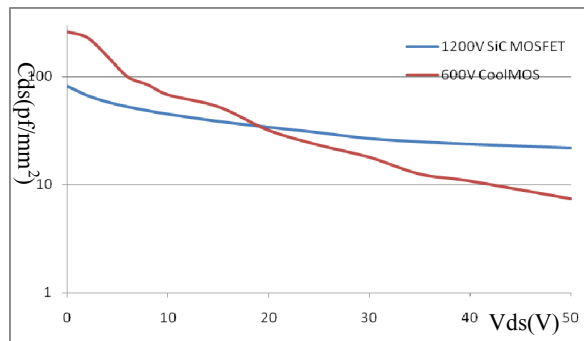


Figure 7. Comparison of C_{ds} capacitance densities.

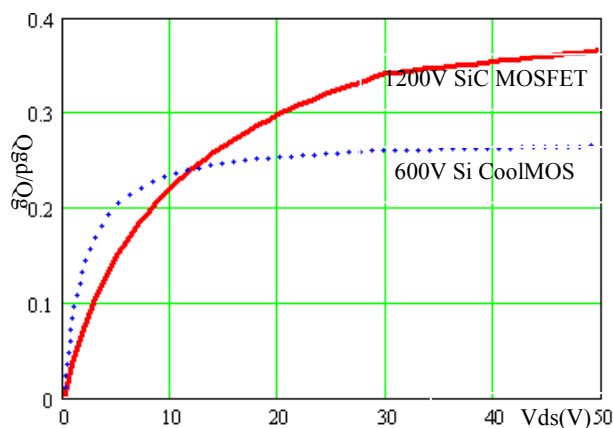


Figure 8. Comparison of the ratios of miller charge to input gate charge.

c) Threshold voltage

The unstable gate threshold voltage has been a concern for SiC MOSFET. The threshold voltage measurement has many criteria. A commonly used criterion for determining threshold voltage is the gate-source voltage level that produces 250 μA

of drain current when the drain and gate terminals are shorted. Using this criterion, the threshold voltage was determined as shown in Fig. 9. The lowest threshold voltage is around 1.5V at 150 $^{\circ}C$. The low threshold voltage at high temperatures can explain why the on-resistance will reduce initially to some extent as the temperature increases. Though it is relatively low compared with commercial high voltage Si MOSFET (typically around 4V), it keeps stable at different temperatures. It should be noted that attention need to be paid on gate drive design to avoid false trigger when the gate threshold voltage is decreased and the ratio of C_{gd}/C_{gs} is increased.

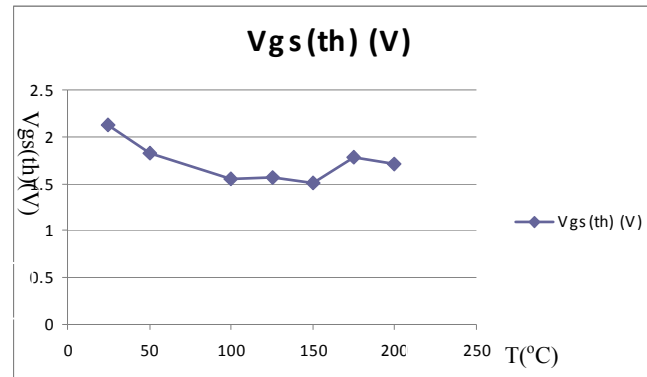


Figure 9. SiC MOSFET threshold voltages at varied temperatures.

III. SiC MOSFET DYNAMIC CHARACTERISTICS

The static characteristics data is not sufficient for converter design and operation. The switching characterization is tested with double pulses under inductive load. During the first pulse the inductor current is charged to the desired value, and the falling edge of this pulse and the rising edge of the following pulse are corresponding to the turn-off and turn-on switching transients of the device under test (DUT), at any desired voltage and current levels. The schematic of the double pulse test is illustrated in Fig. 10.

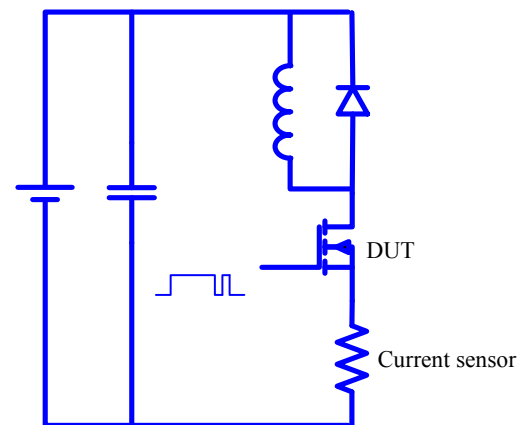


Figure 10. Schematic of double-pulse test.

When designing test circuit board, care must be taken to minimize parasitic inductance in the bus voltage path in order to avoid high switching spikes, and to minimize parasitic inductance in the gate drive path as well. High switching spikes can cause false trigger and also wrong measurements

especially when gate resistance is small. Besides the parasitic inductance, the parasitic capacitances should also be minimized. The capacitances in parallel with the inductor, including the inductor stray capacitance, freewheeling diode parasitic capacitance and PCB board parasitic capacitance, influence the turn-on spike while the capacitance in parallel with the DUT influence the turn-off spike. In order to minimize the parasitic capacitance, low current rating freewheeling diode and a single layer inductor winding are desired.

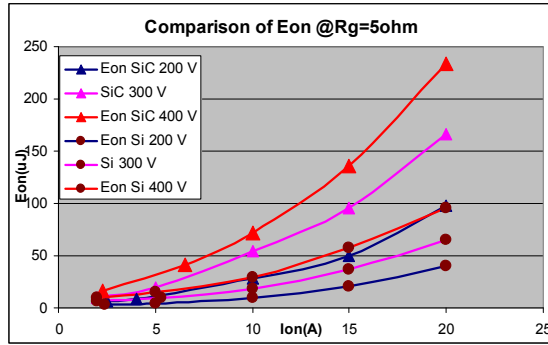


Figure 11. Turn-on loss energy comparison between SiC MOSFET and Si CoolMOS.

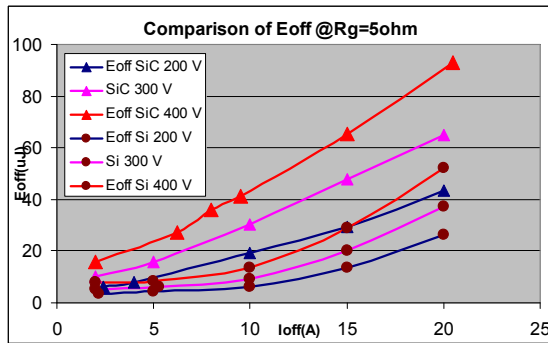


Figure 12. Turn-off loss energy comparison between SiC MOSFET and Si CoolMOS.

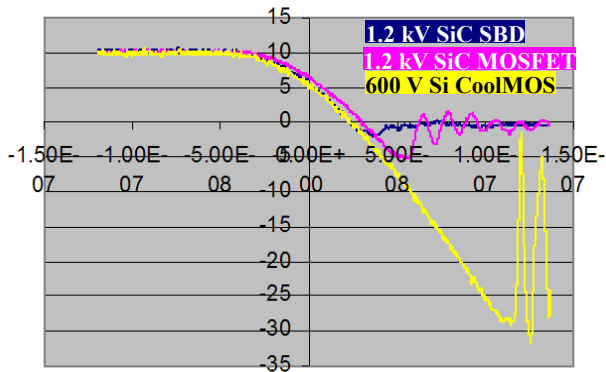


Figure 13. Body diode reverse recovery time (trr) comparison among 1.2 kV SiC SBD, 1.2 kV SiC MOSFET and 600 V Si CoolMOS.

The switching characterization was done for voltage up to 800 V, current up to 20 A and gate resistance from 1 to 30 Ω . The switching power loss of SiC MOSFET is shown in Figs. 11 and 12, as well as that of Si CoolMOS for comparison. The

switching power loss was calculated by the integration of the instantaneous power waveform (drain-source voltage waveform multiplied by drain current waveform). It is seen that the SiC MOSFET has a larger turn-on and turn-off switching loss than Si CoolMOS.

Another critical property is the SiC MOSFET body diode reverse recovery time (trr). The inferior performance of the Si MOSFET body diode is the main bottleneck for high-frequency application with ZVS operation [18]. At present, the commercial high-voltage Si MOSFET, even with a so-called fast reverse-recovery body diode, has a trr around hundreds of nanosecond at room temperature, which significantly restricts high-switching-frequency operation. The SiC MOSFET body diode reverse-recovery time measurements prove that it has a significant improvement on trr performance, with only about 40 ns reverse-recovery time at 25 $^{\circ}\text{C}$ which is even comparable with the performance of SiC Schottky diode (SBD), shown in Fig. 13. The low trr is mainly a result of the very small minority carrier lifetime as well as the thin drift layer. Furthermore, unlike the trr of Si device, the trr for SiC is relatively independent of temperature.

IV. HIGH FREQUENCY CONVERTER DEVELOPMENT AND OPERATION

Fig. 14 shows the topology used for power MOSFET system test. Since the purpose of the test is to evaluate the power switch's high-frequency operation, no rectifier bridge parallel resonant converter (PRC) is needed in the output. The converter with SiC MOSFET successfully operates at 1 MHz 1.2 kW with ZVS operation and 800V input voltage. The key waveforms of system test are shown in Fig. 15 and Fig. 16 for Si CoolMOS and SiC MOSFET respectively. Due to the low voltage rating of Si CoolMOS, the Si converter accordingly operates with 400 V input voltage while delivering the same power and voltage to load at 1 MHz switching frequency as the converter with SiC MOSFET. Figure 17 shows the ZVS turn-on waveform of SiC MOSFET and Figure 18 shows its turn-off waveform. With ZVS operation, the Vds and Vgs are very clean, but higher gate breakdown voltage is still desired for a reliable margin.

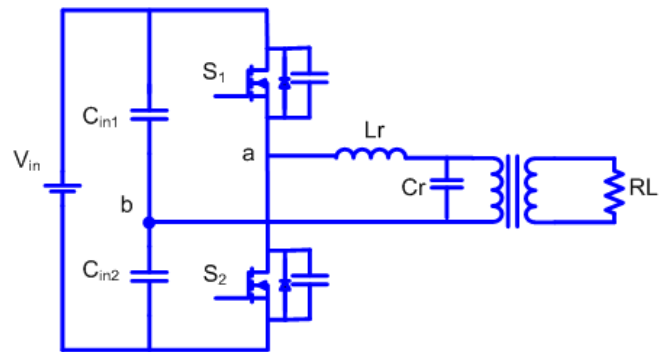


Figure 14. Half-bridge parallel resonant converter for SiC MOSFET high switching frequency operation.

Based on components temperature and efficiency measurements, Fig. 18 shows the power loss comparison between Si CoolMOS and SiC MOSFET. Fig. 19 shows the junction temperature. The low junction temperature of SiC

MOSFET is mainly contributed by its metal case and SiC high thermal conductivity as well as slightly lower power loss.

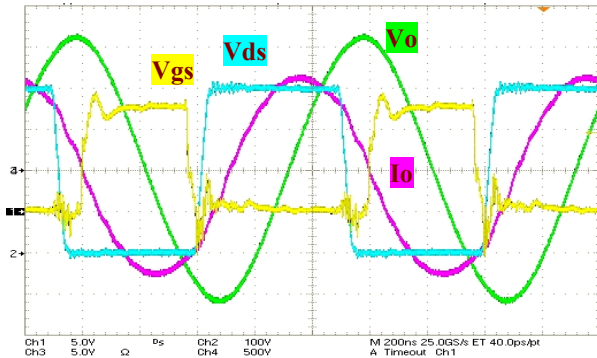


Figure 15. Main waveforms of converter with Si CoolMOS at 1.2 kW 1MHz.

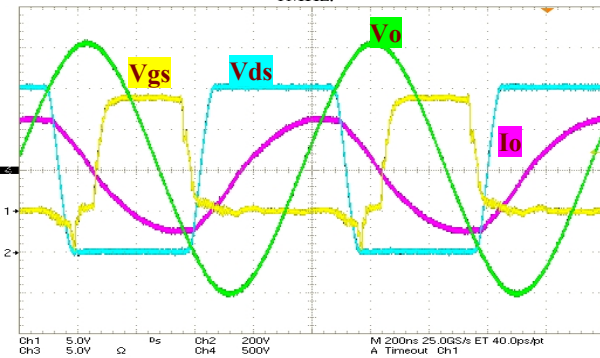


Figure 16. Main waveforms of converter with SiC MOSFET at 1.2 kW 1MHz.

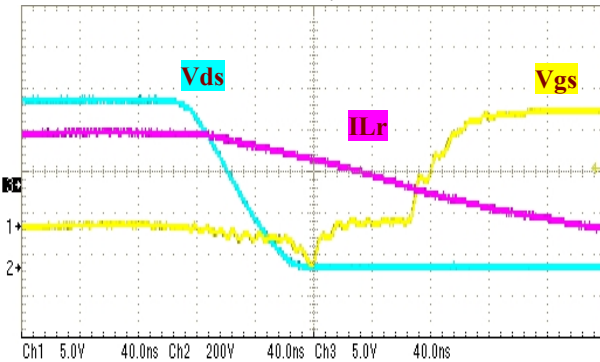


Figure 17. ZVS operation with SiC MOSFET at 1.2 kW 1MHz.

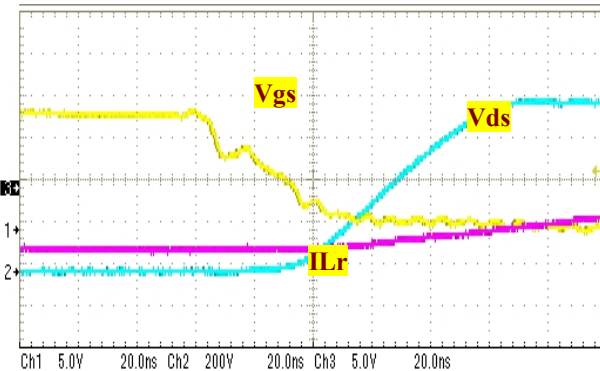


Figure 18. Turn-off waveform of converter with SiC MOSFET at 1.2 kW 1MHz.

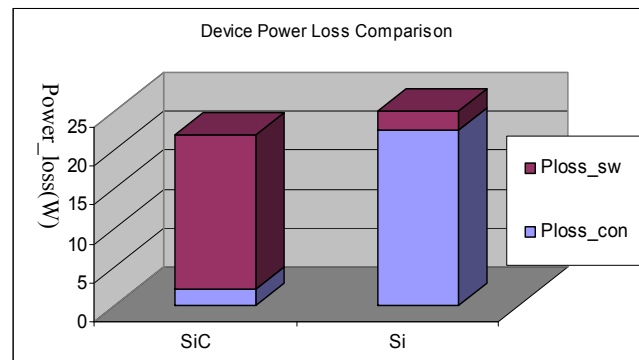


Figure 19. Power loss comparison between Si CoolMOS and SiC MOSFET.

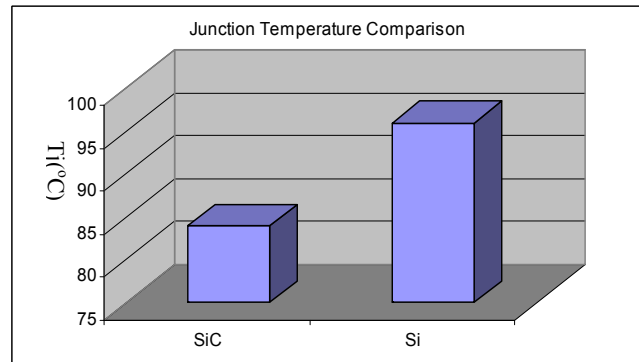


Figure 20. Junction temperature comparison between Si CoolMOS and SiC MOSFET.

Since the conduction loss can be calculated more accurately, the switching loss is obtained with the available total power loss and conduction loss. As the device characterization test shows, the SiC MOSFET has an obvious advantage on conduction loss due to low on-resistance and low conduction current due to the high input voltage when the converters are designed for the same power level and different input voltages, but it suffers high switching loss compared with Si CoolMOS. The system test results are consistent with the device testing results. Higher power or higher switching frequency can be expected when utilizing the high junction temperature margin of SiC MOSFET.

V. CONCLUSIONS

The 1.2 kV SiC MOSFET is fully characterized and applied successfully in a 1 MHz 1.2 kW converter with ZVS operation. For high switching frequency operation, thermal constraint is the practical issue. Although SiC MOSFET suffers relatively large switching loss partly due to larger capacitance density (capacitance per die size), it has a lower total power loss with its superior on-resistance. In addition, SiC MOSFET has a higher power loss handling capability due to its high thermal conductivity and high junction temperature which is limited by the current package technology. When ZVS is desired in high switching frequency applications, the fast reverse recovery time of SiC MOSFET body diode makes it an unbeatable alternative to Si counterpart for high switching frequency ZVS operation.

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