

AlSb/InAs HEMT's for Low-Voltage, High-Speed Applications

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Abstract—The design, fabrication, and characterization of 0.1 μm AlSb/InAs HEMT's are reported. These devices have an $\text{In}_{0.4}\text{Al}_{0.6}\text{As}$ /AlSb composite barrier above the InAs channel and a p^+ GaSb layer within the AlSb buffer layer. The HEMT's exhibit a transconductance of 600 mS/mm and an f_T of 120 GHz at $V_{DS} = 0.6$ V. An intrinsic f_T of 160 GHz is obtained after the gate bonding pad capacitance is removed from an equivalent circuit. The present HEMT's have a noise figure of 1 dB with 14 dB associated gain at 4 GHz and $V_{DS} = 0.4$ V. Noise equivalent circuit simulation indicates that this noise figure is primarily limited by gate leakage current and that a noise figure of 0.3 dB at 4 GHz is achievable with expected technological improvements. HEMT's with a 0.5 μm gate length on the same wafer exhibit a transconductance of 1 S/mm and an intrinsic $f_T L_g$ product of 50 GHz- μm .

Index Terms—InAs, MODFET's, quantum wells, semiconductor device fabrication, semiconductor device noise.

I. INTRODUCTION

THE material properties which have the greatest impact on the high-speed performance of HEMT's are the sheet charge density in the 2-DEG and the effective electron velocity in the channel. In recent years this has led to the increased use of $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel HEMT's with higher and higher mole fractions of In. Increasing the In concentration results in higher electron mobility and velocity in the channel and a larger conduction-band offset which leads to a higher sheet charge density. $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel HEMT's with an In content of over 50% are typically grown on an InP substrate rather than a GaAs substrate due to the better lattice match with InP. Compared to GaAs-based HEMT's, InP-based HEMT's have clear millimeter-wave performance advantages and currently hold the records in frequency response and noise figure for any three-terminal semiconductor device [1]–[3]. However, InP-based pseudomorphic HEMT channel designs with substantially higher In content than the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ lattice-matched composition have increased restrictions on layer thickness due to lattice mismatch. Therefore, the improvement in the channel transport properties in these devices has been limited by deleterious lattice strain effects and interface scattering.

In this work, HEMT's which have only InAs as the channel material have been investigated using the

TABLE I
FET CHANNEL MATERIAL PROPERTIES

	InAs	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	GaAs	InP
Electron Effective Mass (m^*/m_0)	0.023	0.041	0.067	0.077
Electron Mobility ($\text{cm}^2/\text{V}\cdot\text{sec}$ @ 300K, $N_D=10^{17}\text{cm}^{-3}$)	16000	7800	4600	2800
Γ -L Valley Separation (eV)	0.9	0.55	0.31	0.53
Electron Peak Velocity (10^7cm/sec)	4.0	2.7	2.2	2.5
Energy Bandgap (eV @ 300K)	0.36	0.72	1.42	1.35

$\text{Al}_x\text{Ga}_{1-x}\text{Sb}_y\text{As}_{1-y}/\text{InAs}$ material system, where the lattice constant is near 6.1 Å. These HEMT's have potential for low-voltage, high-speed applications due to better InAs properties and the larger conduction band offset at the AlSb/InAs heterojunction. Since these devices were first proposed [4], considerable progress has been reported for gate lengths of 0.5 μm or longer [5]–[9]. However, further development is required to realize the full potential of this material system. In this paper, three key design issues are addressed, namely the reduction of the gate leakage current, the elimination of the kink effect, and the formation of recessed 0.1 μm gates. The dc, small-signal, and microwave noise characteristics of 0.1 μm HEMT's which have improved low-voltage, high-speed performance are presented.

II. MATERIAL PROPERTIES AND GROWTH

Typical values of the key material properties for InP, GaAs, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and InAs are listed in Table I. With the smaller electron effective mass of InAs, higher electron mobilities are attained. Furthermore, due to the large Γ -L valley separation, InAs has the advantage of a higher electron peak velocity compared to the other listed semiconductors [10]. Compared to $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel HEMT's, the considerably larger conduction band discontinuity (1.35 eV) of the AlSb/InAs heterojunction enables the formation of a deeper quantum well with the associated benefits of a larger 2-DEG sheet charge density, superior carrier confinement, and improved modulation efficiency. The AlSb/InAs system has an advantage in the room-temperature mobility which can be achieved for a given 2-DEG sheet charge density. A sheet resistance as low as 40 Ω/\square has been achieved in HEMT material where Te

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InAs 15 Å
In _{0.4} Al _{0.6} As 40 Å
AlSb 125 Å
InAs 100 Å
AlSb 500 Å
GaSb 200 Å $p = 6 \times 10^{17} \text{ cm}^{-3}$
AlSb 2.4 μm
Si GaAs substrate

Fig. 1. HEMT starting material.

doping was used above and below the InAs quantum well [11]. In that case, the material exhibited a sheet density of $8 \times 10^{12} \text{ cm}^{-2}$ and a mobility of $19\,000 \text{ cm}^2/\text{V}\cdot\text{s}$. Because of the above properties, AlSb/InAs HEMT's have the potential for high-speed operation, particularly at low drain voltage. The combination of high sheet-charge density and strong carrier confinement in the quantum well should also enable the HEMT's to exhibit a broad g_m characteristic for highly linear operation [12]. It should be noted, however, that impact ionization in the InAs channel is significantly higher than in the other materials listed in Table I due to its narrow bandgap. The ionization rate for electrons in InAs is two orders of magnitude higher than in In_{0.53}Ga_{0.47}As channels. The full extent to which this affects the performance of InAs-channel HEMT's is still under study.

The AlSb/InAs HEMT material for the devices discussed here was grown by solid-source molecular beam epitaxy on a semi-insulating (100) GaAs substrate. A cross section of the starting material is shown in Fig. 1. A $0.5 \mu\text{m}$ buffer layer of GaAs was grown first at 580°C , followed by $0.1 \mu\text{m}$ of AlSb at 570°C and $2.3 \mu\text{m}$ of AlSb at 535°C . The temperature was then reduced to 500°C and the other layers shown in the figure were grown. All of these are undoped except the p^+ GaSb layer which is doped with Si. The $2.4 \mu\text{m}$ AlSb buffer layer was used to accommodate the 7% lattice mismatch between the HEMT material and the GaAs substrate. Modulation doping of the InAs quantum well was realized with an As soak technique which was performed between the growth of the AlSb and InAlAs barrier layers [13]. In this case, a monolayer of Al was deposited, and the Al-rich surface was soaked in an As beam for 10 s. The sheet carrier density and mobility of the resulting starting material, determined by Hall measurements at 300 K, were $1.5 \times 10^{12} \text{ cm}^{-2}$ and $16\,600 \text{ cm}^2/\text{V}\cdot\text{s}$, respectively.

III. HEMT DESIGN AND FABRICATION

Two key features of the HEMT design are the use of the In_{0.4}Al_{0.6}As/AlSb composite barrier above the InAs quantum well and the 200 Å p^+ GaSb layer located within the AlSb buffer layer [14]. The addition of the InAlAs layer has been found to enhance the insulating property of the barrier and enable a gate recess process to be employed. The p^+ GaSb layer in the buffer is intended to drain a portion of the impact-ionization-generated holes back to the source contact rather than having them remain in the AlSb buffer layer where they

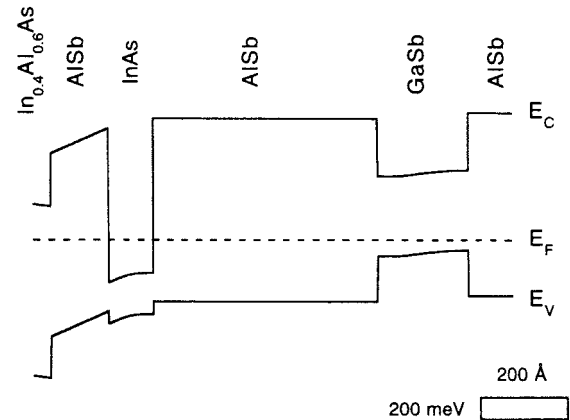


Fig. 2. Calculated band structure.

are likely to cause deleterious trapping effects [15] or be collected at the gate contact and thereby increase the gate leakage current.

The band structure of the HEMT material was calculated using a finite-difference model for the one-dimensional Poisson equation. The effects of the two-dimensional density of states and spatial redistribution of confined carriers were calculated using the Schrodinger equation for the quantum well regions. An iterative algorithm was applied to find a self-consistent solution to the equations. Strain effects were not included in the calculation and the ΔE_v of the InAlAs/AlSb heterojunction was estimated to be 350 meV . The resulting band structure, which shows the presence of the hole barrier due to the addition of the InAlAs layer, is shown in Fig. 2.

A HEMT process sequence was developed to minimize the deleterious effects of the rapid oxidation of AlSb when exposed to air. First, the source and drain ohmic contacts are defined using PMMA resist and deep-UV lithography. Pd/Pt/Au ($100\text{Å}/200\text{Å}/600\text{Å}$) layers are then deposited by e-beam evaporation and heat treated at 175°C for 3 h using a hot plate which is located in a glove box containing a $\text{H}_2:\text{N}_2$ (5:95%) ambient [16]. The resulting contacts have a smooth surface morphology and sharp edge definition.

After the ohmic contact formation, a Cr/Au Schottky-gate metallization is formed using a tri-level PMMA resist e-beam lithography and lift-off procedure. A citric-acid-based etch is performed on the exposed surface prior to gate metal deposition. Finally, device isolation is achieved by wet chemical etching. The elimination of the mesa-sidewall gate leakage current is accomplished at this step by preventing the gate metal from contacting the mesa sidewall with the use of an air-bridge between the channel and the gate bonding pad. The air bridge is formed during the hydrofluoric acid/peroxide-based mesa etch by the undercutting beneath the gate metal in the exposed regions defined by the mesa photoresist pattern. The dimensions of the mesa pattern and the gate metal feed tab extending from the gate stripe to the bonding pad are designed to minimize the final gate stripe air-bridge span and simultaneously allow complete removal of the AlSb buffer layer material in the exposed regions. Small gate anchor pads are used to facilitate air bridge formation at the ends of the gate stripe. The air bridges of a $0.2 \mu\text{m}$ HEMT, with thin gate metallization for clarity, are shown in Fig. 3.

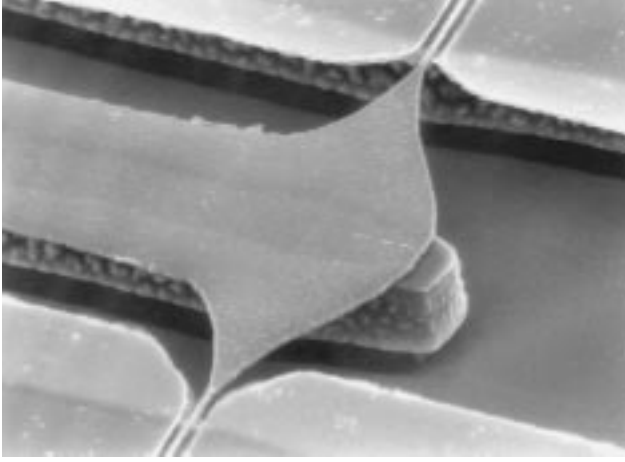


Fig. 3. SEM micrograph of gate air-bridges at mesa edge. $L_G = 0.2 \mu\text{m}$, $L_{DS} = 1.0 \mu\text{m}$.

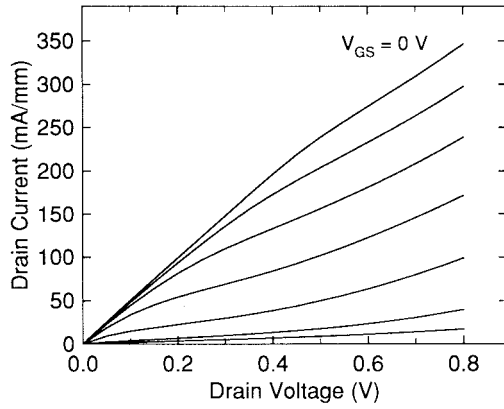


Fig. 4. $0.1 \mu\text{m}$ HEMT drain characteristics. $L_{DS} = 2.3 \mu\text{m}$, $W_G = 28 \mu\text{m}$, $V_{GS} = 0.1 \text{ V/step}$.

IV. DC CHARACTERIZATION

The AlSb/InAs HEMT's were fabricated with gate lengths in the range of $0.1\text{--}0.5 \mu\text{m}$. The drain characteristics of a $0.1 \mu\text{m}$ HEMT are shown in Fig. 4. At $V_{DS} = 0.6 \text{ V}$, a transconductance of 600 mS/mm is observed. The HEMT's of this gate length exhibit an increase in the output conductance at a drain voltage near 0.5 V due to the effects of impact ionization in the channel. The drain characteristics of a HEMT with a $0.5 \mu\text{m}$ gate length, which was fabricated on the same wafer, are shown in Fig. 5. The low-field source-drain resistance of this device is $0.8 \Omega\text{-mm}$. This HEMT has a maximum transconductance of 1 S/mm at $V_{DS} = 1 \text{ V}$. A comparison of the two figures indicates that with longer gate length, the HEMT's exhibit more saturation in the drain current apparently due to the larger gate-channel aspect ratio and the lower electric field strength under the gate which reduces the effects of impact ionization. The higher drain current density in the $0.5 \mu\text{m}$ HEMT is primarily due to a smaller source-drain spacing which results in lower access resistance. Based on measurements on HEMT's without the p^+ GaSb layer, the lack of drain current pinchoff in both HEMT's is mainly due to hole current in that layer.

AlSb/InAs HEMT's are susceptible to high gate leakage current due to the staggered type-II heterojunction band lineup

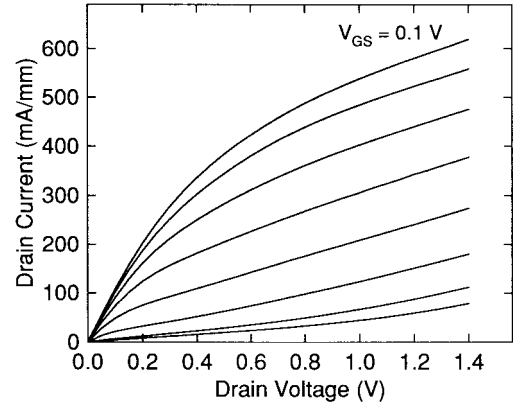


Fig. 5. $0.5 \mu\text{m}$ HEMT drain characteristics. $L_{DS} = 1.3 \mu\text{m}$, $W_G = 25 \mu\text{m}$, $V_{GS} = 0.1 \text{ V/step}$.

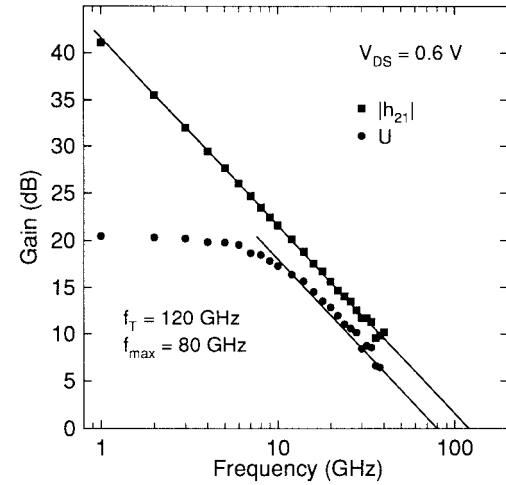


Fig. 6. Extrinsic current gain $|h_{21}|$ and unilateral gain U versus frequency.

as shown in Fig. 2. Although there is a large electron barrier, substantial hole transport can occur across the small valence band barrier between the gate and the channel. The problem is exacerbated by the increased number of holes which are present in the channel due to impact ionization [7]. With the addition of the InAlAs barrier layer and the p^+ GaSb in the buffer, the gate current was found to be reduced by an order of magnitude compared to our previous results [12]. When biased for maximum f_T , a gate leakage current of $3 \mu\text{A}$ was measured for a $0.1 \mu\text{m} \times 28 \mu\text{m}$ gate. In addition to thermally-activated hole transport in the valence band [17], components of the gate leakage current may also be caused by other processes including surface conduction and trap-assisted tunneling via deep levels which are present in the AlSb [18].

V. MICROWAVE CHARACTERIZATION

The S -parameters of the HEMT's were measured on-wafer from 1 to 40 GHz . Plots of the short-circuit current gain, $|h_{21}|$, and Mason's unilateral gain, U , of a $0.1 \mu\text{m}$ HEMT as a function of frequency are shown in Fig. 6. Based on the usual 6 dB/octave extrapolation, the device exhibits an f_T of 120 GHz and an f_{max} of 80 GHz . The drain voltage of 0.6 V represents the drain bias which maximizes the f_T value without significantly compromising the low-frequency power

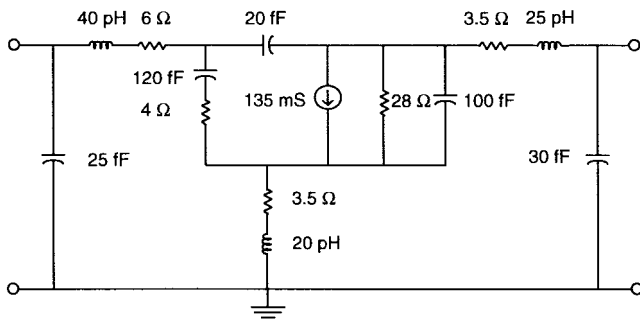


Fig. 7. Small-signal equivalent circuit. $L_G = 0.1 \mu\text{m}$, $W_G = 150 \mu\text{m}$, $V_{DS} = 0.5 \text{ V}$, $V_{GS} = -0.5 \text{ V}$.

gain. At higher drain voltages, the power gain at the lower microwave frequencies diminishes due to impact ionization, as has been reported earlier [19]. It should also be noted that at bias conditions below impact ionization, only minimal g_m and g_{ds} dispersion were observed.

An equivalent circuit of the HEMT at nominal bias, which was developed by fitting the S -parameters to a commonly-used circuit topology over the measured frequencies, is shown in Fig. 7. S -parameter measurements on gate-less HEMT's of the same geometry were utilized to model the external parasitics. A measured gate metal resistance of $280 \Omega/\text{mm}$, obtained using end-to-end resistance measurements, and the low-field source-drain resistance were also incorporated. In this circuit, the parasitic effects of the gate anchor pad capacitance and the p^+ GaSb layer have been absorbed in the remaining elements. The resulting equivalent circuit provides a good fit to the measured S -parameters up to about 20 GHz. Above this frequency some divergence occurs due to the distributed nature of the $75 \mu\text{m}$ gate stripes and p^+ layer, as well as the added complexity of the gate anchor pads. These latter effects were examined with a more complex equivalent circuit. The element values of the circuit shown are fairly normal for $0.1 \mu\text{m}$ HEMT's except that the output admittance is high. There are several reasons for this. The p^+ layer constitutes a parallel current path, impact ionization is contributing some parasitic current flow, and the velocity-field characteristic of InAs may not have a well-defined peak due to the remote upper valley which results in limited current saturation.

It is instructive to examine the effects of higher drain voltages on the equivalent circuit. As mentioned earlier, above 0.6 V the effects of impact ionization become significant. The most important effects are the increase in both output admittance and transconductance, consistent with the drain characteristics at higher drain voltages. In this region the values of f_T and f_{max} saturate due to the increased admittance. The S_{22} in this regime, particularly at lower frequencies, shows inductive characteristics related to the dynamics of impact ionization. This effect can be roughly modeled by adding a series RL branch across the intrinsic device output. The inductive behavior under impact ionization in both InAs-channel and InGaAs-channel HEMT's has been previously reported [20]. In more recent work on InGaAs channel devices, the inductive behavior was modeled by adding an active circuit in order to examine the effect of impact ionization on both the rf and noise performance [21].

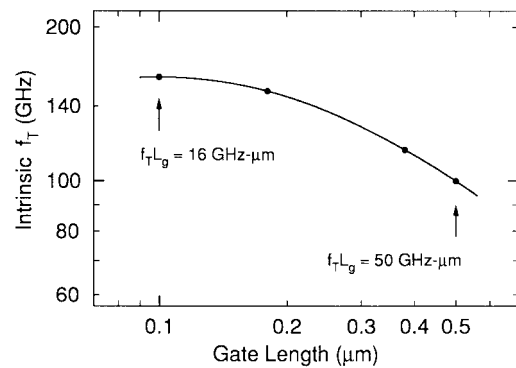


Fig. 8. Intrinsic f_T as a function of gate length.

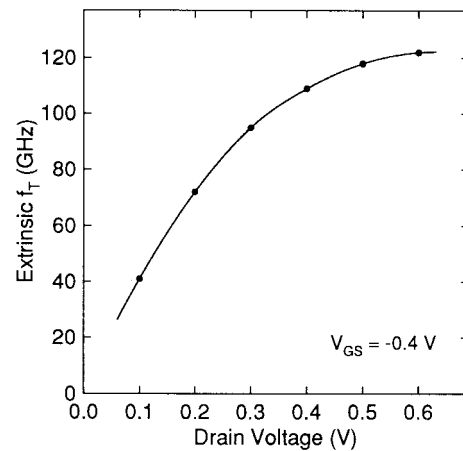


Fig. 9. Extrinsic current gain cutoff frequency f_T versus drain voltage. $L_G = 0.1 \mu\text{m}$.

In order to examine the intrinsic device characteristics, the bonding pad capacitance of the gate was removed from the equivalent circuit. The results indicated an intrinsic f_T of 160 GHz at $V_{DS} = 0.6 \text{ V}$. The removal of the p^+ GaSb layer from the complex equivalent circuit mentioned earlier increased the f_{max} to 90 GHz. Equivalent circuits were also developed for HEMT's with larger gate lengths. The intrinsic f_T as a function of gate length is plotted in Fig. 8. As shown, the $0.5 \mu\text{m}$ HEMT's have an intrinsic $f_T L_g$ product of $50 \text{ GHz-}\mu\text{m}$, which is equal to the highest previously reported for any FET in this gate length region. The highest f_{max} observed was 110 GHz which was measured on a $0.4 \mu\text{m}$ gate length HEMT that had an output conductance of 100 mS/mm , a microwave voltage gain of 7, and a f_{max}/f_T ratio of 2.

The potential for low voltage operation is shown in Fig. 9, which shows the measured f_T as a function of drain voltage for the $0.1 \mu\text{m}$ HEMT described earlier. The maximum f_T occurs at a drain voltage of 0.6 V. At a drain voltage of 0.2 V, an f_T of 72 GHz is obtained. Additional measurements on more recent $0.1 \mu\text{m}$ HEMT's, with lower access resistance, indicated an extrinsic f_T of 100 and 130 GHz at a drain voltage of 0.2 and 0.3 V, respectively.

VI. MICROWAVE NOISE MEASUREMENTS

The first measurements of the microwave noise performance of AlSb/InAs HEMT's were reported earlier [22] and for

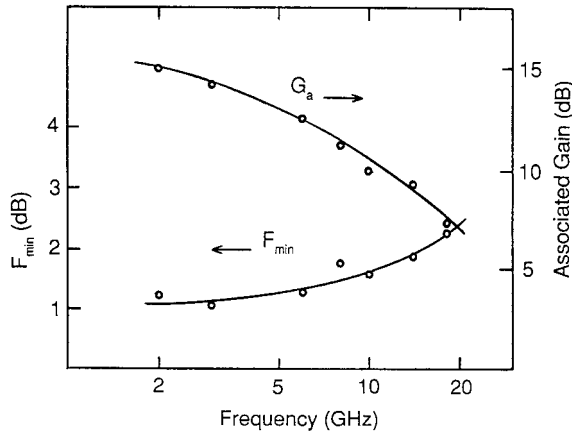


Fig. 10. F_{\min} and G_a as a function of frequency. $V_{GS} = -0.4$ V, $L_G = 0.1$ μm , $W_G = 150$ μm .

completeness are included here. The minimum noise figure, f_{\min} , and the associated gain, G_a , for a 0.1 μm device are shown as a function of frequency in Fig. 10. These measurements were made on-wafer with mechanical tuners. The input circuit loss was determined by measuring the available gain of the tuner/bias-tee combination with a network analyzer [23]. The value of V_{DS} applied to get the performance shown was adjusted from 0.35 V at 2 GHz to 0.55 V at 18 GHz. V_{GS} was picked for the best value of f_{\min} and remained constant over the frequency range.

Since these devices were not designed specifically for low-noise performance, considerable improvements are expected in a more optimal design involving a higher sheet charge density, more suitable horizontal dimensions including shorter gate stripes, smaller bonding pads, and a better barrier layer design resulting in lower gate current. In order to quantify potential improvements from these changes, a noise equivalent circuit was developed. This circuit consists essentially of the circuit shown in Fig. 7 in which the intrinsic van der Ziel partially-correlated channel and gate noise sources as well as the extrinsic noise generators due to the device resistances have been inserted. An additional noise generator was added at the input to approximate the effect of the shot noise produced by the gate leakage current [24]. The resulting circuit provides a good fit to the measured noise figure both with optimum generator impedance and with a 50 Ω generator. Adjustments were then made in the equivalent circuit consistent with expected technological improvements. The gate leakage current was reduced from the present 20 μA to 1 μA for the 150 μm device. The other improvements involve the lowering of the gate and access resistances through adjustments in the horizontal geometry and 2-DEG sheet carrier concentration. With these changes, a noise figure of 0.3 dB at 4 GHz and 0.6 dB at 10 GHz can be expected at a drain voltage of 0.5 V. Furthermore, with anticipated improvements in f_T , these values can be carried up to higher frequencies than in the present devices.

Most of the noise measurements performed in this study were carried out below or near the onset of impact ionization. To gain additional insight into the performance of these

devices, the effect of impact ionization still needs to be examined. Based on these initial measurements, however, it appears that the AlSb/InAs HEMT has considerable potential for low-voltage, low-noise operation.

VII. DISCUSSION

Most AlSb/InAs-based HEMT's previously reported displayed an anomalous increase in the dc output conductance as the drain voltage was increased. This "kink-effect" phenomenon caused degraded performance at nominal bias values and precluded the use of the devices at the electric fields required to optimize the performance. Based on measurements made on a variety of different HEMT designs at our laboratory and elsewhere [8], [25], we believe that this kink was caused by the trapping of holes generated by impact ionization in the channel. The specific characteristics of the kink as a function of bias depend on the number and location of holes generated, the number and location of available trap sites, and the hole trapping and emission dynamics. The presence of the additional positive charge associated with the trapped holes reduces carrier depletion and results in an increase in the drain current. HEMT's which suffer from a large kink effect commonly have poor drain current saturation, strong g_m compression near $V_{GS} = 0$, and a large threshold voltage shift with increasing drain voltage.

Despite the high field present under the gate, the drain characteristics of the present 0.1 μm HEMT's do not display the charge control problems associated with the kink which have been previously observed in our HEMT's with gate lengths at or below 0.2 μm [19], [25]. In addition to the previous work which attributed the kink to hole trapping in the buffer layer, our study of the present InAlAs/AlSb composite barrier HEMT's indicates that the kink can also be caused by hole trapping at or near the gate metal-semiconductor interface. These results are consistent with low-frequency output dispersion measurements in the area of the kink which were made as a function of bias and temperature [25]. In that study, it was found that the kink is associated with a dispersion mechanism which contains a broad distribution of time constants typical for interface states. Measurements on devices with and without a gate recess have shown that hole trapping in this region can be reduced through the use of a proper gate recess etch. It should be noted that control samples grown without the InAlAs/AlSb composite barrier display a prominent kink in the drain characteristics.

Optimization of the present growth process will lead to higher sheet charge densities and channel mobilities. However, as has been pointed out above, there are some fundamental HEMT design issues which must be addressed before the intrinsic material properties can be fully exploited. To realize the performance potential, improvements in the device design are required to reduce gate leakage current, reduce output admittance, minimize trapping effects, and more effectively manage the holes generated by impact ionization. Reductions in the leakage current may be achieved through optimization of the InAlAs/AlSb thickness ratio, the addition of As to the AlSb layer [6], [8], the use of a dual-gate design [26], [27],

and the use of material combinations with alloys composed of InAlAsSb [28], AlGaAsSb [9], InPSb [29], or AlPSb. The use of low-temperature growth techniques may also be used to enhance the insulating properties of the barrier and buffer layers. Optimization of the gate-recess process and cap layer design are needed to tailor the electric field profile in the gate-drain region. Finally, additional study is needed to understand the effects of the reduced intervalley transfer in the InAs channel and to determine to what extent the output admittance can be reduced using advanced designs which reduce short channel effects and impact ionization in the channel.

VIII. CONCLUSION

The fabrication and characterization of 0.1 μm AlSb/InAs HEMT's with a composite InAlAs/AlSb barrier layer above the InAs quantum well and a p^+ GaSb layer within the AlSb buffer layer have been presented. The devices exhibit a transconductance of 600 mS/mm and an f_T of 120 GHz at $V_{DS} = 0.6$ V. An intrinsic f_T of 160 GHz is obtained after removal of the gate bonding pad capacitance from the equivalent circuit. 0.5 μm HEMT's on the same wafer exhibit a transconductance of 1 S/mm and an intrinsic $f_T L_g$ product of 50 GHz- μm . At 4 GHz, the 0.1 μm HEMT's have a minimum noise figure of 1 dB with 14 dB associated gain at $V_{DS} = 0.4$ V. Noise equivalent circuit simulation has indicated that noise figures of 0.3 dB at 4 GHz and 0.6 dB at 10 GHz can be expected through technological improvements. Due to the unique material properties of this heterojunction system, continued improvements in the material growth, design, and fabrication of AlSb/InAs-based HEMT's will make them attractive candidates in future applications where high speed and low noise at very low bias voltage will be required.

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