Epitaxial Ge virtual substrates versus Ge-on-Nothing: Impact of Si in-diffusion and dislocation density on excess carrier lifetime

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Owing to its compatibility with mainstream Si technologies and remarkable physical properties, Ge has become a key enabler of modern electrical and optical semiconductor devices. In most applications, carrier mobility and carrier lifetime are critical parameters. Thin films of Ge can be epitaxially grown on low-cost Si substrates, with an impact on quality due to the large lattice and thermal expansion mismatch between the Si substrate and the active part of the device. A post-epi thermal treatment is applied to improve the layer quality and its electrical and optical material properties. A concern is the Si diffusion into the Ge layer during the thermal treatment for defect reduction. It might increase the electrical band gap of the photodetector and it reduces the excess carrier lifetime [1]. Recently, Ge-on-Nothing (GeON) has been proposed as an alternative template for strain relaxed Ge [2,3]. This template can serve as starting material for multijunction solar cells as well as for layer transfer and 3D device stacking technologies.

This contribution first re-addresses the impact of the thermal budget during the post-epi anneal of Ge epitaxially grown on Si. It will be discussed how the post-Ge epi anneal affects material properties like the surface roughness, threading dislocation density (TDD), the Si diffusion into the Ge, and, as a result, the excess carrier lifetime. Next, the excess carrier lifetimes will be compared for Ge on Si with those obtained for GeON.

As an example, the decrease in TDD with increasing Ge thickness and the corresponding increase in extracted excess carrier lifetime is shown in figure 1. With increasing Ge thickness, most of the carriers are no longer confined close to the unpassivated top Ge surface and the defective Ge/Si interface. As a result, the carrier lifetime increases. Growing thicker Ge layers and polishing the stack down to the target value has a positive impact on material defectivity. However, the approach has only a limited or no effect on the carrier lifetime, with trendlines overlapping with those obtained with epi only (Fig. 1b). A reduction of the Si in-diffusion into the Ge layer by decreasing the post-epi annealing temperature has indeed a positive impact on lifetime (Fig. 1b) despite the higher remaining TDD (Fig. 1a). Significantly higher excess carrier lifetimes have been obtained for the GeON template (Fig. 2). In this case the top Ge layer is separated from the defective Ge/Si interface. The GeON template has therefore an interesting potential for applications relying on maximal lifetimes.

[1] P. Fakhimi *et al.*, 10th Int. Conf. On Silicon Epitaxy and heterostructures (ICSI), book of abstracts, pp. 191-192 (2017)
[2] S. Park *et al.*, Joule **3** (7), pp. 1782-1793 (2019)
[3] R. Loo *et al.*, ECS J. Solid State Sci. and Techn. **10**, p. 084003 (7p) (2021)

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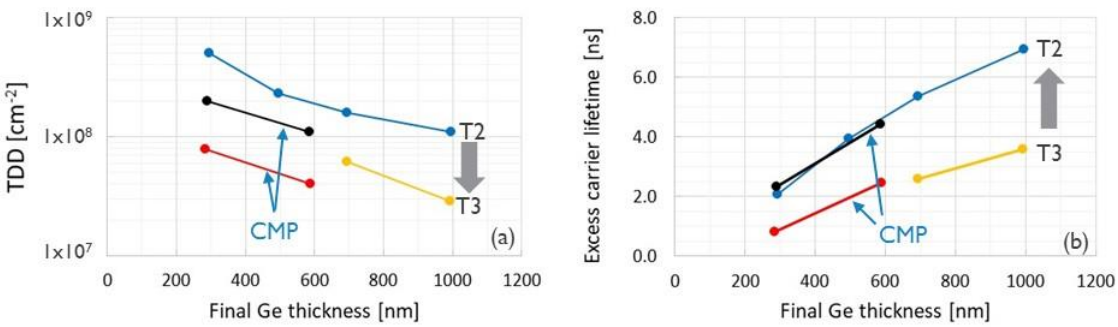

Fig. 1. a) TDD values obtained from electron channeling contrast imaging (ECCI) carried out on Ge/Si stacks with different Ge thicknesses and annealed in different conditions, as grown and after chemical mechanical polishing. The post epi anneal conditions applied on the samples of the black and red data points were identical to those of the blue and yellow data points, respectively. b) Excess carrier lifetimes obtained from TR-PL measurements from the same stacks.

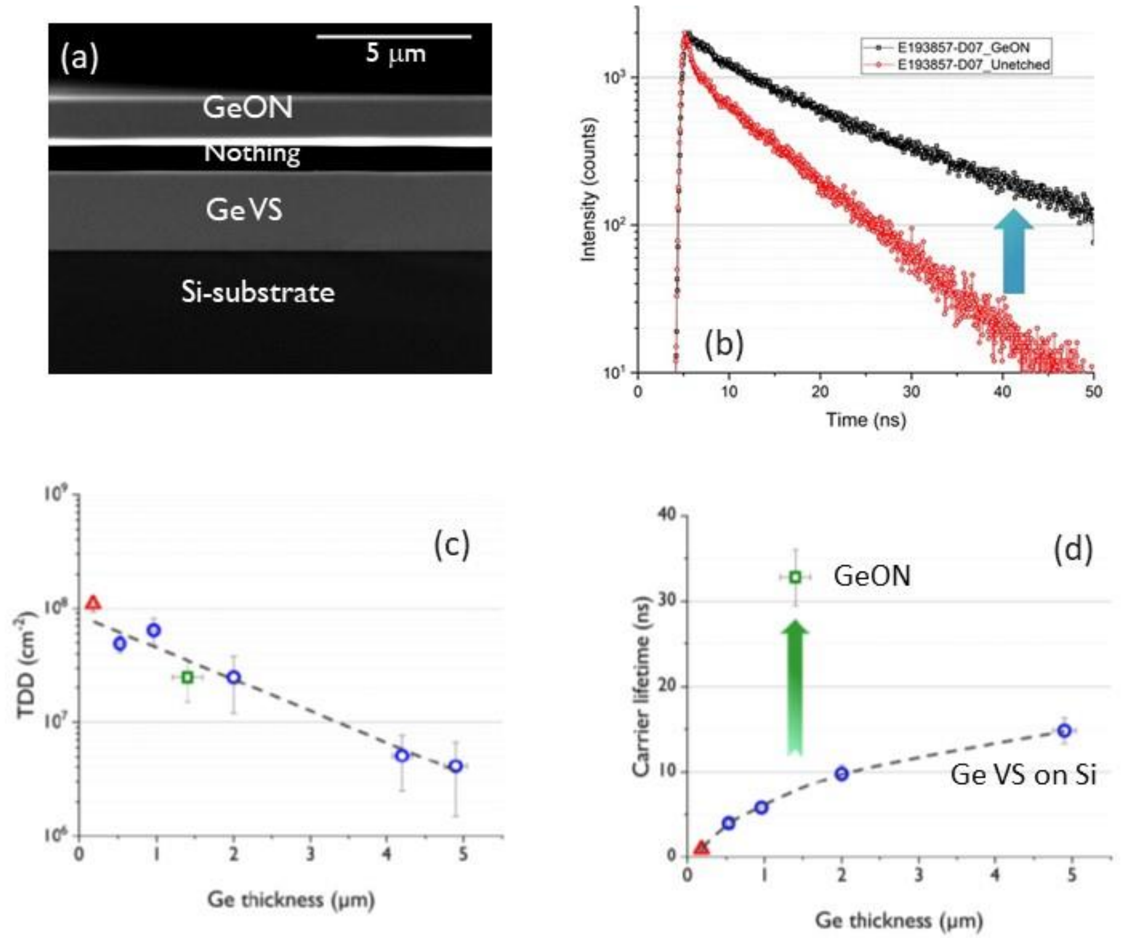

Fig. 2 a) Cross-sectional SEM image of a GeON template. b) Fluorescence decay curves of the Ge photoluminescence emission measured at 1560 nm. The red curve corresponds to a 4.3 μm Ge on unprocessed Si; the brown curve corresponds to GeON. c) Thickness dependency of TDD, estimated by ECCI, and d) excess carrier lifetimes, obtained by time resolved photoluminescence measurements, for different Ge virtual substrates (blue circles and red triangles) and GeON (green squares) samples. The dashed lines are guides for the eye.