Approaches for Wafer Level Packaging and Heterogeneous System Integration for CMOS and MEMS Sensors

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***Abstract*— This paper describes approaches for 3D integration of CMOS and MEMS sensors. It implies methods for wafer level packaging, Through-Silicon-Vias (TSV) and novel methods for heterogeneous system integration like micro-transfer-printing. These technologies are described on sensor devices.**

I. Introduction And Background

The demand for miniaturized CMOS and MEMS sensors with high performance has increased significantly in the last years. In addition to MEMS / CMOS processing, advanced technologies are required for wafer level packaging and heterogeneous system integration for achieving the needed sensor performance as well as packaging requirements. Different technologies have been developed in microelectronic and also MEMS industry and are described in literature[1,2]. Hereby, waferbonding technologies are most established processes for protection fragile micromechanical components and also for achieving the sensor functionality. TSVs are required for realization of 3D packaging or stacking of dies. In addition to common approach, the sensor functionality can be increased by heterogeneous integration of non-native components e.g. by micro-transfer-printing (µTP). This paper describes these technologies which can be applied for wafer level integration and heterogeneous system integration.

II. Results

A. Waferbonding Technologies

Joining two or more wafers by waferbonding is a common approach for wafer-level-system integration. Based on the specific sensor application, a wide range of bonding techniques are used in production and is on continuous enhancements, additionally. Thereby, process parameters of well-known bonding techniques are optimized for improving the device functionality. Furthermore, new bonding processes and integration methodologies are developed. Glass frit waferbonding is one example where bonding process parameters are in continuous improvement. Fig. 1 shows the relation between the bonding time at a fixed temperature and the resulting pressure inside of the sealed cavity, measured using X-FAB's PCM Pirani test structure. The graph illustrates that the longer the bonding time, the higher the resulting pressure, which is related to the specific out-gassing of the glass frit layer at fusion temperature.

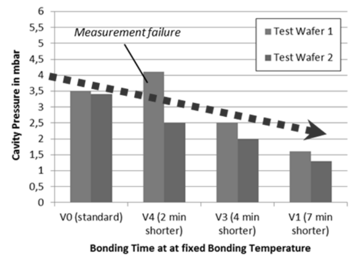

Fig. 1 Glass frit bonding: Relation between cavity pressure and bonding time[4].

B. Integration of Through Silicon Vias

In contrasts to microelectronic, the wafers for MEMS applications have to be thicker. This requires TSVs with larger geometrical dimensions and high aspect ratios. Two approaches were investigated: Via Last (TSV in bonded device) and Via Middle (TSV in cap wafer before bonding).

C. Heterogeneous System Integration by Transfer Printing

Micro-transfer-printing is a suitable technology for the integration of functional components like processed III/V devices, optical filters or special sensors on CMOS or MEMS wafers. The working principle of the micro-transfer-printing technology is to use a micro-structured elastomer stamp for the transfer of microscale functional components from their native substrate to the target substrates. The lateral dimensions of the microscale functional components can range from a few to hundreds of microns with a thickness of only a few microns. The µTP technology offers a lot of unique features for heterogeneous system integration on wafer level.

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References

[1] C. Zinck, "MEMS & Sensors Packaging Evolution: New Flexible Platforms for HVM Manufacturing", SEMI European MEMS Summit 2015.

[2] L. Hofmann et al., "3D integration approaches for MEMS and CMOS sensors based on a Cu Through-Silicon-Via technology and wafer level bonding", Proc. SPIE 9517, 2015,

[3] C. A. Bower et al., "Heterogeneous Integration of Microscale Compound Semiconductor Devices By Micro-Transfer-Printing", Proc. ECTC, 2015, pp. 963-967.

[4] R. Knechtel et al., " Glass Frit Wafer Bonding Sealed Cavity Pressure in Relation to Bonding Process Parameters", ECS 2014